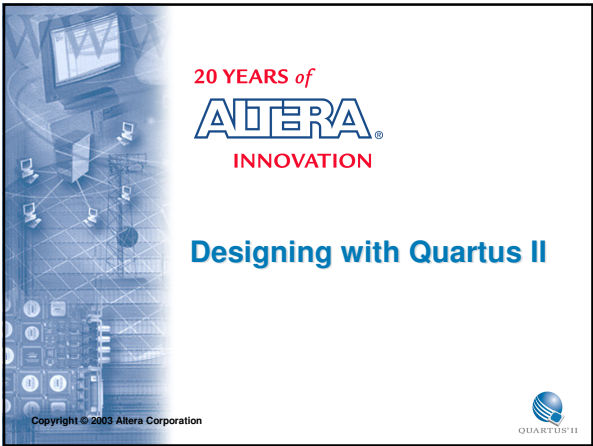
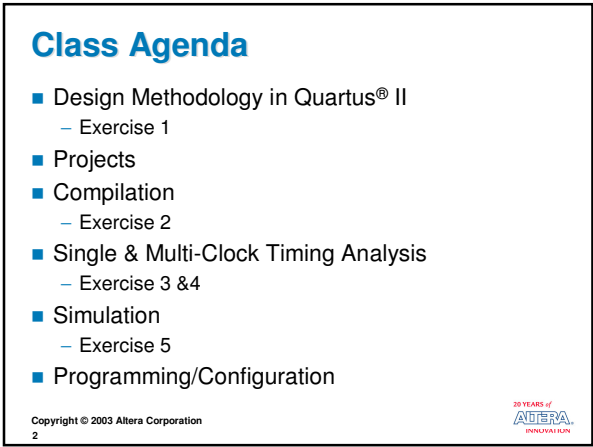








The Programmable Solutions Company®

- Programmable Devices
- Design Software
- Intellectual Property (IP)



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20 YEARS of ALTERA INNOVATION

Introduction to Altera Devices

- Programmable Logic Families
 - High & Medium Density FPGAs
 - Stratix™ II, Stratix, APEX™ II, APEX 20K, & FLEX® 10K
 - Low-Cost FPGAs
 - Cyclone™ & ACEX® 1K
 - FPGAs with Clock Data Recovery
 - Stratix GX & Mercury™
 - CPLDs
 - MAX® 7000 & MAX 3000
 - Embedded Processor Solutions
 - Nios™, Excalibur™
 - Configuration Devices
 - EPC



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20 YEARS of ALTERA INNOVATION

Introduction to Altera Design Software

- Software & Development Tools:
 - Quartus II
 - Stratix II, Stratix, Stratix GX, Cyclone, APEX II, APEX 20K/E/C, Excalibur, & Mercury Devices
 - FLEX 10K/A/E, ACEX 1K, FLEX 6000, MAX 7000S/AE/B, MAX 3000A Devices
 - Quartus II Web Edition
 - Free Version
 - Not All Features & Devices Included
 - MAX+PLUS® II
 - All FLEX, ACEX, & MAX Devices



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20 YEARS of ALTERA INNOVATION



20 YEARS of
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INNOVATION

Designing with Quartus II

*Quartus II Development System
Feature Overview*

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Quartus II Development System

- Fully-Integrated Design Tool
 - Multiple Design Entry Methods
 - Logic Synthesis
 - Place & Route
 - Simulation
 - Timing & Power Analysis
 - Device Programming

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More Features

- MegaWizard® & SOPC Builder Design Tools
- LogicLock™ Optimization Tool
- NativeLink® 3rd-Party EDA Tool Integration
- Integrated Embedded Software Development
- SignalTap® II & SignalProbe™ Debug Tools
- Windows, Solaris, HP-UX, & Linux Support
- Node-Locked & Network Licensing Options
- Revision Control Interface

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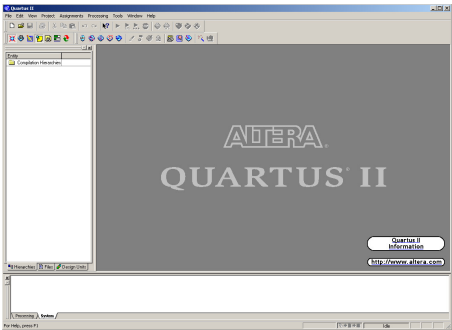
What's New in Quartus II 4.0

- SOPC Builder
- LogicLock™ Block-Based Methodology
- Assignment Editor
- Creating & Validating I/O Assignments
- IP Cores
- Integrated Synthesis
- Scripting
- Block Design Entry & Documentation
- MAX+PLUS® II Project Conversion

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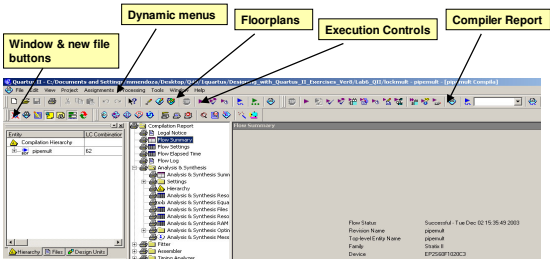
Quartus II Operating Environment



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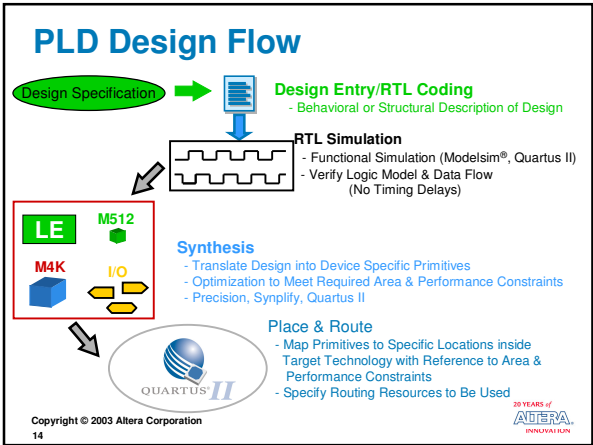
Main Toolbar & Modes

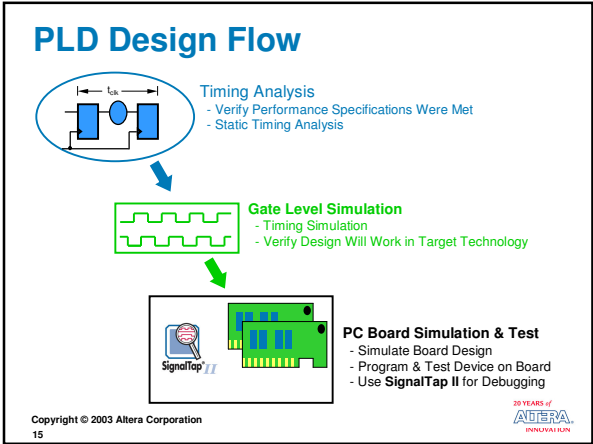


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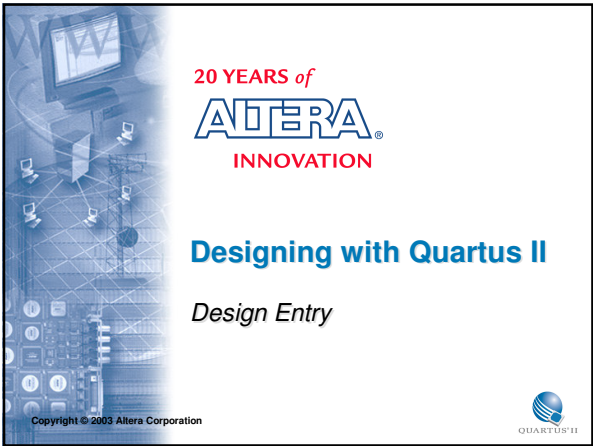








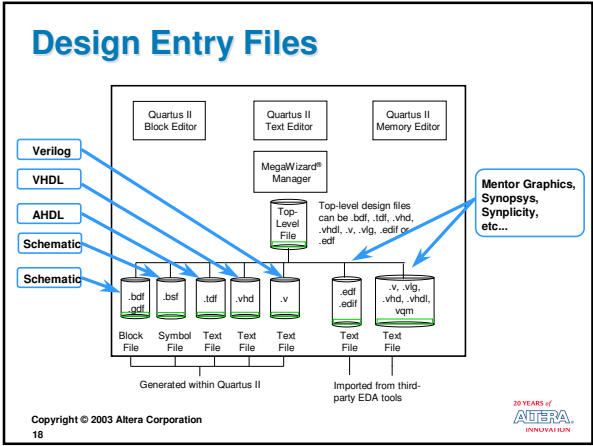
Designing with Quartus II



Design Entry Methods

- Quartus II
 - Text Editor
 - AHDL, VHDL, Verilog
 - Memory Editor
 - HEX, MIF
 - Schematic Design Entry
- 3rd-Party EDA Tools
 - EDIF
 - HDL
 - VQM
- Mixing & Matching Design Files Allowed

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Text Design Entry

- Available Features
 - Line Numbering in the HDL Text Files
 - Preview of HDL Templates
 - Syntax Coloring
 - When Editing a Text File, an Asterisk (*) Appears Next to the Filename
 - Asterisk Disappears after Saving the File
- Enter Text Description
 - AHDL (.TDF)
 - VHDL (.VHD)
 - Verilog (.V)

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Verilog & VHDL

- VHDL- VHSIC Hardware Description Language
 - 1987 & 1993 IEEE 1074 Standards Supported
- Verilog - 1995 & 2001 IEEE 1364 Standard HDL
- Create in Quartus II or any Standard Text Editor
- Use Quartus II Integrated Synthesis to Synthesize
- View Supported Commands in On-Line Help

Learn more about HDL in Altera HDL
Customer Training Classes

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AHDL

- Altera Hardware Description Language
 - High-Level Hardware Behavior Description Language
 - Used in Altera Megafunctions
 - Uses Boolean Equations, Arithmetic Operators, Truth Tables, Conditional Statements, etc.
- Create in Quartus II or any Standard Text Editor

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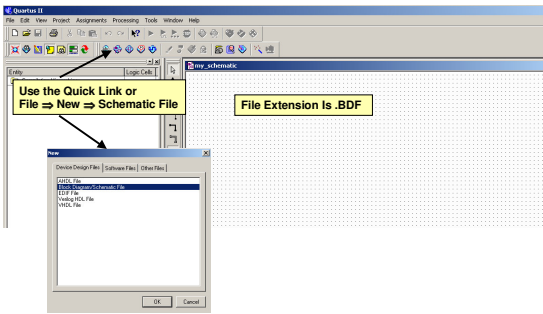




20 YEARS of
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ENHANCING LIFE

Designing with Quartus II

Create Schematic

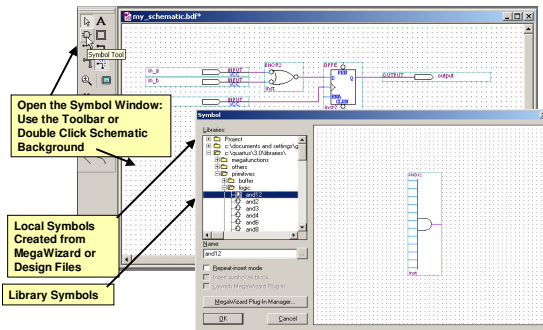


Use the Quick Link or File => New => Schematic File

File Extension is .BDF

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Insert Symbols



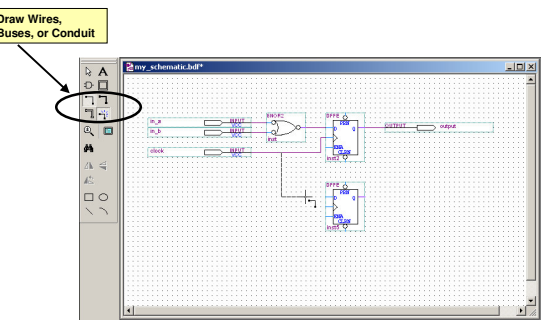
Open the Symbol Window: Use the Toolbar or Double Click Schematic Background

Local Symbols Created from MegaWizard or Design Files

Library Symbols

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Connect Wires & Buses



Draw Wires, Buses, or Conduit

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Change Names & Properties

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Create Symbols

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Optional Block Design Entity

Megafunctions

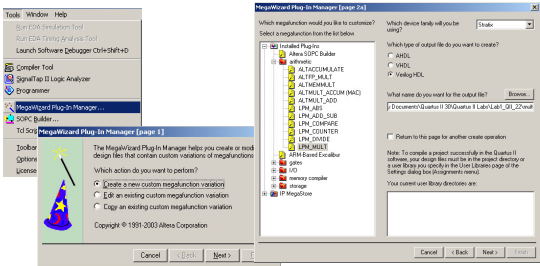
- Pre-Made Design Blocks
 - Ex. Multiply-Accumulate, PLL, Double-Data Rate
- Benefits
 - Accelerate Design Entry
 - Pre-Optimized for Altera Architecture
 - Add Flexibility
- Two Types
 - Altera-Specific Megafunctions
 - Library of Parameterized Modules (LPMs)
 - Industry Standard Logic Functions

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MegaWizard Plug-In Manager

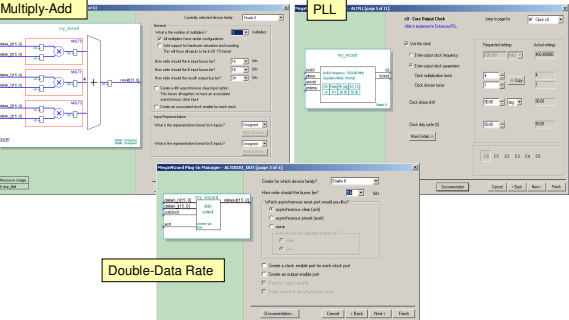
- Eases Implementation of Megafunctions & IP



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MegaWizard Examples

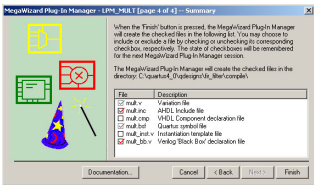


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MegaWizard Output File Selection

- Default
 - HDL Wrapper File
- Selectable
 - HDL Instantiation Template
 - VHDL Component Declaration (CMP)
 - Quartus II Symbol (BSF)
 - Verilog Black Box



Memory Editor

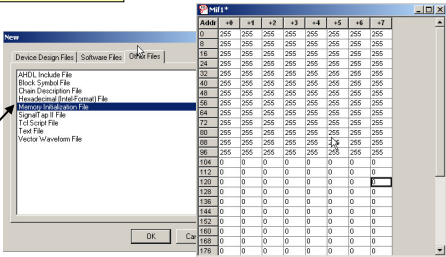
- Create or Edit Memory Initialization Files in Intel Hex (.HEX) or Altera-Specific (.MIF) Format
- Design Entry
 - Use to Initialize Your Memory Block (Ex. RAM, ROM) during Power-Up
- Simulation
 - Use to Initialize Memory Blocks before Simulation



Create Memory Initialization File

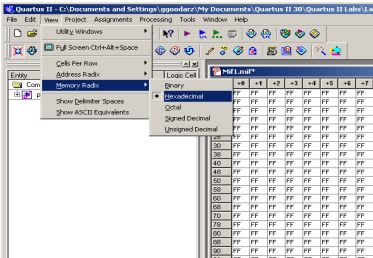
File ⇒ New ⇒ Other Files tab

HEX format or MIF format



Change Options

- View Options of Memory Editor
 - View ⇒ Select from Available Options

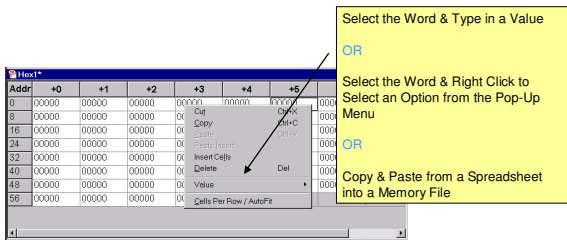


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Edit Contents

- Edit Contents of the Memory File
- Save the Memory File as .HEX or .MIF File



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Memory Size Wizard

Need to Edit Size of Memory File?

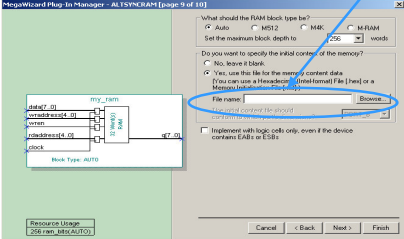
- Use the Memory Size Wizard (Edit Menu)
 - Edit Word Size
 - Edit Number of Words
 - Specify How to Handle Word Size Change
 - Increasing Word Size
 - Pad Words
 - Combine Words
 - Decreasing Word Size
 - Truncate Words from Left
 - Truncate Words from Right

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Using Memory File in Design

Specify MIF or HEX file in MegaWizard Interface

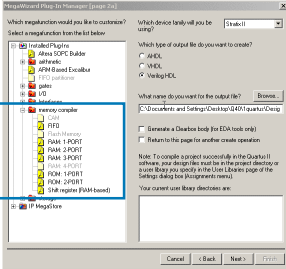


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30 YEARS of ALTERA INNOVATION

Memory Compiler

- Memory Functions are Organized by Type
- MegaWizard is Family-Aware
 - Select Memory Type & Parameters
 - Appropriate Megafunction Selected Automatically

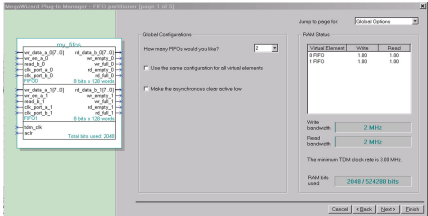


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FIFO Partitioner

- Map Multiple FIFOs into a Single Physical Memory Block
- Partition M-RAM Blocks into Multiple FIFOs



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30 YEARS of ALTERA INNOVATION

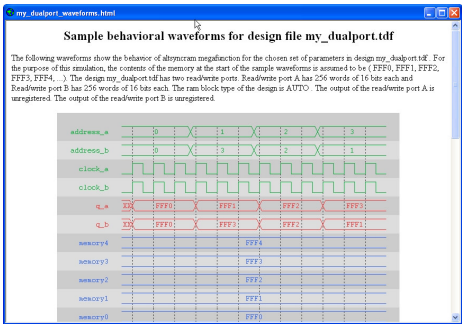
Memory Behavioral Waveforms

- HTML file Generated by MegaWizard
- Description of Memory Functionality
 - Reviews Selected Parameters
 - Describes Read & Write Operations

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Example Memory Waveform



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EDA Interfaces Introduction

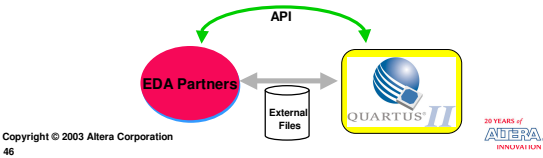
- Interface with Industry-Standard EDA Tools that Generate a Netlist File
 - EDIF 200
 - VHDL '87 or '93
 - Verilog
- NativeLink Interface Provides Seamless Integration with 3rd-party EDA Software Tools
 - Tools Pass Information/Commands in Background
 - Designers Can Complete Entire Design in One Tool

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NativeLink

- Comprised of Two Components
 - External Files
 - WYSIWYG (What You See Is What You Get) ATOM Netlist Files (EDIF, Verilog, VHDL)
 - Cross Reference Files (Ex. XRF)
 - Timing Files (Ex. SDO)
 - Application Programming Interface (API)
 - Pre-Defined Interface of Commands/Functions



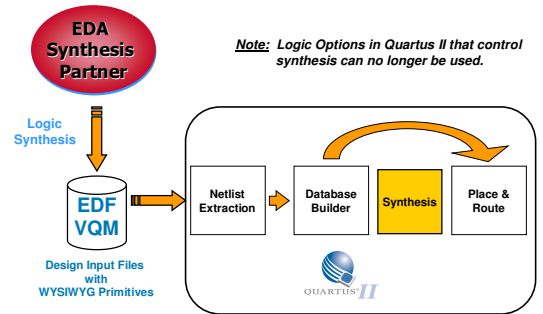
WYSIWYG ATOM Primitives

- Set of Design Primitives that Support WYSIWYG Compilation
- Provide Direct Control of How a Design Is Technology-Mapped to a Specific Target Device
- Allow Synthesis Vendors to Provide an Optimal Realization of a Design for Each Architecture

```
00104 strativ_1cell par_err_high_0_and2_62_2 (
00105   .combinout(par_err_high_0_and2_62_2),
00106   .data0(ram_out_c_11),
00107   .data1(ram_out_c_10),
00108   .data2(ram_out_c_9),
00109   .data3(ram_out_c_8)
00110 );
00111 defparam par_err_high_0_and2_62_2.operation_mode="noexal";
00112 defparam par_err_high_0_and2_62_2.lut_mask="0000";
00113 defparam par_err_high_0_and2_62_2.synch_mode="off";
00114 defparam par_err_high_0_and2_62_2.sva_lutc_input="data0";
```

Synplify .vqm

WYSIWYG Compilation Flow



Three EDA Design Flows

- Quartus II Driven Flow
 - User Launches other EDA Tools from Quartus II in the Background
 - Messages Appear in Quartus II Message Window
- Vendor Driven Flow
 - User Runs Quartus II in the Background from the 3rd-Party EDA Tool
- File Based Flow
 - Each Tool Ran Separately
 - Files Are Manually Transferred between Tools

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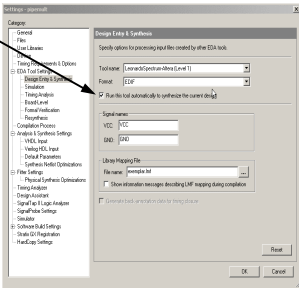
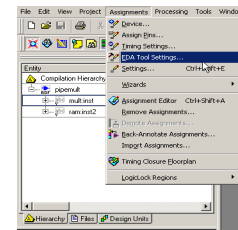


Quartus II Driven Flow

Assignments => EDA Tool Settings

Check the "Run ..." Button to Launch the EDA Tool in the Background

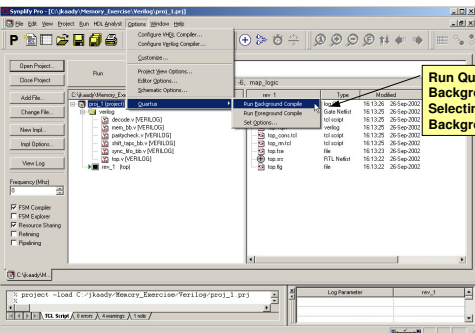
Leave Unchecked for File Based Flow



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EDA Driven Flow



Run Quartus II in the Background by Selecting Run Background Compile

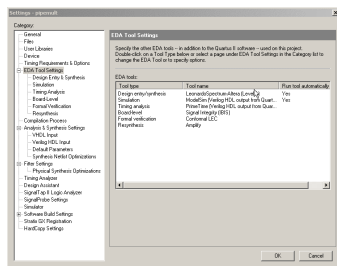
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File Based Flow

- Work Separately in Individual Tools

- Synthesis
- Simulation
- Timing Analysis
- Board-Level
- Formal Verification
- Resynthesis

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Third Party Tool Support

Synthesis Tools

- LeonardoSpectrum™
- Precision
- DesignCompiler
- FPGA Compiler II™
- FPGA Express™
- Synplify
- Synplify Pro
- Amplify

Verification Tools

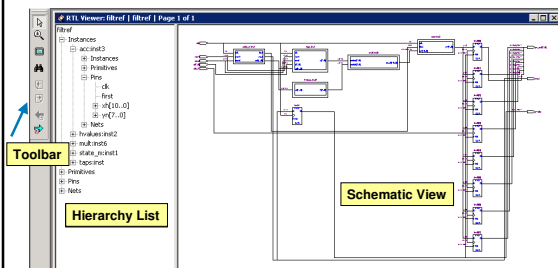
- ModelSim®
- ModelSim-Altera
- Cadence Verilog-XL
- Cadence NC-Verilog
- Cadence NC-VHDL
- Innoveda BLAST
- PrimeTime®
- Synopsys® VCS & VSS
- Mentor Graphics® Tau
- Synopsys Scirocco

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RTL Viewer

- Graphically Represents Results of Synthesis



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RTL Viewer Uses

- Visually Checking Initial HDL Synthesis Results
 - Before Any Quartus II Optimizations
- Locating Synthesized Nodes for Assigning Constraints
- Debugging Verification Issues
- Reading VQM/EDIF Netlist Files

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Starting RTL Viewer

1. Run Analysis & Elaboration (Processing Menu or )
 - Any Processing that Performs Elaboration
2. Open RTL Viewer
 - Tools Menu or 
 - Displays Last Successful Compilation

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RTL Viewer Features

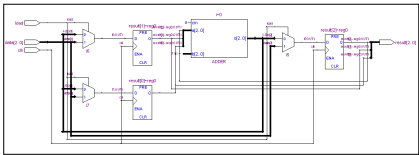
- Schematic View
- Hierarchy List
- Hierarchy Navigation
- Filter Schematic
- Page Control

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Schematic View



- Represents Design Using Logic Blocks & Nets
 - Registers
 - Muxes
 - Gates
 - Adders

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Hierarchy List

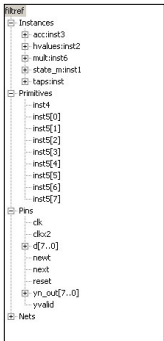
- Traverses between Design Hierarchy
- Views Logic Schematic for Each Hierarchical Level
- Breaks down Design into Netlist Elements

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Netlist Elements

- Instances
 - Lower Hierarchy Levels that Can Be Expanded (Unless Encrypted)
- Primitives
 - Low-level Nodes/Blocks that Cannot Be Expanded
- Pins
 - I/O Ports in the Current Level of Hierarchy
- Nets
 - Nets or Wires that Connect Nodes



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Using Hierarchy List

Highlighting a Netlist Element in Hierarchy List Highlights/Views that Element in the Schematic View

Expanding Instances Shows the Instances, Pins & Nets within Internal Modules

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Hierarchy Navigation

- Hierarchy List
 1. Click on Netlist Element (Ex. Instance)
 2. Schematic View Automatically Adjusts Hierarchical Level to Show Element
- Schematic View
 - Mouse Pointer Indicates Action
 - ← Descending Hierarchy
 - Double-Click on Instance
 - Right-Click & Select **Hierarchy Down**
 - ← Ascending Hierarchy
 - Double-Click in Empty Space
 - Right-Click & Select **Hierarchy Up**

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Filter Schematic

Unfiltered: All Components & Paths Shown

Filtered: Only Selected Components & Related Paths Displayed

Right-Click for Filter Menu

Filter Options

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Filter Options

- Sources, Destinations, Sources & Destinations

- Between Selected Nodes

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More on Filtering

- Displays Only Nodes on Current Hierarchy Level
- Stops Tracing Paths at
 - Hierarchical Ports
 - Registers
 - Option to Disable (Tools Menu ⇒ Options)
 - Specified Number of Logic Levels
 - 10 by Default (Tools Menu ⇒ Options)

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Page Control

- Schematic Automatically Partitioned
- Option to Control Design Size Per Page (Tools Menu ⇒ Options)
 - Nodes Per Page
 - 1 – 1000 (Default: 50)
 - Ports Per Page
 - 1 – 2000 (Default: 1000)

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Managing Pages

- Title Bar Indicates Number of Pages

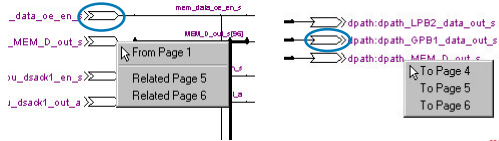


- Moving between Pages
 - Next Page/Previous Page
 - Moves between Partitioned Pages
 - Back/Forward
 - Displays Previously Viewed Design Views

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Nets between Pages

- Indicated by Special I/O Connectors
- Right-Click to Trace within Hierarchy
 - From Page (Source)
 - To Page (Destination)
 - Related (Other Parallel Connections)



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Other Features

- Go to Net Driver
 - Traces Net Back to Source Driver
 - Changes Schematic View if Necessary
- Locate in Design File
 - Finds Node Definition in Source File

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Exercise 1

Please go to Exercise 1 in the Exercise Manual

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Exercise Summary

- Schematic Design Entry is Simple
- MegaWizard Makes It Easy
 - Implements Many Design Entities in AHDL, Verilog, or VHDL
 - Makes Best Use of the Device Architecture
 - Has Direct Link to Make IP Downloads Even Easier
- Analysis & Elaboration Option Checks the File

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20 YEARS of

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INNOVATION

Summary

- Multiple Design Entry Methods
 - Text (Verilog, VHDL, AHDL)
 - Third Party Netlist (VQM, EDF)
 - Schematic
- Memory Editor
- MegaWizard
- EDA Tool Flows
- RTL Viewer

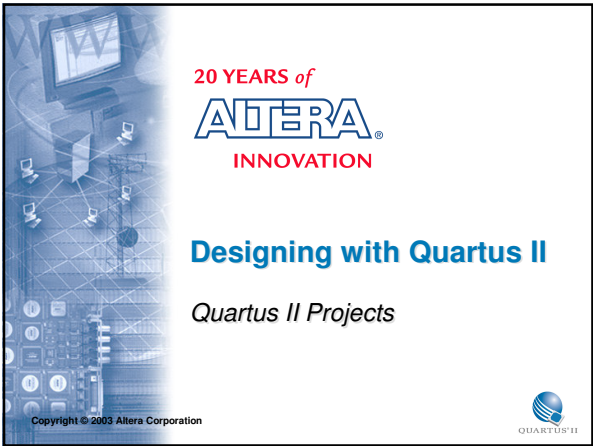
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INNOVATION



Quartus II Projects

- Description
 - Collection of Related Design Files & Libraries
 - Must Have at Least One Designated Top-Level Entity
 - Target a Single Device or Can Be Partitioned into Multiple Devices
 - Store Settings in Quartus Settings File (.QSF)
- Create New Projects with New Project Wizard
 - Can Be Created Using Tcl Scripts

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New Project Wizard

Invoke New Project Wizard

Select Working Directory

Name of Project Can Be Any Name; Recommend Using Top-Level File Name

Top-level Entity Does Not Need to Be the Same Name as Top-Level File Name

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Add Files

Add Design Files

- Graphic (.BDF, .GDF)
- AHDL
- VHDL
- Verilog
- EDIF

Notes:

- Files in project directory do not need to be added
- Add top level file if filename & entity name are not the same

Add User Library Pathnames & Files

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User Libraries

Add User Library Paths

- User Libraries
- MegaCore®/AMPP Sm Libraries
- Pre-Compiled VHDL Packages

User Library Pathnames

Add any non-default libraries that you will use in the project. List the library names in the order you want to search them. Custom libraries can contain user-defined or vendor-supplied regular functions. Block Symbol Files, AHDL, Verilog files, and pre-compiled VHDL packages.

Library name: Add Remove Up Down

Libraries: c:\megacore\h_compiler\2.5.0\lib

OK Cancel

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EDA Tool Settings

Choose EDA Tools

Add or Change Settings Later

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Device Selection

Which device family do you wish to target?
Family: **Strata II**

Do you want to assign a specific device?
☒ No, I want to allow the Compiler to choose a device

Back Next Finish Cancel

Choose the Device Family

Auto Device or Choose a Specific Device

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Device Selection

Available devices:

- EP2K10K10 (Advanced)
- EP2K10K10-1 (Advanced)
- EP2K10K10-2 (Advanced)
- EP2K10K10-3 (Advanced)
- EP2K10K10-4 (Advanced)
- EP2K10K10-5 (Advanced)
- EP2K10K10-6 (Advanced)
- EP2K10K10-7 (Advanced)
- EP2K10K10-8 (Advanced)
- EP2K10K10-9 (Advanced)
- EP2K10K10-10 (Advanced)
- EP2K10K10-11 (Advanced)
- EP2K10K10-12 (Advanced)
- EP2K10K10-13 (Advanced)
- EP2K10K10-14 (Advanced)
- EP2K10K10-15 (Advanced)
- EP2K10K10-16 (Advanced)
- EP2K10K10-17 (Advanced)
- EP2K10K10-18 (Advanced)
- EP2K10K10-19 (Advanced)
- EP2K10K10-20 (Advanced)
- EP2K10K10-21 (Advanced)
- EP2K10K10-22 (Advanced)
- EP2K10K10-23 (Advanced)
- EP2K10K10-24 (Advanced)
- EP2K10K10-25 (Advanced)
- EP2K10K10-26 (Advanced)
- EP2K10K10-27 (Advanced)
- EP2K10K10-28 (Advanced)
- EP2K10K10-29 (Advanced)
- EP2K10K10-30 (Advanced)
- EP2K10K10-31 (Advanced)
- EP2K10K10-32 (Advanced)
- EP2K10K10-33 (Advanced)
- EP2K10K10-34 (Advanced)
- EP2K10K10-35 (Advanced)
- EP2K10K10-36 (Advanced)
- EP2K10K10-37 (Advanced)
- EP2K10K10-38 (Advanced)
- EP2K10K10-39 (Advanced)
- EP2K10K10-40 (Advanced)
- EP2K10K10-41 (Advanced)
- EP2K10K10-42 (Advanced)
- EP2K10K10-43 (Advanced)
- EP2K10K10-44 (Advanced)
- EP2K10K10-45 (Advanced)
- EP2K10K10-46 (Advanced)
- EP2K10K10-47 (Advanced)
- EP2K10K10-48 (Advanced)
- EP2K10K10-49 (Advanced)
- EP2K10K10-50 (Advanced)
- EP2K10K10-51 (Advanced)
- EP2K10K10-52 (Advanced)
- EP2K10K10-53 (Advanced)
- EP2K10K10-54 (Advanced)
- EP2K10K10-55 (Advanced)
- EP2K10K10-56 (Advanced)
- EP2K10K10-57 (Advanced)
- EP2K10K10-58 (Advanced)
- EP2K10K10-59 (Advanced)
- EP2K10K10-60 (Advanced)
- EP2K10K10-61 (Advanced)
- EP2K10K10-62 (Advanced)
- EP2K10K10-63 (Advanced)
- EP2K10K10-64 (Advanced)
- EP2K10K10-65 (Advanced)
- EP2K10K10-66 (Advanced)
- EP2K10K10-67 (Advanced)
- EP2K10K10-68 (Advanced)
- EP2K10K10-69 (Advanced)
- EP2K10K10-70 (Advanced)
- EP2K10K10-71 (Advanced)
- EP2K10K10-72 (Advanced)
- EP2K10K10-73 (Advanced)
- EP2K10K10-74 (Advanced)
- EP2K10K10-75 (Advanced)
- EP2K10K10-76 (Advanced)
- EP2K10K10-77 (Advanced)
- EP2K10K10-78 (Advanced)
- EP2K10K10-79 (Advanced)
- EP2K10K10-80 (Advanced)
- EP2K10K10-81 (Advanced)
- EP2K10K10-82 (Advanced)
- EP2K10K10-83 (Advanced)
- EP2K10K10-84 (Advanced)
- EP2K10K10-85 (Advanced)
- EP2K10K10-86 (Advanced)
- EP2K10K10-87 (Advanced)
- EP2K10K10-88 (Advanced)
- EP2K10K10-89 (Advanced)
- EP2K10K10-90 (Advanced)
- EP2K10K10-91 (Advanced)
- EP2K10K10-92 (Advanced)
- EP2K10K10-93 (Advanced)
- EP2K10K10-94 (Advanced)
- EP2K10K10-95 (Advanced)
- EP2K10K10-96 (Advanced)
- EP2K10K10-97 (Advanced)
- EP2K10K10-98 (Advanced)
- EP2K10K10-99 (Advanced)
- EP2K10K10-100 (Advanced)

Filters:

Package: Any
Pin count: Any
Speed grade: Any
Voltage: 1.5V

Back Next Finish Cancel

Use Filters for Auto Selection or Picking a Specific Device

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Done!

When you click Finish, your project will be created with the following settings:

Project directory: c:\test_designs\memory_test_4\1\

Project name: Lab6_Oil

Top-level design entity: Lab6_Oil

Number of files added: 0

Number of user libraries added: 0

EDA tools:

- Design entry/synthesis: <None>
- Simulation: <None>
- Timing analysis: <None>
- Board design: <None>

Device assignment:

- Family name: Strata II
- Device: EP2K10K10-1

Back Next Finish Cancel

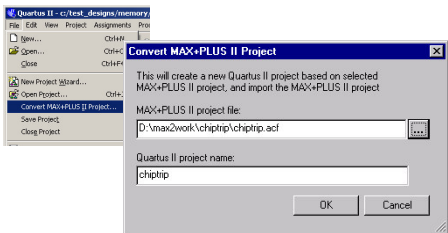
Review Results & Click on Finish

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MAX+PLUS II to Quartus II

- Convert MAX+PLUS II Projects into Quartus II Projects
- Assignments Automatically Translated

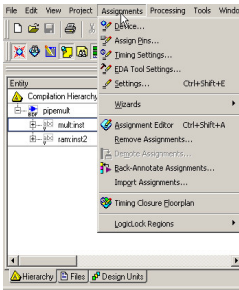
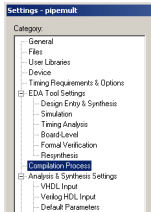


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Assignments Menu

- Accesses All Assignments & Settings
- Opens Settings Dialog Box

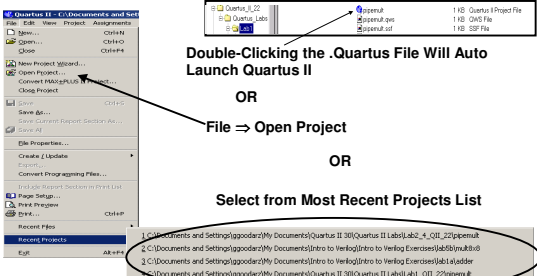


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Editing Project Settings

- Open Existing Project First to Edit Settings

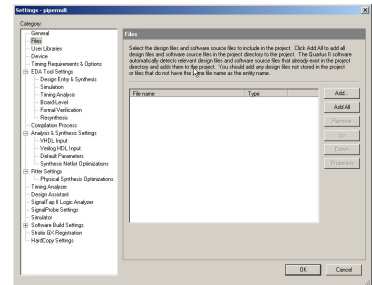


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Editing Project Settings (cont.)

■ Assignments ⇒ Settings

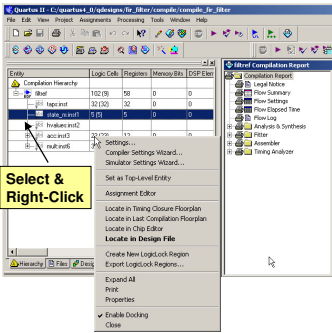


- Change Settings**
- Rename
 - Add/Remove Files
 - Libraries
 - VHDL '87, '93?
 - Verilog '85, '01?
 - EDA Tool Settings
 - Timing Settings
 - Compiler Settings
 - Simulator Settings

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Project Navigator – Hierarchy Tab

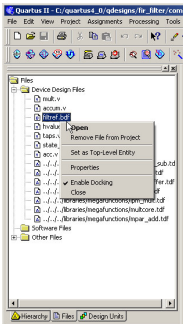


- Displays Project Hierarchy after Project Is Analyzed
- Uses
 - Set Top-Level Entity
 - Make Assignments
 - Locate in Design Files, Floorplan or Chip Editor
 - View Resource Usage
 - Drag & Drop Hierarchical Blocks

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Project Navigator – Files Tab



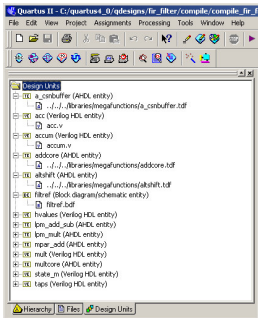
- Shows All Files in Project
 - All Source Files Appear under Design Files
- Uses
 - Open Files
 - Remove Files from Project
 - Set New Top-Level Entity

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Project Navigator - Design Units Tab

- Displays each Design Unit & Type
 - VHDL Entity
 - VHDL Architecture
 - Verilog Module
 - AHDL Subdesign
 - Block Diagram Filename
- Details the File which Instantiates Design Unit



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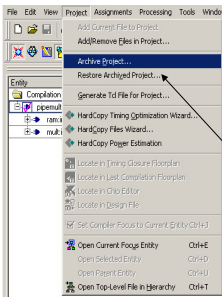
Project Files

- Quartus Project File (QPF)
 - Quartus II Version
 - Time Stamp
 - Active Revision
- Quartus Default File (QDF)
 - Project Defaults
 - Name: assignment_defaults.qdf
 - Local or Bin Directory
 - Local Read First

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Project Archive & Restore



- Archive Project Creates:**
1. <project>.QAR
 - Compressed Archive File
 - Options to Choose which Files Get Archived
 2. <project>.QARLOG
 - Log of Archive Activity

- Restore Archived Project:**
- Restores Complete Project & Library Function Files from <project>.QAR File

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Summary

- Use Project Wizard to Create New Projects
- Use Assignments Menu Dialog Boxes to
 - Edit Existing Project Settings
 - Edit Third-Party Tools
- Use Project Navigator to Study File & Entity Relationships within Project

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Designing with Quartus II

Quartus II Compilation

QUARTUS II

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Quartus II Compilation

- Synthesis
- Fitting
- Generating Output
 - Timing Analysis Output Netlist
 - Simulation Output Netlists
 - Programming/Configuration Output Files

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A-MNL-QUARTUSII-09 v4.0

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Controlling Synthesis & Fitting

- Two Methods to Control Logic Synthesis & Fitting Operations
 - Settings
 - Project-Wide Switches
 - Assignments (i.e. Logic Options; Constraints)
 - Individual Entity/Node Controls

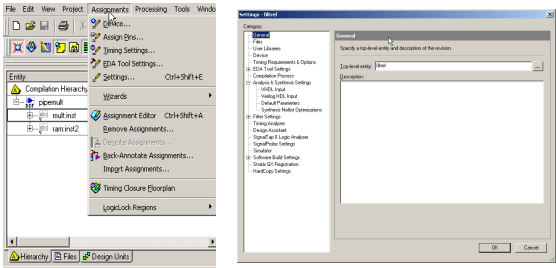


Settings

- Examples
 - Device Selection
 - Pin Assignments
 - Synthesis Optimization
 - Fitter Optimization
 - Physical Synthesis
- Located in Settings Dialog Box (Assignments Menu)



Editing Settings



Assignments → Settings

Several Options Control
Compilation & Device Options



Device Selection

Change Device Type

Migration Devices

Specify Device & Pin Options

- General
- Configuration
- Programming Files
- Unused Pins
- Dual Purpose Pins
- Voltage

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Compilation Process

Smart Compilation

- Used for Incremental Re-Compilation
- Saves Compiler Time
- Uses More Disk Space
- Preserve Node Names
- Disable for VHDL/Verilog Synthesis

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Synthesis Options

Global Optimization Goal

- Select Speed vs. Area or Balanced

Logic Replacement

- Replace Logic with Equivalent Megfunction

State Machine Processing

- Auto, One-Hot or Minimal Bit

Seed

- Controls Initial Placement Configuration
- Different Seeds Give Different Fmax

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Synthesis Netlist Optimizations

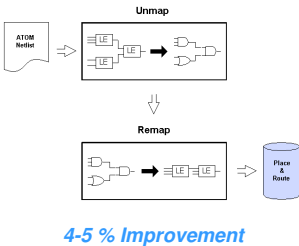
- Further Optimize Netlists during Synthesis
- Types
 - WYSIWYG Primitive Resynthesis
 - Gate-Level Register Retiming

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WYSIWYG Primitive Resynthesis

- Unmaps 3rd-Party Atom Netlist Back to Gates & then Remaps to Altera Primitives
 - Unavailable when Using Integrated Synthesis
- Considerations
 - Node Names May Change
 - 3rd-Party Synthesis Attributes May Be Lost
 - Preserve/Keep
 - Some Registers May Be Synthesized Away

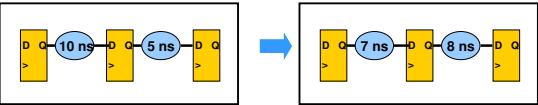


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Gate-Level Register Retiming

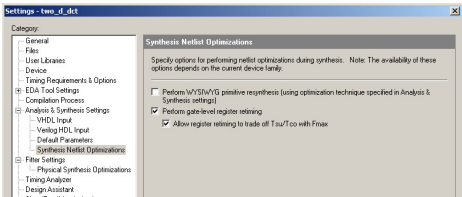
- Moves Registers across Combinatorial Logic to Balance Timing
- Trades between Critical & Non-Critical Paths
- Makes Changes at Gate Level



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Enabling Synthesis Optimizations

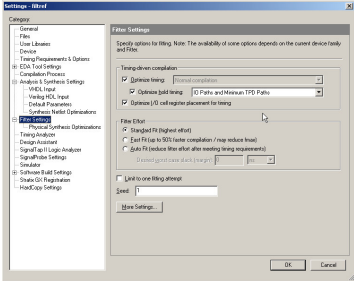


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Fitter Optimizations

- Timing Driven Compilation**
 - Optimize Internal Timing
 - Optimize I/O Register Placement
- Compilation Speed/Fitter Effort**
 - Standard Fit (Highest Effort)
 - Fast Fit (Faster Compile but Possibly Lesser Design Performance)
 - Auto Fit (Compile Stops after Meeting Timing)
 - One Fitting Attempt
- Seed**
 - Controls Initial Placement Configuration



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Physical Synthesis

- Re-Synthesis Based on Fitter Output
 - Makes Incremental Changes that Improve Results for a Given Placement in Altera Device
 - Compensates for Routing Delays from Fitter
 - Routing Delays Large Part of Typical Critical Path Delay
- Types
 - Combinational Logic
 - Registers
 - Register Duplication
 - Register Retiming

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Combinational Logic

- Swaps Look-Up Table (LUT) Ports within LEs to Reduce Critical Path LEs
- Allows LUT Duplication to Enable Further Optimizations on the Critical Path

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Register Duplication

- High Fan-Out Register Is Duplicated & Placed to Reduce Delay
 - Combinational Logic May Also Be Duplicated

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Enabling Physical Synthesis

Created/Modified Nodes Noted in Compilation Report

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More Netlist Optimizations Info

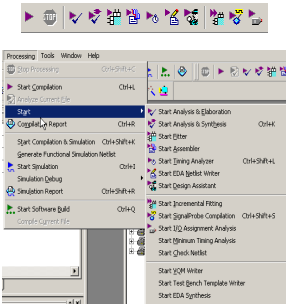
- Disable Optimizations on Specific Entities/Nodes
 - Set **Netlist Optimizations** Logic Option to **Never Allow**
 - Entities/Nodes Cannot Be Altered
- Prevent Nodes from Being Optimized Away
 - HDL Attributes
 - Use **PRESERVE** (Registers) or **KEEP** (Combinational Logic)
 - **Preserve** Logic Option
- Unsafe Registers & Logic Remain Unaffected
 - Registers with Certain Timing Constraints
 - Registers that Feed Clocks, Asynchronous Controls
 - Registers Fed by Registers in Other Clock Domains

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Processing Options

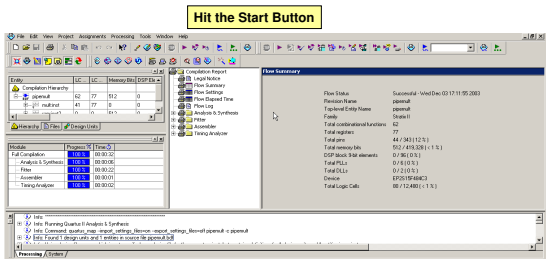
- Start Compilation
 - Perform Full Compilation
- Start Analysis & Elaboration
 - Check Syntax & Build Database Only
- Start Analysis & Synthesis
 - Synthesize Code & Estimate Timing
- Start Fitter
- Start Assembler
- Start Timing Analysis
- Start I/O Assignment Analysis
- Start Design Assistant



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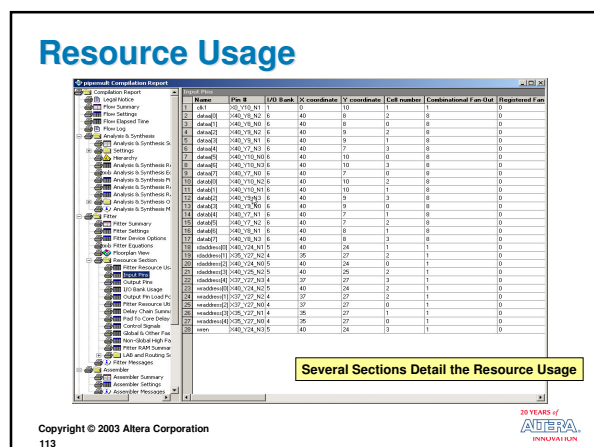
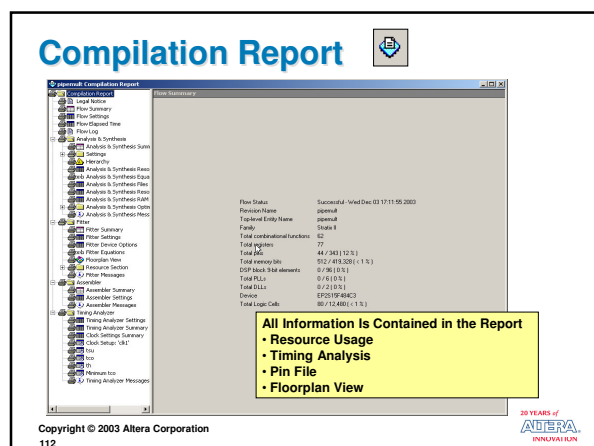
Status & Message Windows



- Status Bars Scroll to Indicate Progress
- Message Window Displays Informational, Warning, & Error Messages

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Floorplan



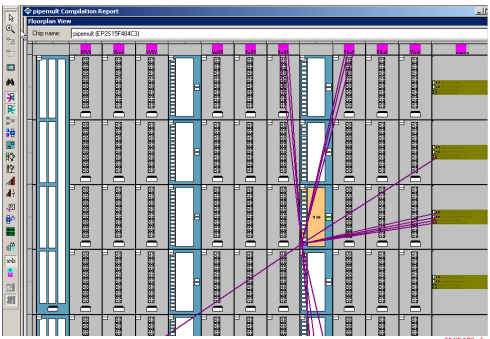
- Available Views
 - Last Compilation
 - Chip Editor
 - Timing Closure
- Uses
 - Make Assignments
 - View Placement
 - View Connections

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[illegible]

Floorplan View



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Assignments

- Assignment Editor
- Example Assignments
- I/O Assignments & Analysis

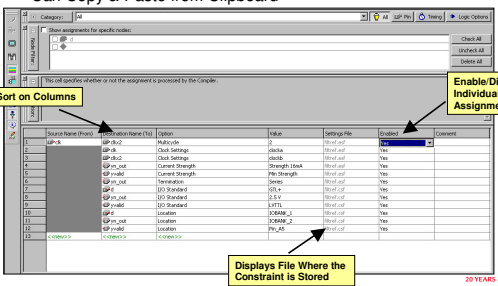
- Perform Analysis & Elaboration before Obtaining Hierarchy & Node Information

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Assignment Editor (AE)

- Provides Spreadsheet Assignment Entry & Display
 - Can Copy & Paste from Clipboard



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Designing with Quartus II

Opening Assignment Editor

The screenshot shows the Altera Quartus II software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, and Window. The 'Assignments' menu is open, showing options like Compiler Settings Wizard..., Simulation Settings Wizard..., Assignment Editor, Locate in Timing Closure Floorplan, Locate in Last Compilation Floorplan, Locate in Chip Editor, and Locate in Design File. The 'Assignment Editor' option is highlighted. A yellow callout box labeled 'Assignments Menu' points to the 'Assignments' menu in the top toolbar. The 'Assignment Editor' dialog box is also visible, showing the 'General' tab with options for Compiler Settings Wizard..., Simulation Settings Wizard..., Assignment Editor, Locate in Timing Closure Floorplan, Locate in Last Compilation Floorplan, Locate in Chip Editor, and Locate in Design File. The 'Assignment Editor' option is highlighted.

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Opening Assignment Editor (cont.)

- Locate to Assignment Editor from Timing Report, Messages, Etc

The screenshot shows the Cadence Virtuoso environment. On the left, the 'Messages' window is open, displaying a list of messages. The 'Assignment Editor' menu item is highlighted in the 'Edit' menu. The main window displays a timing report for a circuit named 'circuit1'. The 'Messages' window shows a list of messages, including 'Timing Report for circuit1' and 'Timing Report for circuit1'.

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The screenshot displays the 'Assignment Editor' window. On the left, a table lists assignments with columns for 'Source Name', 'Destination N.', 'Option', and 'Value'. The table contains 13 rows of data. On the right, a list of available options is shown, including 'CPU Utilization', 'Disk I/O', 'Network I/O', and 'System Uptime'. A callout box points to the 'Option' column header, stating 'Double-Click Cells to Edit or Add New Assignment'. Another callout box points to the 'Option' column, stating 'Launches Node Finder'. A third callout box points to the 'Option' column, stating 'Selecting an Option Determines which Fields are Available for Editing'.

Source Name	Destination N.	Option	Value
1	0	CPU Utilization	10.0
2	0	Disk I/O	10.0
3	0	Network I/O	10.0
4	0	System Uptime	10.0
5	0	CPU Utilization	10.0
6	0	Disk I/O	10.0
7	0	Network I/O	10.0
8	0	System Uptime	10.0
9	0	CPU Utilization	10.0
10	0	Disk I/O	10.0
11	0	Network I/O	10.0
12	0	System Uptime	10.0
13	0	CPU Utilization	10.0

Double-Click Cells to Edit or Add New Assignment

Launches Node Finder

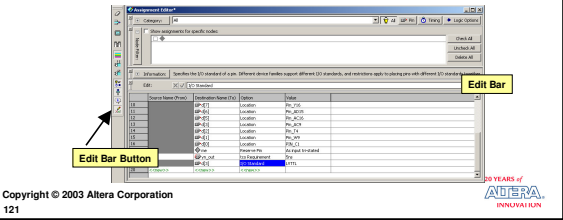
Selecting an Option Determines which Fields are Available for Editing

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Entering Assignments

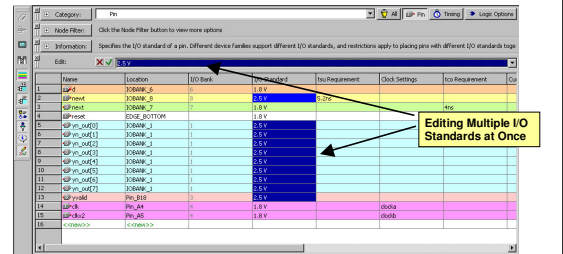
- Other Ways to Edit Cells
 - Single-Click & Type Name Directly
 - Useful for Known Node Names
 - Edit Menu
 - Edit Bar



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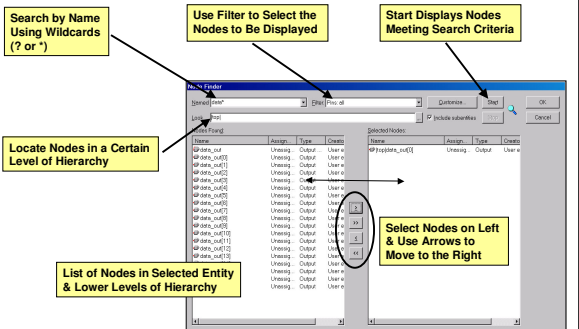
Editing Multiple Assignments

- Edit Multiple Constraints Simultaneously
 - Select Multiple Pins & Use Edit Bar (Click Check Mark to Accept)



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Node Finder



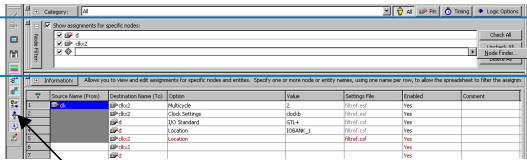
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AE Node Filter Bar



- Enables/Disables Selective Filtering of Constraints Displayed Based on Node Name
- Can Be Hidden or Minimized



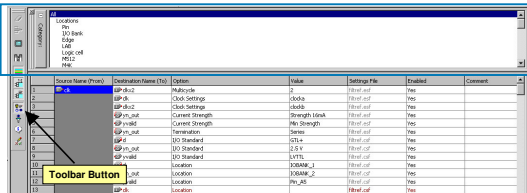
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AE Category Bar



- Selects Category of Assignments to View
 - Ex. Pin Assignments, Timing Assignments
- Can Be Hidden or Minimized

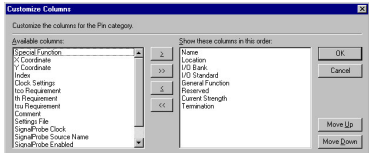


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AE Customizable Columns

- Each Category Has a Set of Customizable Columns
 - Ex. Include Common Timing Assignments in Pin Category
- Comment Column for Each Assignment



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AE Tcl Commands

- Equivalent Tcl Commands Are Displayed as Assignments Are Entered
 - Manually Copy to Create Tcl Scripts
 - Export Command (File Menu) Writes All Assignments to a Tcl File

Assignments Editor

Source Name (Value)

Destination Name (Tcl)

Value

1	AD_CONVERT	AD_CONVERT	AD_CONVERT
2	AD_CONVERT	AD_CONVERT	AD_CONVERT
3	AD_CONVERT	AD_CONVERT	AD_CONVERT
4	AD_CONVERT	AD_CONVERT	AD_CONVERT
5	AD_CONVERT	AD_CONVERT	AD_CONVERT
6	AD_CONVERT	AD_CONVERT	AD_CONVERT
7	AD_CONVERT	AD_CONVERT	AD_CONVERT
8	AD_CONVERT	AD_CONVERT	AD_CONVERT
9	AD_CONVERT	AD_CONVERT	AD_CONVERT
10	AD_CONVERT	AD_CONVERT	AD_CONVERT
11	AD_CONVERT	AD_CONVERT	AD_CONVERT
12	AD_CONVERT	AD_CONVERT	AD_CONVERT
13	AD_CONVERT	AD_CONVERT	AD_CONVERT
14	AD_CONVERT	AD_CONVERT	AD_CONVERT
15	AD_CONVERT	AD_CONVERT	AD_CONVERT
16	AD_CONVERT	AD_CONVERT	AD_CONVERT
17	AD_CONVERT	AD_CONVERT	AD_CONVERT
18	AD_CONVERT	AD_CONVERT	AD_CONVERT
19	AD_CONVERT	AD_CONVERT	AD_CONVERT
20	AD_CONVERT	AD_CONVERT	AD_CONVERT

Message Window

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Example Assignments

- Optimization Technique
- PCI I/O
- Output Pin Load

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OPTIMIZATION TECHNIQUE

- Selects Synthesis Optimization Goal
 - Speed (Default)
 - Area
- Applies Only to Hierarchical Entities
- Effects Synthesis & Logic Mapping
- Only Applies to Quartus II Integrated Synthesis

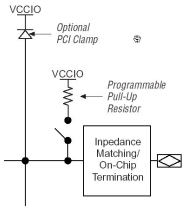
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PCI I/O

- Turns on PCI Compatibility for Pins
 - Ignored If Applied to Anything other than a Pin or a Top-Level Design Entity
- Controls Clamping Diode Located in the I/O Elements



Output Pin Load

I/O Standard	Load	Capacitance (pF)
LVCMOS	10 pF	10 pF
LVCMOS1	10 pF	10 pF
LVCMOS2	10 pF	10 pF
LVCMOS3	10 pF	10 pF
LVCMOS4	10 pF	10 pF
LVCMOS5	10 pF	10 pF
LVCMOS6	10 pF	10 pF
LVCMOS7	10 pF	10 pF
LVCMOS8	10 pF	10 pF
LVCMOS9	10 pF	10 pF
LVCMOS10	10 pF	10 pF
LVCMOS11	10 pF	10 pF
LVCMOS12	10 pF	10 pF
LVCMOS13	10 pF	10 pF
LVCMOS14	10 pF	10 pF
LVCMOS15	10 pF	10 pF
LVCMOS16	10 pF	10 pF
LVCMOS17	10 pF	10 pF
LVCMOS18	10 pF	10 pF
LVCMOS19	10 pF	10 pF
LVCMOS20	10 pF	10 pF
LVCMOS21	10 pF	10 pF
LVCMOS22	10 pF	10 pF
LVCMOS23	10 pF	10 pF
LVCMOS24	10 pF	10 pF
LVCMOS25	10 pF	10 pF
LVCMOS26	10 pF	10 pF
LVCMOS27	10 pF	10 pF
LVCMOS28	10 pF	10 pF
LVCMOS29	10 pF	10 pF
LVCMOS30	10 pF	10 pF
LVCMOS31	10 pF	10 pF
LVCMOS32	10 pF	10 pF
LVCMOS33	10 pF	10 pF
LVCMOS34	10 pF	10 pF
LVCMOS35	10 pF	10 pF
LVCMOS36	10 pF	10 pF
LVCMOS37	10 pF	10 pF
LVCMOS38	10 pF	10 pF
LVCMOS39	10 pF	10 pF
LVCMOS40	10 pF	10 pF
LVCMOS41	10 pF	10 pF
LVCMOS42	10 pF	10 pF
LVCMOS43	10 pF	10 pF
LVCMOS44	10 pF	10 pF
LVCMOS45	10 pF	10 pF
LVCMOS46	10 pF	10 pF
LVCMOS47	10 pF	10 pF
LVCMOS48	10 pF	10 pF
LVCMOS49	10 pF	10 pF
LVCMOS50	10 pF	10 pF
LVCMOS51	10 pF	10 pF
LVCMOS52	10 pF	10 pF
LVCMOS53	10 pF	10 pF
LVCMOS54	10 pF	10 pF
LVCMOS55	10 pF	10 pF
LVCMOS56	10 pF	10 pF
LVCMOS57	10 pF	10 pF
LVCMOS58	10 pF	10 pF
LVCMOS59	10 pF	10 pF
LVCMOS60	10 pF	10 pF
LVCMOS61	10 pF	10 pF
LVCMOS62	10 pF	10 pF
LVCMOS63	10 pF	10 pF
LVCMOS64	10 pF	10 pF
LVCMOS65	10 pF	10 pF
LVCMOS66	10 pF	10 pF
LVCMOS67	10 pF	10 pF
LVCMOS68	10 pF	10 pF
LVCMOS69	10 pF	10 pF
LVCMOS70	10 pF	10 pF
LVCMOS71	10 pF	10 pF
LVCMOS72	10 pF	10 pF
LVCMOS73	10 pF	10 pF
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LVCMOS78	10 pF	10 pF
LVCMOS79	10 pF	10 pF
LVCMOS80	10 pF	10 pF
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LVCMOS82	10 pF	10 pF
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LVCMOS86	10 pF	10 pF
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LVCMOS89	10 pF	10 pF
LVCMOS90	10 pF	10 pF
LVCMOS91	10 pF	10 pF
LVCMOS92	10 pF	10 pF
LVCMOS93	10 pF	10 pF
LVCMOS94	10 pF	10 pF
LVCMOS95	10 pF	10 pF
LVCMOS96	10 pF	10 pF
LVCMOS97	10 pF	10 pF
LVCMOS98	10 pF	10 pF
LVCMOS99	10 pF	10 pF
LVCMOS100	10 pF	10 pF

- Specifies Output Pin Loading in picoFarads (pF)
 - Changes Default Loading Value of I/O Standard
 - Changes t_{co} of Output Pins
- Allows Designer to Accurately Model Board Conditions
- Must Be Applied to Output or Bidirectional Pins

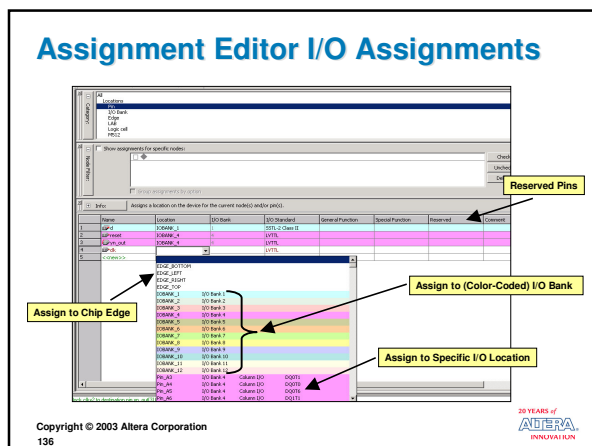


I/O (Pin) Assignments

- Make I/O Assignments Quickly
 - Assignment Editor
 - Settings Dialog Box (Device)
 - Scripting
 - Floorplan
- Specific Pin Location Unnecessary
 - IO Bank & Chip Edge Location Assignments
 - Reserved Pins with or without Locations



Assignment Editor I/O Assignments



AE Show All Known Pin Names

- Populate Spreadsheet with List of All Pin Names in Design
 - Assigned & Not Assigned

	Name	Address	IO bank	IO Standard	General Function	Special Function	Reserved
1	GP-0	77..C1		1VTTT	pin I/O	GPIO_0[2:0]	
2	GP-1			1VTTT			
3	GP-2			1VTTT			
4	GP-3			1VTTT			
5	GP-4			1VTTT			
6	GP-5			1VTTT			
7	GP-6			1VTTT			
8	GP-7			1VTTT			
9	GP-8			1VTTT			
10	GP-9			1VTTT			
11	GP-10			1VTTT			
12	GP-11			1VTTT			
13	GP-12			1VTTT			
14	GP-13			1VTTT			
15	GP-14			1VTTT			
16	GP-15			1VTTT			
17	GP-16			1VTTT			
18	GP-17			1VTTT			
19	GP-18			1VTTT			
20	GP-19			1VTTT			
21	GP-20			1VTTT			
22	GP-21			1VTTT			
23	GP-22			1VTTT			
24	GP-23			1VTTT			
25	GP-24			1VTTT			
26			CGMIO-0				

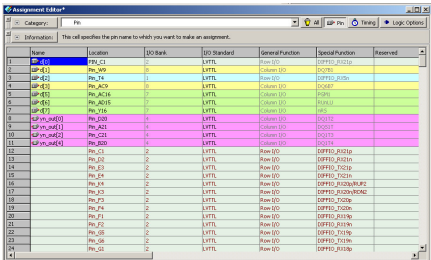
AE Assignable Pin Numbers

- Show All Assignable Pin Numbers
 - Populate Spreadsheet with All Pin Numbers Available for Assignment

	Input	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved
1	INP0_0	PORTC_0	2	LVTTL	Row I/O	EEPROM_A021p	
2	INP0_1	PORTC_1	2	LVTTL	Row I/O	EEPROM_A021p	
3	INP0_2	PORTC_2	2	LVTTL	Row I/O	EEPROM_A021p	
4	INP0_3	PORTC_3	2	LVTTL	Row I/O	EEPROM_A021p	
5	INP0_4	PORTC_4	2	LVTTL	Row I/O	EEPROM_A021p	
6	INP0_5	PORTC_5	2	LVTTL	Row I/O	EEPROM_A021p	
7	INP0_6	PORTC_6	2	LVTTL	Row I/O	EEPROM_A021p	
8	INP0_7	PORTC_7	2	LVTTL	Row I/O	EEPROM_A021p	
9	INP0_8	PORTC_8	2	LVTTL	Row I/O	EEPROM_A021p	
10	INP0_9	PORTC_9	2	LVTTL	Row I/O	EEPROM_A021p	
11	INP0_10	PORTC_10	2	LVTTL	Row I/O	EEPROM_A021p	
12	INP0_11	PORTC_11	2	LVTTL	Row I/O	EEPROM_A021p	
13	INP0_12	PORTC_12	2	LVTTL	Row I/O	EEPROM_A021p	
14	INP0_13	PORTC_13	2	LVTTL	Row I/O	EEPROM_A021p	
15	INP0_14	PORTC_14	2	LVTTL	Row I/O	EEPROM_A021p	
16	INP0_15	PORTC_15	2	LVTTL	Row I/O	EEPROM_A021p	
17	INP0_16	PORTC_16	2	LVTTL	Row I/O	EEPROM_A021p	
18	INP0_17	PORTC_17	2	LVTTL	Row I/O	EEPROM_A021p	
19	INP0_18	PORTC_18	2	LVTTL	Row I/O	EEPROM_A021p	
20	INP0_19	PORTC_19	2	LVTTL	Row I/O	EEPROM_A021p	
21	INP0_20	PORTC_20	2	LVTTL	Row I/O	EEPROM_A021p	
22	INP0_21	PORTC_21	2	LVTTL	Row I/O	EEPROM_A021p	
23	INP0_22	PORTC_22	2	LVTTL	Row I/O	EEPROM_A021p	
24	INP0_23	PORTC_23	2	LVTTL	Row I/O	EEPROM_A021p	
25	INP0_24	PORTC_24	2	LVTTL	Row I/O	EEPROM_A021p	
26	INP0_25	PORTC_25	2	LVTTL	Row I/O	EEPROM_A021p	
27	INP0_26	PORTC_26	2	LVTTL	Row I/O	EEPROM_A021p	
28	INP0_27	PORTC_27	2	LVTTL	Row I/O	EEPROM_A021p	
29	INP0_28	PORTC_28	2	LVTTL	Row I/O	EEPROM_A021p	
30	INP0_29	PORTC_29	2	LVTTL	Row I/O	EEPROM_A021p	
31	INP0_30	PORTC_30	2	LVTTL	Row I/O	EEPROM_A021p	
32	INP0_31	PORTC_31	2	LVTTL	Row I/O	EEPROM_A021p	
33	INP0_32	PORTC_32	2	LVTTL	Row I/O	EEPROM_A021p	
34	INP0_33	PORTC_33	2	LVTTL	Row I/O	EEPROM_A021p	
35	INP0_34	PORTC_34	2	LVTTL	Row I/O	EEPROM_A021p	
36	INP0_35	PORTC_35	2	LVTTL	Row I/O	EEPROM_A021p	
37	INP0_36	PORTC_36	2	LVTTL	Row I/O	EEPROM_A021p	
38	INP0_37	PORTC_37	2	LVTTL	Row I/O	EEPROM_A021p	
39	INP0_38	PORTC_38	2	LVTTL	Row I/O	EEPROM_A021p	
40	INP0_39	PORTC_39	2	LVTTL	Row I/O	EEPROM_A021p	
41	INP0_40	PORTC_40	2	LVTTL	Row I/O	EEPROM_A021p	
42	INP0_41	PORTC_41	2	LVTTL	Row I/O	EEPROM_A021p	
43	INP0_42	PORTC_42	2	LVTTL	Row I/O	EEPROM_A021p	
44	INP0_43	PORTC_43	2	LVTTL	Row I/O	EEPROM_A021p	
45	INP0_44	PORTC_44	2	LVTTL	Row I/O	EEPROM_A021p	
46	INP0_45	PORTC_45	2	LVTTL	Row I/O	EEPROM_A021p	
47	INP0_46	PORTC_46	2	LVTTL	Row I/O	EEPROM_A021p	
48	INP0_47	PORTC_47	2	LVTTL	Row I/O	EEPROM_A021p	
49	INP0_48	PORTC_48	2	LVTTL	Row I/O	EEPROM_A021p	
50	INP0_49	PORTC_49	2	LVTTL	Row I/O	EEPROM_A021p	
51	INP0_50	PORTC_50	2	LVTTL	Row I/O	EEPROM_A021p	
52	INP0_51	PORTC_51	2	LVTTL	Row I/O	EEPROM_A021p	
53	INP0_52	PORTC_52	2	LVTTL	Row I/O	EEPROM_A021p	
54	INP0_53	PORTC_53	2	LVTTL	Row I/O	EEPROM_A021p	
55	INP0_54	PORTC_54	2	LVTTL	Row I/O	EEPROM_A021p	
56	INP0_55	PORTC_55	2	LVTTL	Row I/O	EEPROM_A021p	
57	INP0_56	PORTC_56	2	LVTTL	Row I/O	EEPROM_A021p	
58	INP0_57	PORTC_57	2	LVTTL	Row I/O	EEPROM_A021p	
59	INP0_58	PORTC_58	2	LVTTL	Row I/O	EEPROM_A021p	
60	INP0_59	PORTC_59	2	LVTTL	Row I/O	EEPROM_A021p	
61	INP0_60	PORTC_60	2	LVTTL	Row I/O	EEPROM_A021p	
62	INP0_61	PORTC_61	2	LVTTL	Row I/O	EEPROM_A021p	
63	INP0_62	PORTC_62	2	LVTTL	Row I/O	EEPROM_A021p	
64	INP0_63	PORTC_63	2	LVTTL	Row I/O	EEPROM_A021p	
65	INP0_64	PORTC_64	2	LVTTL	Row I/O	EEPROM_A021p	
66	INP0_65	PORTC_65	2	LVTTL	Row I/O	EEPROM_A021p	
67	INP0_66	PORTC_66	2	LVTTL	Row I/O	EEPROM_A021p	
68	INP0_67	PORTC_67	2	LVTTL	Row I/O	EEPROM_A021p	
69	INP0_68	PORTC_68	2	LVTTL	Row I/O	EEPROM_A021p	
70	INP0_69	PORTC_69	2	LVTTL	Row I/O	EEPROM_A021p	
71	INP0_70	PORTC_70	2	LVTTL	Row I/O	EEPROM_A021p	
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73	INP0_72	PORTC_72	2	LVTTL	Row I/O	EEPROM_A021p	
74	INP0_73	PORTC_73	2	LVTTL	Row I/O	EEPROM_A021p	
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81	INP0_80	PORTC_80	2	LVTTL	Row I/O	EEPROM_A021p	
82	INP0_81	PORTC_81	2	LVTTL	Row I/O	EEPROM_A021p	
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101	INP0_100	PORTC_100	2	LVTTL	Row I/O	EEPROM_A021p	
102	INP0_101	PORTC_101	2	LVTTL	Row I/O	EEPROM_A021p	
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165	INP0_164	PORTC_164	2	LVTTL	Row I/O	EEPROM_A021p	
166	INP0_165	PORTC_165	2	LVTTL	Row I/O	EEPROM_A021p	
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169	INP0_168	PORTC_168	2	LVTTL	Row I/O	EEPROM_A021p	
170	INP0_169	PORTC_169	2	LVTTL	Row I/O	EEPROM_A021p	
171	INP0_170	PORTC_170	2	LVTTL	Row I/O	EEPROM_A021p	
172	INP0_171	PORTC_171	2	LVTTL	Row I/O	EEPROM_A021p	
173	INP0_172	PORTC_172	2	LVTTL	Row I/O	EEPROM_A021p	
174	INP0_173	PORTC_173	2	LVTTL	Row I/O	EEPROM_A021p	
175	INP0_174	PORTC_174	2	LVTTL	Row I/O	EEPROM_A021p	
176	INP0_175	PORTC_175	2	LVTTL	Row I/O		

AE Show I/O Banks in Color

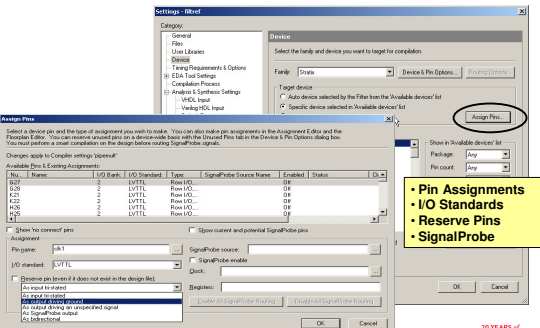
- Enable/Disable I/O Color Coding of Spreadsheet Based upon Floorplan



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20 YEARS of ALTERA INNOVATION

Setting Dialog Box - Device



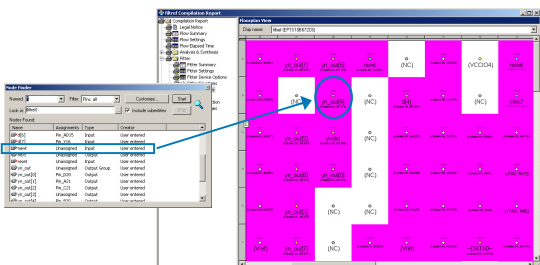
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20 YEARS of ALTERA INNOVATION

- Pin Assignments
- I/O Standards
- Reserve Pins
- SignalProbe

Drag & Drop I/O Assignments

- Drag & Drop from Node Finder to Floorplan



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20 YEARS of ALTERA INNOVATION

I/O Assignment Problems

- I/O Selected & Verified Too Far into Design Cycle
- Variety of Complex I/O Standards on Single Device
 - Not All Supported on Every I/O Block
- I/O Placement Limitations
 - Current Strength
 - Single-Ended vs. Differential
 - Single-Ended vs. V_{ref}

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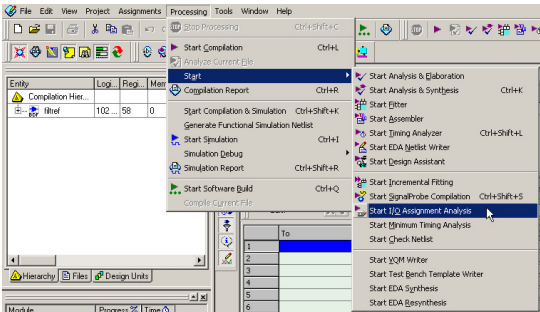
I/O Assignment Solution

- I/O Assignment Analysis Command
 - Quickly Checks Legality of I/O Assignments
 - Checks All Assignments
 - Does Not Stop at First Failure
 - Allows User to Identify & Correct Pin-Related Issues without Full Compilation
 - Has Two Usages
 - Performing Legality Checks Based on User Reserved Pin Assignments with Partial or No Design Files
 - Performing Legality Checks Based on User I/O Assignments with a Complete Design

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I/O Assignment Analysis



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I/O Analysis Requirements

- I/O Declaration
 - HDL Port Declaration
 - Reserved Pin
- Pin-Related Assignments
 - I/O Standard
 - Current Strength
 - Pin Location (Pin, Bank, Edge)
 - PCI Clamping Diode
 - Toggle Rate

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Legality Checks

Rule (subset of the rules)	Incomplete Design	Complete Design
Differential Pin Spacing		●
# of Output/Bidirs Toggling with a VREF		●
Blocks Directly Feeding or Fed by I/O pins		●
Current Strength	●	●
DC Current Draw	●	●
Pin Location	●	●
I/O Bank Capacity	●	●
Voltage Conflict (Vref, VCCIO)	●	●
On-Chip Termination	●	●

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I/O Assignment Analysis Notes

- Uses Toggle Rate Assignment
 - Set Toggle_rate = 0 for Very Low Frequency Output Pins
 - Allows Single Ended Pins to be Placed Closer to Differential Pins
- Invokes Smart Recompile for I/O Features
 - Delay Chains
 - Drive Strengths
 - Bus Hold

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I/O Assignment Analysis Output

- Detailed Messages on
 - Incorrect I/O Assignments & Problem Description
 - Compiler Assumptions that User did Not Specify
 - Pins Changing Functionality with Pin-Migration
 - Used I/O Standards & Voltages per I/O Bank
- Compilation Report (Fitter Section)
 - I/O Pin Tables
 - Show User & Fitter Assigned I/O
 - Shows Partial Placement Results in Floorplan to Help Debug Fitting Errors
- Messages Locate to Assignment Editor & Floorplan to Explain Placement Failure

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I/O Assignment Analysis Messages

Messages

- Info: Running Quartus II Fitter
- Info: Command: quartus_ii -report_settings -fitter-on -report_settings -fitter-off compile_3_0 -fitter -check_pin
- Info: Selected device EPF10K10-10 for design build
- Info: Selected migration device bit is legal with ESD tool of registration pin
- Info: Selected device migration path can use 5 pins as regular I/Os
 - Info: Pin A020
 - Info: Pin A021
 - Info: Pin A025
 - Info: Pin A026
 - Info: Pin A027
- Info: Selected device migration path can use 5 pins as I/Os
- Info: Completed User Assigned Global Signal Precondition Operation
- Info: Automatically generated signal ok to use Global clock in Pin A025
- Info: Automatically generated signal ok to use Global clock in Pin A025
- Info: Completed Global Signal Precondition Operation
- Info: Statistics of I/O pins that use the same VCCO and VREF
 - Info: There are 0 I/O pins VREF = unused, VCCO = 3.3V, 2 pins, 0 bidirectional
 - Info: Used I/O standard: LVTTTL
- Info: I/O banks and pins statistics before I/O pin placement
- Info: I/O banks and pins statistics after I/O pin placement
- Info: Statistics of I/O banks
 - Info: I/O bank 1: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 2: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 3: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 4: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 5: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 6: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 7: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 8: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 9: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 10: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 11: VREF = unused, VCCO = unused, used pin 1, available pins 38
 - Info: I/O bank 12: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: Completed I/O Pin Placement Operation
- Info: Quartus II Fitter was successful. 0 errors, 0 warnings
- Info: Writing report file: What if it go

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Example Error Message

Messages

- Info: Running Quartus II Fitter
- Info: Command: quartus_ii -report_settings -fitter-on -report_settings -fitter-off compile_3_0 -fitter -check_pin
- Info: Selected device EPF10K10-10 for design build
- Info: Selected migration device bit is legal with ESD tool of registration pin
- Info: Selected device migration path can use 5 pins as regular I/Os
- Info: Selected device migration path can use 5 pins as I/Os
- Info: Completed User Assigned Global Signal Precondition Operation
- Info: Statistics of I/O pins that use the same VCCO and VREF
- Info: There are 0 I/O pins VREF = unused, VCCO = 3.3V, 2 pins, 0 bidirectional
- Info: Used I/O standard: LVTTTL
- Info: I/O banks and pins statistics before I/O pin placement
- Info: I/O banks and pins statistics after I/O pin placement
- Info: Statistics of I/O banks
- Info: I/O bank 1: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 2: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 3: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 4: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 5: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 6: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 7: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 8: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 9: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 10: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 11: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: I/O bank 12: VREF = unused, VCCO = unused, used pin 1, available pins 38
- Info: Completed I/O Pin Placement Operation
- Info: Quartus II Fitter was successful. 0 errors, 0 warnings
- Info: Writing report file: What if it go

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Using I/O Assignment Analysis

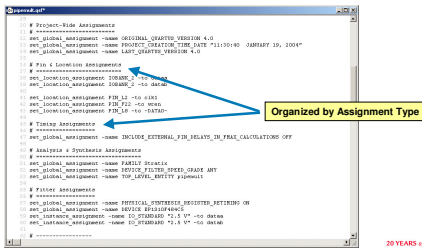
- 1. Use Complete Design Files or Reserve Pins if Incomplete
- 2. Make Pin-Related Assignments
- 3. Start I/O Assignment Analysis
- 4. Review Report File for Errors
- 5. Modify & Correct Illegal Assignments, if Any
- 6. Re-Run Analysis until Errors Are Resolved
- 7. Back-Annotate Pins to Lock Locations

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Quartus Settings File (QSF)

- Stores All Settings & Assignments
- Uses Tcl Syntax



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Design File Management

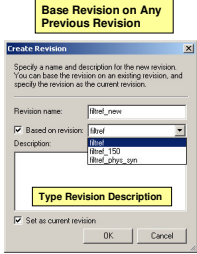
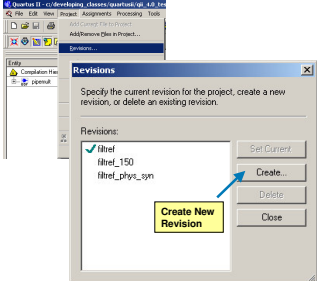
- Project Archive & Restore
 - Stores All Project Files
 - Design Files
 - Settings File
 - Output Files
- Revisions
 - Stores Only QSF
 - Allows Designer to Try Different Options

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Creating a Revision

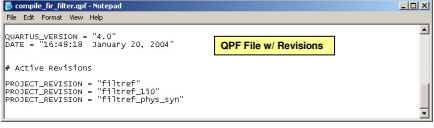
- Project ⇒ Revisions



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Project Revision Support

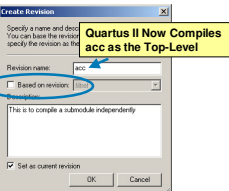
- Active Revision Names Stored in QPF
- QSF Created for Each Revision
 - <Revision_name>.QSF
- Text File Created for Each Revision
 - <Revision_Name>_description.TXT



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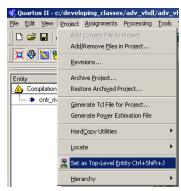
Compiling a Submodule

1. Create a New Revision
2. Disable “Based on revision”



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1. Open Submodule File
2. Select “Set as Top-Level Entity” from Project Menu



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Exercise 2

Please go to Exercise 2 in the Exercise Manual

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Exercise Summary

- Created Project
- Compiled Design
- Gathered Information from the Compilation Report
- Used Assignment Editor to Change Logic Usage
- Used I/O Analysis to Check I/O Placement

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Compilation Summary

- Compiling a Design
 - Compiler Settings
 - Synthesis & Fitting Options
 - Compilation Report
- Assignments
 - Assignment Editor
 - I/O Assignment Analysis
- Managing Revisions

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Designing with Quartus II

Timing Analysis

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Features

- Built-In Static Timing Analysis
- Single & Multi-Clock Timing Analysis
- Standard & Minimum Timing Analysis
- Timing Export for Analysis in Another EDA Tool

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Timing Analysis Agenda

- Single Clock Analysis
- Timing Assignments
 - Global & Individual
- Multi-Clock Analysis
- Multi-Cycle Analysis
- Minimum Timing

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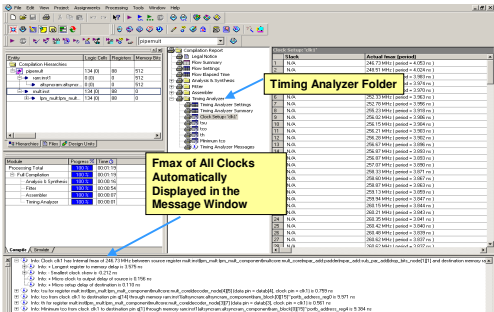
Running Timing Analysis

- Automatically
 - Use Full Compilation
- Manually
 - Processing Menu ⇒ Start ⇒ Start Timing Analysis
 - Tcl Scripts
 - Uses
 - Changing Speed Grade
 - Annotating Netlist with Delay Information

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Timing Analysis

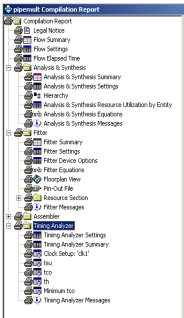


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Reporting Timing Results

- Timing Analyzer Section of Compilation Report
 - Summary
 - Timing Analyses
 - Clock Setup (fmax)
 - Clock Hold
 - tsu (Input Setup Times)
 - th (Input Hold Times)
 - tco (Clock to Out Delays)
 - tpd (Pin to Pin Delays)
 - Minimum tpd & tco

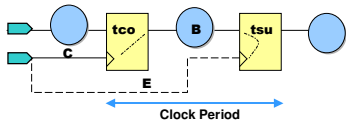


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Clock Setup (fmax)

- Worst-Case Clock Frequency
 - Without Violating Internal Setup & Hold Times



Clock Period = Clock-to-Out + Data Delay + Setup Time - Clock Skew
= $t_{co} + B + t_{su} - (E - C)$

fmax = $1/\text{Clock Period}$

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Clock Setup (fmax) Tables

Worst fmax

Fmax Values Are Listed in Ascending Order; Worst Fmax Is Listed on the Top

Select Clock Setup

Rank	From	To	From Clock	To Clock	Required Setup
1	N/A	231.11 MHz (period = 4.327 ns)	transports_math10...	new_d01_row_d01_end...	ck
2	N/A	231.56 MHz (period = 4.331 ns)	transports_math10...	new_d01_row_d01_end...	ck
3	N/A	232.05 MHz (period = 4.291 ns)	transports_math10...	new_d01_row_d01_end...	ck
4	N/A	232.02 MHz (period = 4.295 ns)	transports_math10...	new_d01_row_d01_end...	ck
5	N/A	232.02 MHz (period = 4.293 ns)	transports_math10...	new_d01_row_d01_end...	ck
6	N/A	232.72 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
7	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
8	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
9	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
10	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
11	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
12	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
13	N/A	242.44 MHz (period = 4.135 ns)	transports_math10...	new_d01_row_d01_end...	ck
14	N/A	242.79 MHz (period = 4.153 ns)	transports_math10...	new_d01_row_d01_end...	ck
15	N/A	241.02 MHz (period = 4.148 ns)	transports_math10...	new_d01_row_d01_end...	ck
16	N/A	241.00 MHz (period = 4.148 ns)	data_vald_mstr-22	columns_d01_row_d01...	ck
17	N/A	241.14 MHz (period = 4.147 ns)	transports_math10...	new_d01_row_d01_end...	ck
18	N/A	241.15 MHz (period = 4.146 ns)	transports_math10...	new_d01_row_d01_end...	ck
19	N/A	241.60 MHz (period = 4.139 ns)	transports_math10...	new_d01_row_d01_end...	ck
20	N/A	242.30 MHz (period = 4.117 ns)	transports_math10...	new_d01_row_d01_end...	ck
21	N/A	242.13 MHz (period = 4.133 ns)	transports_math10...	new_d01_row_d01_end...	ck
22	N/A	243.25 MHz (period = 4.111 ns)	columns_d01_row_d01...	columns_d01_row_d01...	ck

Source, Destination Registers & Associated Fmax Values

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fmax Analysis

- To Analyze the Path More Closely

Highlight, Right-Click Mouse & Select List Paths

Rank	From	To	From Clock	To Clock	Required Setup
1	N/A	231.11 MHz (period = 4.327 ns)	transports_math10...	new_d01_row_d01_end...	ck
2	N/A	231.56 MHz (period = 4.331 ns)	transports_math10...	new_d01_row_d01_end...	ck
3	N/A	232.05 MHz (period = 4.291 ns)	transports_math10...	new_d01_row_d01_end...	ck
4	N/A	232.02 MHz (period = 4.295 ns)	transports_math10...	new_d01_row_d01_end...	ck
5	N/A	232.02 MHz (period = 4.293 ns)	transports_math10...	new_d01_row_d01_end...	ck
6	N/A	232.72 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
7	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
8	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
9	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
10	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
11	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
12	N/A	232.95 MHz (period = 4.189 ns)	transports_math10...	new_d01_row_d01_end...	ck
13	N/A	242.44 MHz (period = 4.135 ns)	transports_math10...	new_d01_row_d01_end...	ck
14	N/A	242.79 MHz (period = 4.153 ns)	transports_math10...	new_d01_row_d01_end...	ck
15	N/A	241.02 MHz (period = 4.148 ns)	transports_math10...	new_d01_row_d01_end...	ck
16	N/A	241.00 MHz (period = 4.148 ns)	data_vald_mstr-22	columns_d01_row_d01...	ck
17	N/A	241.14 MHz (period = 4.147 ns)	transports_math10...	new_d01_row_d01_end...	ck
18	N/A	241.15 MHz (period = 4.146 ns)	transports_math10...	new_d01_row_d01_end...	ck
19	N/A	241.60 MHz (period = 4.139 ns)	transports_math10...	new_d01_row_d01_end...	ck
20	N/A	242.30 MHz (period = 4.117 ns)	transports_math10...	new_d01_row_d01_end...	ck
21	N/A	242.13 MHz (period = 4.133 ns)	transports_math10...	new_d01_row_d01_end...	ck
22	N/A	243.25 MHz (period = 4.111 ns)	columns_d01_row_d01...	columns_d01_row_d01...	ck

Similar Steps for All Timing Path Analysis in Quartus II

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fmax Analysis Details

Data Delay (B)

Destination Register Clock Delay (E)

Source Register Clock Delay (C)

Clock to Output (tco)

Messages Window (System Tab) in Quartus II

Info: Clock clk has internal fmax of 231.11 MHz between source register transpose_matrix2p_mbr_in0[0]m_count

Info: Longest register to register delay is 4.135 ns

Info: Smallest clock skew is 0.000 ns

Info: Shortest clock path from clock clk to destination register is 2.548 ns

Info: Longest clock path from clock clk to source register is 2.548 ns

Info: Micro clock to output delay of source is 0.099 ns

Info: Micro setup delay of destination is 0.093 ns

Setup Time (tsu)

Clock Period

$0.099\text{ ns} + 4.135\text{ ns} + 0.093\text{ ns} - 0.000\text{ ns} = 231.11\text{ MHz}$

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fmax Analysis Details (cont.)

Node Fan-Out

Interconnect Delay

Cell Delay

Running Total

Destination Cell Name & Type

% Interconnect vs. % Cell Delay

This signal path consists of 28 locations

Notes:

- 1) This Timing Convention Is Similar for All Timing Path Analysis
- 2) Carry Chain Delay Is Included in Cell Delay Number

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Locate Delay Path in Floorplan

Message Window

Info: Longest register to register delay is 4.135 ns

Info: Shortest clock path from clock clk to destination register is 2.548 ns

Info: Longest clock path from clock clk to source register is 2.548 ns

Info: Micro clock to output delay of source is 0.099 ns

Info: Micro setup delay of destination is 0.093 ns

Right-Click & Select Locate

Compilation Report

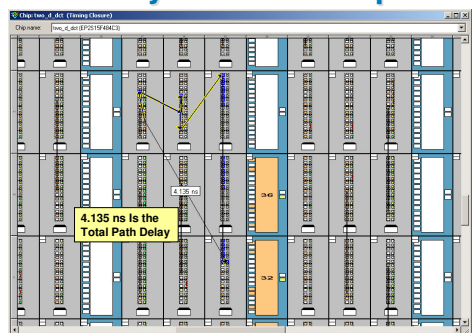
Path	Delay	Location	Component	Delay	Location	Component
clk to destination register	2.548 ns	clk to destination register	clk to destination register	2.548 ns	clk to destination register	clk to destination register
clk to source register	2.548 ns	clk to source register	clk to source register	2.548 ns	clk to source register	clk to source register
micro clock to output delay of source	0.099 ns	micro clock to output delay of source	micro clock to output delay of source	0.099 ns	micro clock to output delay of source	micro clock to output delay of source
micro setup delay of destination	0.093 ns	micro setup delay of destination	micro setup delay of destination	0.093 ns	micro setup delay of destination	micro setup delay of destination

Notes:

- 1) Use Similar Procedure for All Timing Path Analysis

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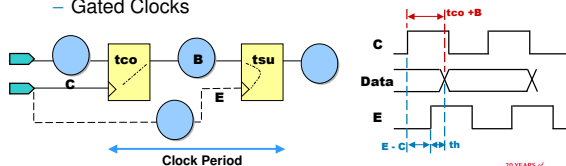
Locate Delay Path in Floorplan

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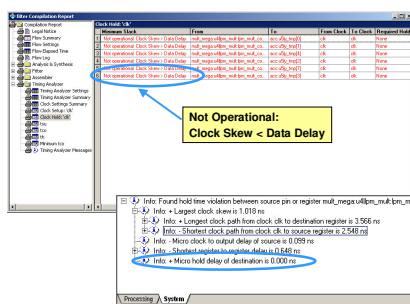
Clock Hold Analysis

- Checks Internal Register-Register Timing
 - Report Occurs Only When Hold Violations Occur
- Results Usually When Data Delay (B) is Greater than Clock Skew (E-C)
 - Non-Global Clock Routing
 - Gated Clocks



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Hold Time Violations Table



Discover Internal Hold Time Issues before Simulation

Not Operational:
Clock Skew < Data Delay

- Info - Found hold time violation between source pin or register multi_mega_uart_tx_pin_mcu_component1alt31external_data
- Info - Largest clock skew is 1.018 ns
- Info - Longest clock path from clock clk to destination register is 3.566 ns
- Info - Shortest clock path from clock clk to source register is 2.548 ns
- Info - Micro clock to output delay of source is 0.099 ns
- Info - Shortest register to register delay is 0.648 ns
- Info - Micro hold delay of destination is 0.000 ns

List Paths Window

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I/O Setup Time Analysis (tsu)

$$tsu = \text{data delay} - \text{clock delay} + \text{intrinsic tsu}$$

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I/O Hold Time Analysis (th)

$$th = \text{clock delay} - \text{data delay} + \text{intrinsic thold}$$

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I/O Clock-to-Output Analysis (tco)

$$\text{clock delay} + \text{intrinsic tco} + \text{data delay} = tco$$

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I/O Timing Analyzer

tsu, tco, th Will All Show up in the Timing Analyzer Report

No	Slack	Required tns	Actual tns	From	To	To Clock
1	N/A	None	2.702 ns	lapin[0]	lapin[0]	clk
2	N/A	None	2.564 ns	lapin[0]	lapin[0]	clk
3	N/A	None	2.648 ns	lapin[0]	lapin[0]	clk
4	N/A	None	2.642 ns	lapin[0]	lapin[0]	clk
5	N/A	None	2.597 ns	lapin[0]	lapin[0]	clk
6	N/A	None	2.573 ns	lapin[0]	lapin[0]	clk
7	N/A	None	2.548 ns	lapin[0]	lapin[0]	clk
8	N/A	None	2.521 ns	lapin[0]	lapin[0]	clk
9	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
10	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
11	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
12	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
13	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
14	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
15	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
16	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
17	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
18	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
19	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
20	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
21	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk
22	N/A	None	0.950 ns	lapin[0]	lapin[0]	clk

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Note: Timing Analysis of tpd is similar

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Timing Analysis Options

- Used to Limit which Paths Are Displayed
- Global Cut Timing Options (On by Default)
 - Cut Paths between Unrelated Clock Domains
 - Cut Off Feedback from I/O Pins (Next Slide)
 - Cut Off Clear & Preset Signal Paths
 - Cut Off Read during Write Signal Paths
- Timing Analyzer Options
 - Display Paths that Do Not Meet Timing Only

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Cut Off Feedback from I/O Pin

- Breaks Bidirectional I/O Pin from Analysis
- When On, Paths A & B Are Valid; C Is Not
- When Off, Paths A, B, & C Are Valid

- Performed Automatically during Each Compile
- Detects Clocks Automatically If No Assignments Are Made
 - Single or Multiple Asynchronous Clock Domains
 - Still Important to Specify Clock Frequencies
- Displays Results in the Timing Analyzer Report

- Performed Automatically during Each Compile
- Detects Clocks Automatically If No Assignments Are Made
 - Single or Multiple Asynchronous Clock Domains
 - Still Important to Specify Clock Frequencies
- Displays Results in the Timing Analyzer Report

Exercise 3

Please go to Exercise 3 in the Exercise Manual

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Exercise Summary

- Single Clock Timing Analysis
- List Timing Paths & View Details
 - Locate in Floorplan

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Timing Assignments

- **VERY IMPORTANT!!**
- Have a Major Impact on Design Compilation
 - Specify **ALL** Timing Requirements for Your Design
 - Fitter Works Hardest on the Worst Timing
 - Timing Will Be Reported in Red If Not Met
- Types
 - Internal & I/O Timing
 - Maximum & Minimum
- Can Be Assigned Globally or Individually
 - Individual Assignments Better

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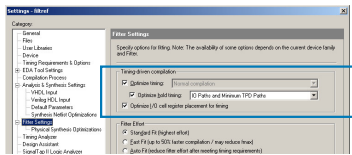
INNOVATION



Timing Driven Compilation (TDC)

- Directs Fitter to Place & Route Logic to Meet Timing Assignments
 - Optimize Timing
 - Placing Nodes in Critical Paths Closer Together
 - Optimize I/O Cell Register Placement
 - Moving Registers into I/O Cells

Assignments →
Settings →
Fitting Settings



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Optimize Hold Timing

- Modifies Place & Route to Meet Hold or Minimum Timing Requirements
 - May Add Additional Routing in Path
 - Supported in Stratix II, Stratix, Stratix GX, Cyclone Devices

Settings

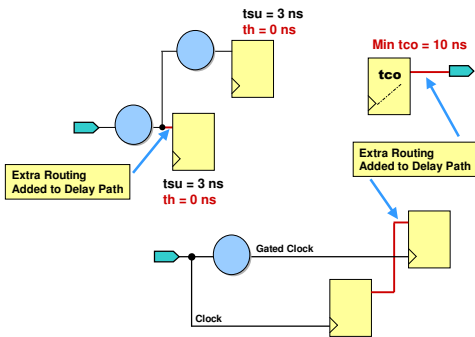
- Any I/O Paths
- All Paths (I/O & Internal)



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Optimize Hold Time Examples



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Global Clock Assignments

Assignments ⇒ Settings ⇒ Timing Requirements & Options

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Asynchronous Global Clocks

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Global Maximum I/O Delay

Assignments ⇒ Settings ⇒ Timing Requirements & Options

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Global Minimum I/O Delay

Assignments => Settings => Timing Requirements & Options

Global t_{th}
All Inputs or Bidirectional Pins Driving Registers Must Have a t_{th} Less Than This Value

Global Minimum t_{co}
All Registers Driving Outputs or Bidirectional Pins Must Have a t_{co} Greater Than This Value

Global Minimum t_{od}
All Direct Pin-to-Pin Path Delays Must Be Greater Than This Value

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Slack Calculations

- Timing Margin Comparing Actual Timing to Timing Requirements
- Appear Only When Timing Assignments Are Made

Slack = Required Time – Actual Time

Positive Slack

- Timing Requirement Met (**BLACK**)

Negative Slack

- Timing Requirement Not Met (**RED**)

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Global Timing Assignments Examples

Clock Setup: 'clk1'

Rank	Actual fmax (period)	From	To	From Clock	To Clock	Required Setup Relationship
1	1.165 ns	304.57 MHz period = 3.279 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	4.444 ns
2	1.205 ns	306.74 MHz period = 3.233 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	4.444 ns
3	1.215 ns	308.63 MHz period = 3.223 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	
4	1.247 ns	312.79 MHz period = 3.191 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	
5	1.253 ns	313.38 MHz period = 3.178 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	
6	1.265 ns	314.65 MHz period = 3.178 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	
7	1.293 ns	317.36 MHz period = 3.151 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	
8	1.300 ns	318.07 MHz period = 3.144 ns multiinst0pin_mult...	raminst02ahy...	clk1	clk1	4.444 ns

fmax Timing Assignment Values Are BLACK, Because Actual fmax Exceeds the Required fmax

t_{su} timing assignment Values Are RED, Because Actual t_{su} Falls below Required t_{su}

Rank	Required t _{su}	Actual t _{su}	From	To	To Clock
71	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
72	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
73	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
74	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
75	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
76	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
77	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
78	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
79	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
80	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
81	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	
82	0.200 ns	0.200 ns	data05[multiinst0pin_mult_pin_compound0_0]_clk1	data05[multiinst0pin_mult_pin_compound0_0]_clk1	

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Individual Timing Assignments

- Available Settings
 - tsu (Max)
 - th (Max)
 - tco (Max & Min)
 - tpd (Max & Min)
 - Pin-to-Pin
 - Point-to-Point (I/O→Reg; Reg→Reg; Reg→I/O)
- Available Assignment Types
 - Single-Point
 - Point-to-Point
 - Wildcard (* or ?)

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Individual Assignment Targets

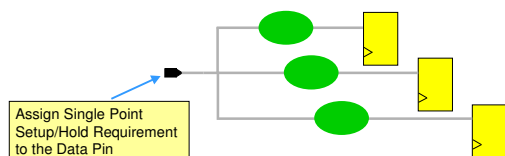
- Registers (all)
- Clock Pins (tsu, tco, th)
- Input Pins (tsu, th, tpd)
- Output Pins (tco, tpd)
- Bi-Directional Pins (all)

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Single-Point tsu/th

- Setup/Hold Timing Required on Every Register Fed by Pin



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Point-to-Point tsu/th

- Setup/Hold Timing Required Only on the Specified Path

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Single-Point tco

- Clock-to-Out Timing Required on All tco Paths Starting from the Specified Clock

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Single-Point tco (cont.)

- Clock-to-Out Timing Required on All Paths from Any Clock to Specified Output Pin

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Point-to-Point tco

- Clock-to-Out Timing Required Only on the Specified Path

Assign Point-to-Point Clock-to-Out Requirement to Source Register or Clock Pin & Output Pin

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Wildcard Assignment

- Indicates All Targets with a Character or String
 - '*' - Zero or More Characters
 - '?' - Single Character

Point-to-Point Setup Using Wildcard:
Assign Setup Requirement from "data" to "Rg*" or "Rg?"

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Ex. Assigning Setup Requirement

Assignment Editor Is Used for All Individual Timing Requirements

Select Timing Category

Use Source Name (From) to Create a Point-to-Point Requirement

Enter the Target or Destination Node Name

Choose tsu Requirement from the Drop-down List & Enter the Value

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External Delay Assignments

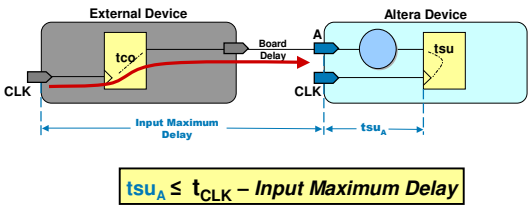
- Specify System-Level Timing Constraints
- Constrain I/O Timing
 - Same as tsu, th, tco & Minimum tco
- Include I/O Timing as Part of Clock Timing Analysis Report
 - Clock Setup(fmax)
 - Clock Hold
- Settings
 - Input Minimum/Maximum Delay
 - Output Minimum/Maximum Delay

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Input Maximum Delay

- Maximum Delay from External Device to Altera I/O
 - Represents External Device tco + Board Delay
- Constrains Input Pin tsu

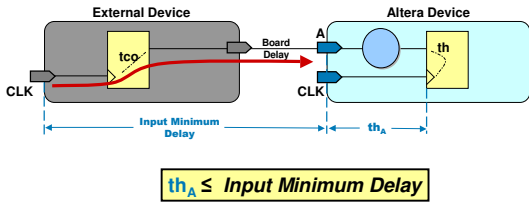


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Input Minimum Delay

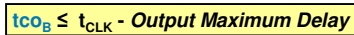
- Minimum Delay from External Device to Altera I/O
 - Represents External Device tco + Board Delay
- Constrains Input Pin th



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- Maximum Delay from Altera I/O to External Device
 - Represents External Device t_{su} + Board Delay
- Constrains Output Pin t_{co}



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- Minimum Delay from Altera I/O to External Device
 - Represents External Device t_h - Board Delay
- Constrains Output Pin Minimum t_{co}

[illegible]

- Info: Slack time is 219 ns for clock, clk, between source pin (Q5) and destination register taps, m01n01 (Q1)
- Info: Finis = 264.48 ns [period= 3.781 ns]
- Info: Largest pin to register requirement is 2.450 ns
- Info: Setup relationship between source and destination is 4.000 ns
- Info: Shortest clock path from clock, clk, to destination register is 2.543 ns
- Info: Micro setup delay of destination is 0.093 ns
- Info: Max input delay of pin is 4.0 ns
- Info: Longest pin to register delay is 2.231 ns

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Clock Setup/Hold (I/O Paths)

- External (System-Level) I/O Timing Reported Separately in Timing Analyzer
 - Option Found in **Assignments** ⇒ **Settings** ⇒ **Timing Requirements & Options**

Item	Setup (ns)	Hold (ns)	From	To	From Clock	To Clock	Reported Setup (ns)
1	0.750 ns	0.400 ns	input[0]	output[0]	clk	clk	4.000 ns
2	0.750 ns	0.400 ns	input[1]	output[1]	clk	clk	4.000 ns
3	0.750 ns	0.400 ns	input[2]	output[2]	clk	clk	4.000 ns
4	0.750 ns	0.400 ns	input[3]	output[3]	clk	clk	4.000 ns
5	0.750 ns	0.400 ns	input[4]	output[4]	clk	clk	4.000 ns
6	0.750 ns	0.400 ns	input[5]	output[5]	clk	clk	4.000 ns
7	0.750 ns	0.400 ns	input[6]	output[6]	clk	clk	4.000 ns
8	0.750 ns	0.400 ns	input[7]	output[7]	clk	clk	4.000 ns
9	0.750 ns	0.400 ns	input[8]	output[8]	clk	clk	4.000 ns
10	0.750 ns	0.400 ns	input[9]	output[9]	clk	clk	4.000 ns
11	0.750 ns	0.400 ns	input[10]	output[10]	clk	clk	4.000 ns
12	0.750 ns	0.400 ns	input[11]	output[11]	clk	clk	4.000 ns
13	0.750 ns	0.400 ns	input[12]	output[12]	clk	clk	4.000 ns
14	0.750 ns	0.400 ns	input[13]	output[13]	clk	clk	4.000 ns
15	0.750 ns	0.400 ns	input[14]	output[14]	clk	clk	4.000 ns
16	0.750 ns	0.400 ns	input[15]	output[15]	clk	clk	4.000 ns
17	0.750 ns	0.400 ns	input[16]	output[16]	clk	clk	4.000 ns
18	0.750 ns	0.400 ns	input[17]	output[17]	clk	clk	4.000 ns
19	0.750 ns	0.400 ns	input[18]	output[18]	clk	clk	4.000 ns
20	0.750 ns	0.400 ns	input[19]	output[19]	clk	clk	4.000 ns



Other Individual Timing Assignments

- Cut Timing Path
 - Removes Paths from TDC & Timing Analysis
 - Ex. Test Logic
- Not a Clock
 - Disables Clock Identification
 - Ex. Gate Inputs to Gated Clocks
- Inverted Clock
 - Marks Inverted Clocks Generated with Complex Logic



Report Delay Assignment

Item	Actual Delay (ns)	Reported Delay (ns)	From	To
1	4.000 ns	4.000 ns	input[0]	output[0]
2	4.000 ns	4.000 ns	input[1]	output[1]
3	4.000 ns	4.000 ns	input[2]	output[2]
4	4.000 ns	4.000 ns	input[3]	output[3]
5	4.000 ns	4.000 ns	input[4]	output[4]
6	4.000 ns	4.000 ns	input[5]	output[5]
7	4.000 ns	4.000 ns	input[6]	output[6]
8	4.000 ns	4.000 ns	input[7]	output[7]
9	4.000 ns	4.000 ns	input[8]	output[8]
10	4.000 ns	4.000 ns	input[9]	output[9]
11	4.000 ns	4.000 ns	input[10]	output[10]
12	4.000 ns	4.000 ns	input[11]	output[11]
13	4.000 ns	4.000 ns	input[12]	output[12]
14	4.000 ns	4.000 ns	input[13]	output[13]
15	4.000 ns	4.000 ns	input[14]	output[14]
16	4.000 ns	4.000 ns	input[15]	output[15]
17	4.000 ns	4.000 ns	input[16]	output[16]
18	4.000 ns	4.000 ns	input[17]	output[17]
19	4.000 ns	4.000 ns	input[18]	output[18]
20	4.000 ns	4.000 ns	input[19]	output[19]

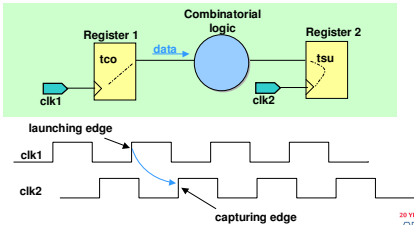
Assign Nodes in Assignment Editor
& Re-Run Timing Analysis Only

- Reports Delay between Selected Nodes
 - Pin-Register
 - Register-Register
 - Register-Pin
- Reports Results in Custom Delay Section of Timing Analyzer



Multi-Clock Frequency Analysis

- Analyzes Timing on Register-to-Register Paths Controlled by Different Synchronous Clocks
 - Individual Clocks Treated as Same Frequency & Phase Unless Specified

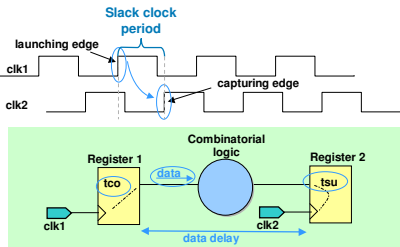


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Slack Equations for Multi-Clock

Slack = Required Time - Actual Time
Slack = Slack Clock Period - (tco + Data Delay + tsu)



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Steps for Multi-Clock Analysis

- 1) Create Clock Settings & Assign to Clock Node
 - Define a Base Clock
 - Define Clock(s) Relative to the Base Clock
- 2) Recompile or Restart Timing Analysis
- 3) Examine Results in Timing Analyzer Report

Note: May Also Use Timing Wizard

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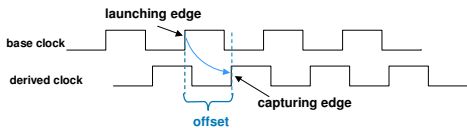


1) Create Clock Settings

- Set Clock Relationships
 - Assign Base Clock
 - Assign Derived Clock(s) Referenced to Base

$$\text{derived clock} = \text{base clock} \times (\text{ratio}) + \text{offset}$$

Note: Multiple Base & Derived Clocks Allowed



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Base Clocks

Timing Requirements & Options

Assignments ⇒ Settings ⇒ Timing Settings...

Click New to Add New Setting

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Base Clocks (cont.)

Enter Name of Clock Node

Enter Name of Clock Setting

Select Independent of Other Clock Settings

Adjust fmax & Duty Cycle

Click OK to Add Setting

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Derived Clocks

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Click New to Add New Setting

Enter Name of Derived Clock Setting

Enter Name of Derived Clock Node

Select Clock Setting on which This Derived Clock is Based

Click on Derived Clock Requirements

Derived Clocks (cont.)

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Adjust Base Ratio, Duty Cycle, Offset & Inversion Settings

Click OK to Add Setting

3) Examine Timing Analyzer Report

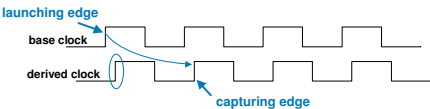
- Positive Slack - Timing Was Met (BLACK)
- Negative Slack - By How Much Timing Was Not Met (RED)
- Must Alter Design or Use Timing Assignments (Multi-Cycle) to Resolve Negative Slack

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Timing Analyzer Report

Multi-Cycle Paths

- Intentionally Require More Than One Clock Cycle to Become Stable
 - Must Be Considered in Design Implementation
 - Must Tell Timing Analyzer to Account for Multiple Clock Edges in Clock Setup Calculation



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Assigning Multi-Cycle Paths

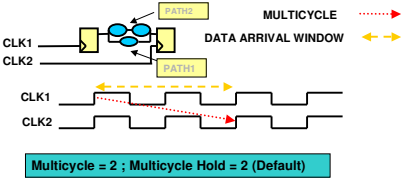
- Destination/Source Register
 - Applies to All Paths Leading from/to Register
- Register-to-Register
 - Applies to All Paths between One Source & One Destination Register
- Two Clock Domains
 - Applies to All Signals Traveling between Clock Domains
- Register Clock Enables
 - Applies to All Registers Controlled by Clock Enable

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Multi-Cycle Assignment

- Maximum Point-to-Point Timing
 - Data Cannot Arrive after Number of Cycles
 - Ex: One Path Is < 1 Cycle, Other Path Is > 1 Cycle
 - Circuit Requires Enables for Proper Operation



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Multi-Cycle Hold Assignment

- **Minimum Point-to-Point Timing**
 - Data Must Arrive after Hold Time
 - Used in Conjunction with a Multi-cycle Assignment

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Clock Enable Multi-Cycle Assignments

- Assigns Multi-Cycle to Source of Clock Enable
 - I/O Pin
 - Register
- Settings
 - Clock Enable Multicycle (Maximum)
 - Clock Enable Multicycle Hold (Minimum)

Source Multi-Cycle Assignments

- Used When Source Clock is Higher Frequency
- Settings
 - Source Multicycle & Multicycle Hold
 - Source Clock Enable Multicycle & Multicycle Hold

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Ex. Assigning a Multi-Cycle

Assignments ⇒ Assignment Editor...

1) Choose Timing Category

2) Enter Destination Node

3) Choose Multicycle

4) Specify Number of Edges

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Minimum Timing Analysis

- Reports Best-Case I/O Results
 - Minimum tco
 - th
 - Minimum tpd
- Uses Fastest Timing Model
 - Fastest Process
 - Highest Voltage
 - Lowest Temperature

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Running Minimum Timing Analysis

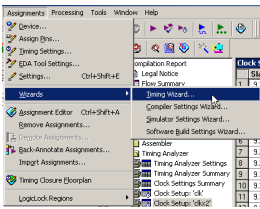
- Processing ⇒ Start ⇒ Start Minimum Timing Analysis
- Must Re-Run Standard Timing Analysis Afterwards
 - Netlist Annotated with Minimum Values
 - Previous Standard Analysis Overwritten

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Timing Wizard

- Easy Way to Enter Timing Assignments
- Consolidates Timing Settings into One Menu
 - Individual Clock Settings OR Overall Circuit Frequency
 - Default System Timing
 - Default External Input/Output Delays
 - Enable/Disable Timing Analysis during Compilation
 - TDC



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Exercise 4

*Please go to Exercise 4 in the
Exercise Manual*

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Exercise Summary

- Multi-Clock Timing Analysis
 - Slack Analysis
- Used Timing Wizard to Define Clocks
- Making Multi-Cycle Timing Assignments
 - Used the Node Finder

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Timing Analysis Summary

- Single-Clock Timing Analysis
- Timing Assignments
- Multi-Clock Timing Analysis
- Multi-Cycle Timing Assignments
- Minimum Timing Analysis

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More Timing Analysis Info

- Quartus II Handbook: Using Quartus II Timing Analysis

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Designing with Quartus II

Simulation

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 **QUARTUS II**

Quartus II Simulation

- Simulator Method & Features Overview
- Simulator Settings
- VWF File Creation
- Simulation Output
- 3rd Party Simulation

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Supported Simulation Methods

- Quartus II
 - VWF (Vector Waveform File)
 - Primary Graphical Waveform File
 - VEC (Vector File)
 - Text-Based Input File
 - SCF (Simulator Channel File)
 - MAX+PLUS II Graphical Waveform File
 - TBL (Table File)
 - Text-Based Output File from Quartus II or MAX+PLUS II
 - Tcl/TK Scripting
- 3rd Party Simulators
 - Verilog/VHDL Testbench

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Simulator Features

- Supports 9 Signal Values
 - 1 Forcing '1'
 - 0 Forcing '0'
 - XForcing Unknown
 - U Uninitialized
 - ZHigh Impedance
 - H Weak '1'
 - L Weak '0'
 - W Weak Unknown
 - DC Don't Care

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Simulator Features (cont.)

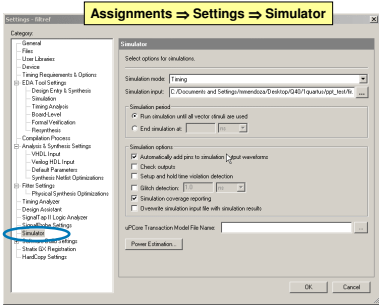
- Performs PowerGauge™ Analysis
- Converts VWF into HDL Testbench
- Generates HDL Testbench Template
- Supports Breakpoints
 - Adding Output Pins to Output Waveform File
 - Checking Outputs at End of Simulation

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Simulator Settings

- Mode
- Input File
- Period
- Options

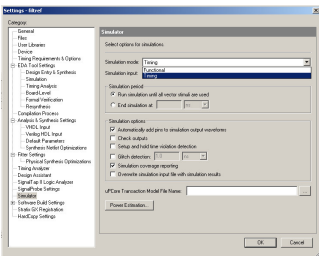


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Simulator Mode

- Functional*
 - Type: RTL
 - Uses Pre-Synthesis Netlist
- Timing
 - Type: Gate-Level or Post-Place & Route
 - Uses Fully Compiled Netlist



* Must Generate Functional Simulation Netlist (Processing Menu) before Performing Functional Simulation

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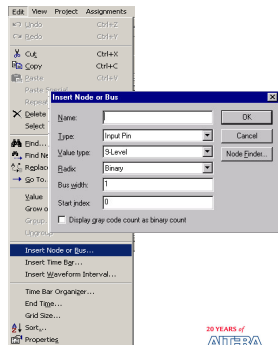


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Insert Nodes

- Select **Insert Node or Bus** (Edit Menu)
 - VWF Must Be Open
 - Use Node Finder

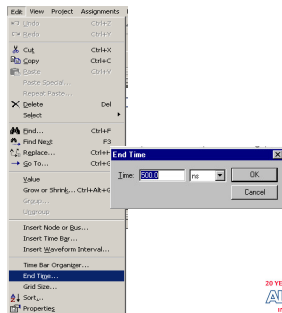


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Specify End Time

- Maximum Length of Simulation Time
 - Edit Menu



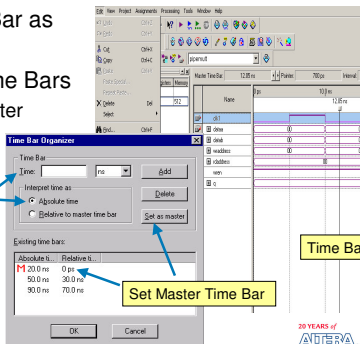
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Insert Time Bars

- Set One Time Bar as Master
- Insert Other Time Bars
 - Relative to Master
 - Absolute

Specify Time Bar

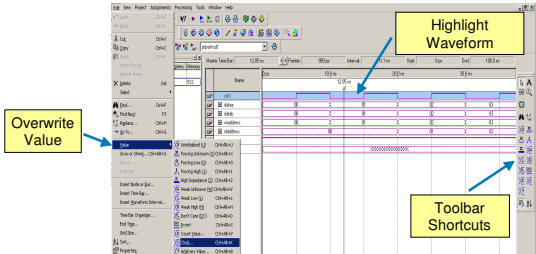


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Draw Stimulus Waveform

- Highlight Portion of Waveform to Change
- Overwrite Value with Desired Value

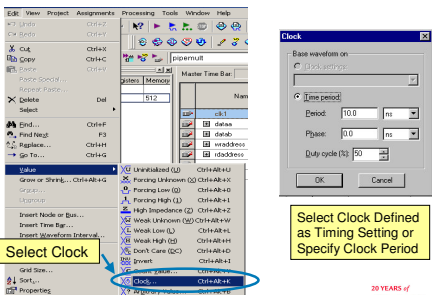


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Create Clock

- Highlight Waveform & Enter Period

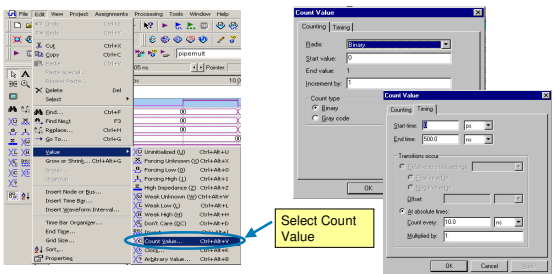


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Creating Counting Pattern

- Highlight Waveform & Enter Pattern

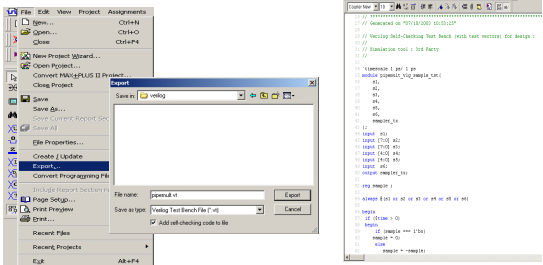


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Waveform to Testbench Generator

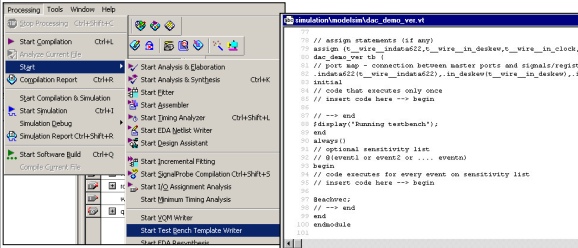
- Converts VWF into HDL Testbench



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Testbench Template Generator

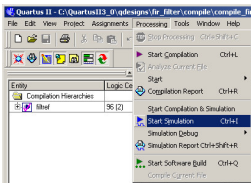
- Generates HDL Testbench Template
- User Inserts Test Stimulus



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Starting Simulation

- Processing Menu ⇒ Start Simulation



- Scripting

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Using Message Window to Debug

1
Double clicking on message

2
Highlights signal with unexpected value

3
Creates time bar at occurrence of unexpected value

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Breakpoints

- Interrupts Simulation at Specified Points
- Consists of 2 Parts
 - Equation (Condition)
 - Action
 - Stop
 - Give Error
 - Give Warning
 - Give Info

Processing ⇒
Simulation Debug ⇒
Breakpoints

Click on condition
to Build Equation

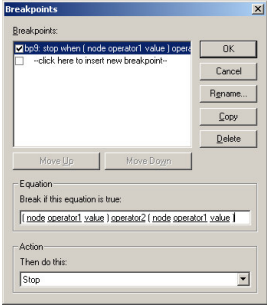
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Breakpoint Conditions

- <Node> <Operator1> <Value>
 - Single Condition
 - Ex. ena = 1
- Time = <Value>
 - Single Condition
 - time = 500ns
- <Condition> <Operator2> <Condition>
 - Complex Tests
 - ena = 1 && time > 500ns

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Breakpoint Equations (cont.)

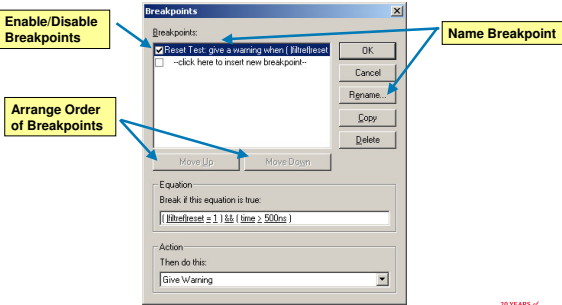


- Node
 - Opens Node Finder
- Operator1
 - <, >, =
- Operator2
 - && (AND)
 - || (OR)

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Example Breakpoint



Enable/Disable Breakpoints

Arrange Order of Breakpoints

Name Breakpoint

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PowerGauge Analysis Software

- Estimates Power Consumption Based on Toggle Rates
 - Derives Toggles Rate from Simulation Stimulus
 - Uses Quartus II Simulator
- Supports Multiple I/O Standards
- Supports Stratix, Stratix GX, Cyclone MAX 7000AE, MAX 7000B, MAX 3000 Families
- 3rd Party Simulation Tools Output PWF File that Can Be Read by Quartus II Simulator

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Designing with Quartus II

Power Analysis

1) Select Power Estimation

2) Enter Simulation Period

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Power Analysis (cont.)

3) After Simulation, Select "Simulator Summary"

4) View Results Based on Stimulus Toggle Rate

Type	Value
1 Simulation Start Time	0 ps
2 Simulation End Time	700.0 ns
3 Simulation Netlist Size	152 nodes
4 Simulation Coverage	53.77 %
5 Total Number of Transitions	2793
6 Power estimation start time	0 ps
7 Power estimation end time	700.0 ns
8 Total Internal Power	68.12 mW
9 Total Standby Internal Power	50.39 mW
10 Total Logic Element Internal Power	6.81 mW
11 Total Clockless Internal Power	3.12 mW
12 Total IO Power	20.72 mW
13 Total IO Buffer Power	20.72 mW
14 Total Power	88.85 mW

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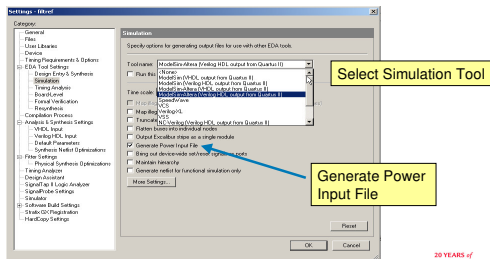
Using 3rd Party Simulators

- Mentor Graphics
 - ModelSim
- Cadence
 - VERILOG-XL
 - NC-Verilog
 - NC-VHDL
- Synopsys
 - VCS
 - VSS
 - Scirocco

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Specify Simulator

- Select EDA Tools Settings
 - Assignments Menu



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3rd Party Simulation Files

- Functional Simulation
 - Use 220models & altera_mf Megafunction Model Files
- VHDL Timing Simulation
 - Use Quartus II-Generated VHO & SDO Files
 - Use <device_name>_ATOMS.VHD & <device_name>_ATOMS_COMPONENTS.VHD Files
 - Located in eda\sim_lib Directory
- Verilog Timing Simulation
 - Use Quartus II-Generated VO & SDO Files
 - Use <device_name>_ATOMS.VO File
 - Located in eda\sim_lib Directory

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Exercise 5

Please go to Exercise 5 in the
Exercise Manual

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Exercise Summary

- Learn about Quartus II Simulator
- Draw Signals in VWF Files
- Functional Simulation
 - View Simulation Results

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Simulation Summary

- Functional & Timing Simulation
- Creating a Vector Waveform File
- Power Analysis

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Designing with Quartus II

Programming/Configuration

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A-MNL-QUARTUSII-09 v4.0

Programming/Configuration

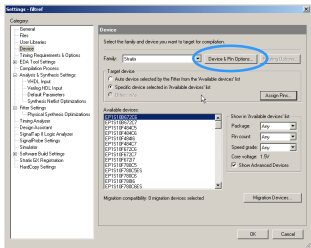
- Setting Device Options
- Assembler Module
- Programmer & Chain Description File
 - Programming Directly with Quartus II
- File Conversion
 - Creating Multi-Device Programming Files

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Setting Device Options

- Assignments ⇒ Device ⇒ Device & Pin Options Button

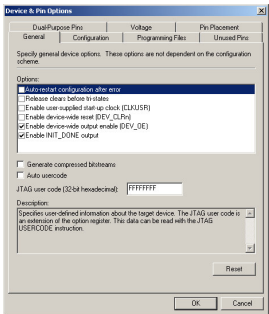


Device Options Control
Configuration &
Initialization of Device

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General Tab

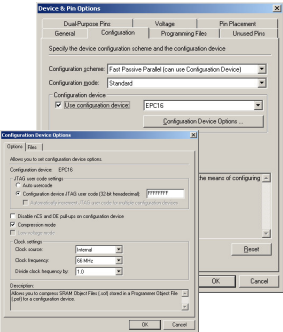


- Device Options Not Dependent on Configuration Scheme
 - Enable Device-Wide Clear
 - Enable Device-Wide Output Enable
 - Enable Initialization Done Output Pin

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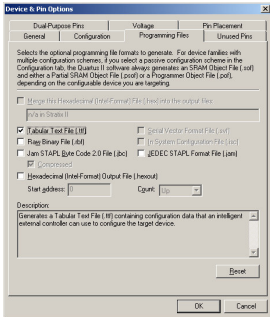
Configuration Tab



- Choose Device Configuration Mode & Available Options
 - Generates Correct Configuration & Programming Files Every Compilation
- Enables Special Features of Configuration Devices
 - Enable Programming File Compression
 - Set Configuration Clock Frequency

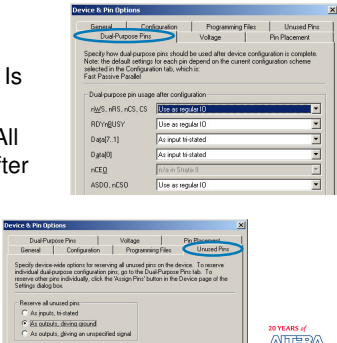
Programming Files Tab

- Output Files Always Created
 - POF (Programming Object File)
 - SOF (SRAM Object File)
- Other Selectable Output Files
 - JAM (JEDEC STAPL)
 - JBC (JAM Byte-Code)
 - RBF (Raw Binary File)
 - HEXOUT (Intel Hex Format)



Unused & Dual-Purpose Pins Tabs

- Selects Usage of Dual-Purpose Pins after Configuration Is Complete
- Indicates State of All Unused I/O Pins after Configuration Is Complete



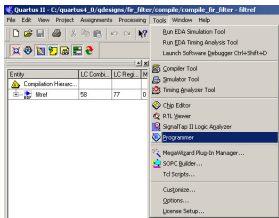
Quartus II Assembler Module

- Generates All Configuration/Programming Files
 - As Selected in Device & Pin Options Dialog Box
- Ways to Run Assembler
 - Full Compilation
 - Execute Assembler Individually
 - Processing Menu => Start => Start Assembler
 - Generates Files without Full Compilation
 - Switching Configuration Devices
 - Enabling/Disabling Configuration Device Feature
 - Scripting

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Open Programmer



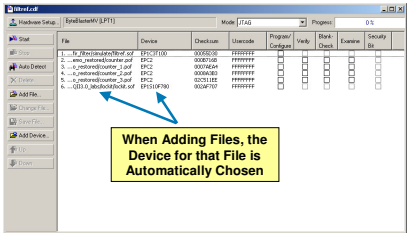
- Enables Device Programming
 - ByteBlaster™ II or ByteBlasterMV™ Cables
 - USB-Blaster
 - MasterBlaster™ Cable
 - APU (Altera Programming Unit)
- Opens Chain Description File (.CDF)
 - Stores Device Programming Chain Information

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CDF File

- Lists Devices & Files for Programming or Configuration
- Programs/Configures in Top-to-Bottom Order



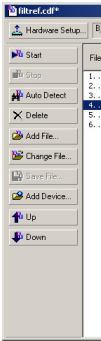
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Programmer Toolbar

- Start Programming
- Auto Detect Devices in JTAG Chain
- Add/Remove/Change Devices in Chain
- Add/Remove/Changes Files in Chain
- Change Order of Files in Chain
- Setup Programming Hardware

Note: All Options are available the Edit Menu except Start Programming & Auto Detect which are available in the Processing Menu

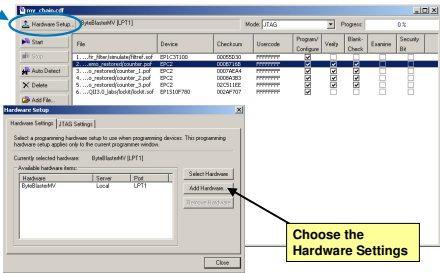


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Setting up Programming Hardware

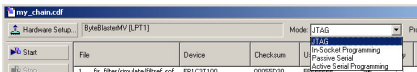
Click on the Hardware Setup Button



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Chain Programming Modes



- Altera FPGAs, CPLDs & Non-Altera Devices
 - JTAG
- Altera FPGAs Only
 - Passive Serial
 - Active Serial
- CPLDs & Configuration Devices in APU
 - In-Socket

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Exercise 6 or 7 (Optional)

Please go to Exercise 6 or 7 in the Exercise Manual

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Programming/Configuration Summary

- Setting Device Options
- Generating Programming Files
- Programming Device or Devices in Chain
- Converting Programming Files

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Class Summary

- Design Entry Techniques
- Project Creation
- Compiler Settings & Assignment Editor
- Timing Analysis
- Simulation
- Programming/Configuration

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 - Chip Editor
 - FPGA Optimization
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- Field Applications Engineers: Contact Your Local Altera Sales Office
- Receive Literature by Mail: (888) 3-ALTERA
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