Introduction to VHDL

Course Length: 1 Day

Course Description

This one-day class is a general introduction to the VHDL language and its use in programmable logic design. The emphasis is on the synthesis constructs of VHDL; however, you will also learn about the simulation constructs. You will gain a basic understanding of VHDL to enable you to begin creating your design file. In the hands-on laboratory sessions, you will put this knowledge to the test by writing simple but practical designs. You will also learn the basic instructions needed for operating both the synthesis and simulation tools of the Quartus II software.

Skills Required

The following skills are strongly recommended:

- Background in digital logic design
- Knowledge of simulation is a plus
- Prior knowledge of a programming language (e.g., "C" language) is a plus

No prior knowledge of VHDL or Quartus II software is needed.

Skills Developed

The skills developed in the course include:

- Understanding the origin of the VHDL language
- Understanding the language basics
- Using VHDL building blocks (Design Units)
    - Entity
    - Architecture
    - Configurations
    - Package declarations
    - Package bodies
- Ability to model code styles
    - Behavioral code style
    - Structural code style
- Understanding the design methodologies of VHDL and the differences in
    - Simulation models
    - Synthesis models