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IAALACW & LASCAS & IBERCHIP PROGRAM

Day 1 – Sunday 28th February 2016

	AGATA ROOM	TOPAZIO ROOM	ESMERALDA ROOM	DIAMANTE ROOM	HALL
13:00 14:00					Registration
14:00 15:30	Tutorial 1A: Prof. Dario Hermida European Space Agency	Tutorial 1T: Prof. Alfredo Arnaud		IEEE CAS Chapter Chairs Meeting	
15:30 16:00					COFFE BREAK
16:00 17:30	Tutorial 2A: Prof. Thais Russomano Biomedical Research in Space	Tutorial 2T: Prof. Claude Fermon	Tutorial 2E: Prof. Leonel Sousa	LASCAS Steering Committee Meeting	
17:30 18:00					COFFE BREAK
18:00 19:30	Tutorial 3A: Prof. Edson W. Pereira Amateur Radio for Space Comm	Tutorial 2T: Prof. Claude Fermon	Tutorial 2E: Prof. Leonel Sousa		
20:00 22:00	Welcome reception: Cocktail				

Key:

LASCAS SESSIONS

IBERCHIP SESSIONS

IAALACW SESSIONS

LASCAS/IBERCHIP

COMMON

IAALACW & LASCAS & IBERCHIP PROGRAM

Day 2 – Monday 29th February 2016

		TOPAZIO ROOM				
	AGATA ROOM	TOPAZIO ROOM 1	TOPAZIO ROOM 2	ESMERALDA ROOM	DIAMANTE ROOM	HALL
08:00 08:50						Registration
08:50 09:00					Opening	
09:00 09:30	KEYNOTE 1A: Prof. Mikhail Ovchinnikov				KEYNOTE 1D: Prof. Simon Delionibus	
09:30 10:00	KEYNOTE 2A: Prof. Jordi Puig-Suari					
10:00 10:30						COFFE BREAK
10:30 12:30	Regular Session 1A: Latin America Projects Overview	Regular Session 1T: Digital Filters & Digital Signal Processing		Regular Session 1E: Computer Arithmetic & Specialized Processors	Regular Session 1D: Analog Circuits-I	
12:30 14:30						LUNCH
14:30 15:00					DIAMOND SPONSOR	
15:00 16:40	Regular Session 2A: Launch Systems and Opportunities Regular Session 3A: Modelling	Regular Session 2T: Bioengineering Circuits & Systems		Regular Session 2E: Signal Processing	Regular Session 2D: RF Circuits & Systems	
16:40 17:00						COFFE BREAK
17:00 18:00	Regular Session 4A: Educational Mission Management & Regulation				PANEL 1D: INDUSTRY SESSION	
18:00 18:20		Regular Session 3T.1: Sensor Circuits & Systems I	Regular Session 3T.2: Design methodology & CAD I	Regular Session 3E: Circuits & Systems for Communication	Regular Session 3D: FPGAs I	
18:20 19:20	PANEL 1A: INDUSTRY SESSION					

IAALACW & LASCAS & IBERCHIP PROGRAM

Day 3 – Tuesday 1st March 2016

		TOPAZIO ROOM				
	AGATA ROOM	**TOPAZIO ROOM 1**	**TOPAZIO ROOM 2**	**ESMERALDA ROOM**	**DIAMANTE ROOM**	**HALL**
09:00 9:30	KEYNOTE 3A: Prof. Shinichi Nakasuka				KEYNOTE 2D: Prof. Franco Maloberti	Registration
09:30 10:00	KEYNOTE 4A: Prof. Kevin Benjamin Malphrus					
10:00 10:30						COFFE BREAK
10:30 11:30	Regular Session 5A: AITV	Regular Session 4T.1: Digital Design and FPGA I	Regular Session 4T.2: Analog Design and RF	Invited Talk 1E: Prof. Israel Koren	Regular Session 4D: Analog Circuits II	
11:30 12:30	Regular Session 6A: Mission Applications					
12:30 14:30						LUNCH
14:30 15:10	Regular Session 7A: ADCS	Regular Session 5T.1: Digital Design and FPGA II	Regular Session 5T.2: Internet of Things	Regular Session 5E: Sensor Circuits & Systems II	Regular Session 5D: Design methodology & CAD II	
15:10 16:30						
16:30 17:00						COFFE BREAK
17:00 18:10	Regular Session 8A: ADCS				PANEL 2D: INDUSTRY SESSION	Poster Session 1H:
18:10 18:30				Regular Session 6E: FPGAs II		
18:30 19:30	PANEL 2A: INDUSTRY SESSION	Regular Session 6T: Analog Circuits III			Regular Session 6D: Imaging Techniques & Pattern Recognition	
20:00 22:00	Social Event					

IAALACW & LASCAS & IBERCHIP PROGRAM

Day 4 – Wednesday 2nd March 2016

	AGATA ROOM	TOPAZIO ROOM	ESMERALDA ROOM	DIAMANTE ROOM	HALL
09:00 09:30	KEYNOTE 5A: Prof. Mikhail Ovchinnikov			KEYNOTE 3D: Prof. Andreas Andreou	Registration
09:30 10:00	KEYNOTE 6A: Prof. Fernanda Lima				
10:00 10:30					COFFE BREAK
10:30 11:50	Regular Session 9A: On Board Systems (OBC, EPS, P/L)	Regular Session 7T: Integrated Sensors & Energy Harvesting	Regular Session 7E: Video Coding Architectures	Regular Session 7D: Low-Power Analog Circuits	Poster Session 2H:
11:50 12:30					
12:30 14:30					LUNCH
14:30 16:10	Regular Session 10A: TT&C	Regular Session 8T: High Level and Cryptography	Regular Session 8E: Logic Circuits & Neural Networks	Regular Session 8D: Energy Harvesting & Power Management	
16:10 16:30					
16:30 17:00					COFFE BREAK
17:00 17:15				Closing Remaks	

Sunday 28th February

Sunday 28th February, 14:00 – 15:30

TUTORIAL 1T / Topazio Room

"RFID Circuits & Systems – the chip perspective"

PROF. ALFREDO ARNAUD – Universidad Católica del Uruguay

Radio Frequency IDentification (RFID) is a widely used method to track pieces, vehicles, lots, animals, in diverse production systems. It is based in an integrated circuit, an antenna, and minimum extra components, hermetically sealed in diverse forms (tokens, paper tag, ear tag, etc. named just tags), capable to store information from an unique EAN.UCC number, to several Kbytes, and to transmit it later, contactless, to a reader unit. RFID market is estimated in more than 9 billion in 2015 and growing. In this tutorial the present and future of passive RFID will be discussed, with an emphasis on the circuit side. This tutorial starts with some application examples showing the utilization at the present, of RFID in animal ID, traceability within transportation, or retail industry, among others, including an overview of transponder types. The main standards corresponding to LF, HF, and UHF frequencies are presented examining existing transponder ICs, reader circuitry, costs, benefits and limitations in each case. The development and manufacture of custom tag and reader will be examined in each case. Other RFID standards and frequency ranges will be discussed, from state of the art RFID sensors, chipless RFID, and GHz range circuits. Finally, a brief analysis on the difficulties to develop an RFID transponder ASIC will be presented, including the digital and analog circuitry, antenna frontend, technology, packaging and assembly, and cost challenges. A survey in the state of the art including among others: recent products and recent published circuits, will be presented.

Sunday 28th February, 16:00 – 17:30 and 18:00 – 19:30

TUTORIAL 2T / Topazio Room

"Spin electronics and its applications"

PROF. CLAUDE FERMON – CEA Nanomagnetism and oxide lab France

Spin electronics is based on the use of not only the charge of electrons but also their magnetic moment. Since two decades, the main application of spin electronics has been read heads for hard disks but now spin electronics devices are used for a wide range of applications both for magnetic sensing and for data storage. In a first part, the tutorial will introduce the basic concepts of spin electronics and will discuss its integration with a CMOS flow. The second part will be devoted to applications of spin electronics to magnetic sensing. The third part of the tutorial will be centered of magnetic storage and radio frequency emission and detection.

Sunday 28th February, 16:00 – 17:30 and 18:00 – 19:30

TUTORIAL 2E / Esmeralda Room

"Cache-Aware Roofline Model: Performance, Power and Energy-Efficiency"

PROF. LEONEL SOUSA – INESC-ID/IST, Universidade de Lisboa – Portugal

As architectures evolve towards more complex multi-core designs, deciding what optimizations provide the best tradeoff between performance and efficiency is becoming a prominent issue. To help in this decision process, a set of fundamental models will be presented in these talks, which allow characterizing the upper bounds for performance, power, energy and energy-efficiency of multi-core architectures. These models evaluate how key micro-architectural aspects, such as accessing different functional units or different memory hierarchy levels, affect the attainable performance, power and efficiency of the processor (by also considering different power domains).

The proposed models are rigorously validated on different Intel microarchitectures by relying on hardware counters and especially developed highly accurate performance/power monitoring tools. The experimental results show a very high accuracy of the proposed models, and their ability to provide more intuitive and useful guidelines than the state-of-the-art approaches, when characterizing a set of synthetic and 38 standard benchmarks from SPEC CPU2006, PARSEC, SPLASH and MKL.

Monday 29th February

Monday 29th February, 9:00 – 10:00

KEYNOTE 1D / Diamante Room

"New Pathways to Future Silicon based Components Architectures and Integration"

PROF. SIMON DELIONIBUS – CEA-LETI, France

SESSION CHAIR: CARLOS SILVA-CÁRDENAS (PUCP)

Linear scaling CMOS has encountered many hurdles, which request new process modules, driven mainly by the maximization of energy efficiency. Fabrication at the sub 10nm node level will request Intrinsic Variability approaching to zero. Moreover, the rapid growth of mobile, multifunctional and autonomous systems is hardly demanding to reach Zero Power consumption. The solutions to integrate Thin Film based devices, architectures and systems in order to face these challenges will be addressed.

Monday 29th February, 10:30 – 12:30

LASCAS Session 1D / Diamante Room

Analog Circuits I / Session Chair: Eric Fabris (UFRGS)

10:30 "A Fully-Differential dc restoration circuit" Enrique Spinelli and Alejandro Veiga.

10:50 "A 90 dB PSRR, 4 dBm EMI Resistant MOSFET-Only Voltage Reference" David Cordova, Pedro Toledo, Hamilton Klimach, Sergio Bampi and Eric Fabris.

11:10 "Pipelined SAR with Comparator-Based Switch-Capacitor Residue Amplification" Frank Sill Torres and Pedro Henrique Köhler Marra Pinto.

11:30 "Self-Biased Class AB CMOS Current Buffer" Javier Alejandro Martínez Nieto, María Teresa Sanz Pascual, Nicolás J. Medrano Marqués and Belén Calvo López.

11:50 "An integrated H-Bridge circuit in a HV technology" Bruno Bellini, Alfredo Arnaud, Stephanía Rezk and Maximiliano Chiossi.

12:10 "A 7.8W continuous and 19.6W burst output power fully integrated 2S Class-D Amplifier with 0.005% THD+N" Mykhaylo Teplechuk, Franck Banag, Barry McAdam, Anthony Gribben and Zakaria Mengad.

Monday 29th February, 10:30 – 12:30

LASCAS Session 1E / Esmeralda Room

Computer Arithmetic & Specialized Processors/ Session Chair: Luiz Santos (UFSC)

10:30 "Area-Delay-Power-Aware Adder Placement Method for RNS Reverse Converter Design" Azadeh Alsadat Emrani Zarandi, Amir Sabbagh Molahosseini, Leonel Sousa, Mehdi Hosseinzadeh and Keivan Navi.

10:50 "RNS reverse converters for moduli sets with dynamic ranges of 9n-bit" Hector Pettenghi, Roberto de Matos and Amir Molahosseini.

11:10 "Design of A Low-Power RNS-Enhanced Arithmetic Unit" Piotr Patronik and Stanislaw Piestrak.

11:30 "The HF-RISC Processor: Performance Assessment" Sergio Johann Filho, Matheus Moreira, Ney L. V. Calazans and Fabiano Hessel.

11:50 A 32-bit 100MHz RISC-V Microcontroller with 10-bit SAR ADC in 130nm CMOS Ckristian Duran, Elkim Roa, Luis Rueda and Hugo Hernandez.

12:10 "Dynamic NoC Buffer Allocation for MPSoC Timing Side Channel Attack Protection" Johanna Sepulveda, Mathias Soeken, Daniel Florez, Guy Gogniat and Jean-Philippe Diguet.

Monday 29th February, 10:30 – 12:30

LASCAS Session 1T / Topazio Room

Digital Filters & Digital Signal Processing/ Session Chair: Sergio Bampi (UFRGS)

10:30 **"On Non-Recursive Comb-Cosine Decimation Structures"** Angel Garcia Robles and Gordana Jovanovic Dolecek.

10:50 **"A Filter Design for Blind Deconvolution to Decouple Unknown RDF/RTN Factors from Complexly Coupled SRAM Margin Variations"** Hiroyuki Yamauchi and Worawit Somha.

11:10 **"Exploiting Architectural Solutions for IIR Filter Architecture with Truncation Error Feedback"** Gustavo Ott, Eduardo A. C. Costa, Sergio J. M. Almeida, Maurício C. Tavares and Mateus B. Fonseca.

11:30 **"Exploiting Approximate Adder Circuits for Power- Efficient Gaussian and Gradient Filters for Canny Edge Detector Algorithm"** Julio Oliveira, Leonardo Soares, Eduardo Costa and Sergio Bampi.

11:50 **"Exploiting Adder Compressors for Power-Efficient 2-D Approximate DCT Realization"** Tiago Schiavon, Guilherme Paim, Mateus Fonseca, Eduardo Costa and Sergio Almeida.

12:10 **"Realization of 4D Lattice-Ladder Digital Filters"** M.T. Kousoulis and G.E. Antoniou.

Monday 29th February, 14:30 – 15:00

DIAMOND SPONSOR / Diamante Room

SESSION CHAIR: HAMILTON KLIMACH (UFRGS)

Mentor Graphics & Creative Solutions Presentation

Monday 29th February, 15:00 – 16:40

LASCAS Session 2D / Diamante Room

RF Circuits & Systems/ Session Chair: Mohamad Sawan (PolyMontreal)

15:00 **"0.8 V 450 µW 2.4 GHz PLL using Back-Gate QVCO for ZigBee/BLE standard in 0.18µm CMOS"** Purushothama Chary, Rizwan Shaik Peerla, Sesha Sairam Regulagadda, Naseeb Mohd Abdul, Amit Acharyya, Rajalaksmi P and Debashis Mandal.

15:20 **"A 30dBm PA for MTC communication in 65nm CMOS Technology"** Johan Wernehag, Waqas Ahmed, Henrik Sjöland, Olof Zander and Vanja Plicanic Samuelsson.

15:40 **"2.4 GHz CMOS Digitally Programmable Power Amplifier for Power Back-off Operation"** Fávero Santos, Andre Mariano and Bernardo Leite.

16:00 **"Simple expression for estimating the switch peak voltage on the class-E amplifier with finite dc-feed inductance"** Arturo Fajardo and Fernando Rangel de Sousa.

16:20 **"CMOS RF Class-E Power Amplifier with Power Control"** Diogo Santana, Hamilton Klimach, Eric Fabris and Sergio Bampi.

Monday 29th February, 15:00 –16:40

LASCAS Session 2E / Esmeralda Room

Signal Processing/ Session Chair: Leonel Sousa (INESC-ID/IST, Universidade de Lisboa)

15:00 "Implementation of method of characteristics on a single board computer to infer Down-hole Dynamometer Cards" Nestor Cáliz, Alexander Molero, Miguel Bravo and Jesús Pérez.

15:20 "Range Segmentation to Improve Latency in Parallel Stochastic Computing" Rai Saraiva, Rafael Soares, Julio Ruzicki and Adão Souza Jr.

15:40 "Detection of ENF Discontinuities Using PLL for Audio Authenticity" Magdalena Fuentes, Pablo Zinemanas, Pablo Cancela and José Antonio Apolinário Jr.

16:00 "Parallel Algorithm Mapping to Memory Multidimensional Signals" Florin Balasa, Ilie I. Luican and Hongwei Zhu.

16:20 "Telepresence using the Kinect sensor and the NAO robot" Jose Avalos, Sergio Cortez, Karina Vasquez, Victor Murray and Oscar Ramos.

Monday 29th February, 15:00 – 16:40

LASCAS Session 2T / Topazio Room

Bioengineering Circuits & Systems/ Session Chair: Alfredo Arnaud (UCU)

15:00 "A Low Energy Pulse Interval Modulation Scheme for Biomedical Wireless Sensors" Decio Faria, Tales Pimenta and Robson Moreno.

15:20 "Cell-Culture Measurements using Voltage Oscillations" Andrés Maldonado, Pablo Pérez, Gloria Huertas, Alberto Yúfera, Adoración Rueda and José Luis Huertas.

15:40 "Redundant Measurement of Vital Signs in a Wearable Monitor to Overcome Movement Artifacts in Home Health Care Environment" Fabian Andres Castaño Usuga, Alher Mauricio Hernández, Carlos Andres Sarmiento, Alejandro Camacho, Cristian Vega and Juan Diego Lemos.

16:00 "Bioimpedance Measurement Using Mixed-Signal Embedded System" John Jairo Cabrera Lopez, Jaime Velasco-Medina, Ernesto Rodríguez Denis, Juan Felipe Briceño Calderon and Oscar Julián Gómez Guevara.

16:20 "Effects of Nanoelectroporation on Plasma and Nuclear Membranes" Lucenara Dos Santos Pereira and Daniela Suzuki.

Monday 29th February, 17:00 – 18:00

PANEL 1D / Diamante Room

INDUSTRY SESSION

SESSION CHAIR: VICTOR GRIMBLATT (SYNOPSYS)

This session includes presentations by:
– Mentor Graphics
– Synopsys
– Allegro
– Cadence (to be confirmed)

Monday 29th February, 18:00 – 19:20

LASCAS Session 3D / Diamante Room

FPGAs I / Session Chair: Tiago Balen (UFRGS)

18:00 "A Fault Injection Platform for FPGA-based Communication Systems" Marcos T. Leipnitz, Geferson L. H. Júnior and Gabriel L. Nazar.

18:20 "An FPGA-based Emulation Platform for Evaluation of Time-Interleaved ADC Calibration Systems" Raul M. Sanchez, Benjamin T. Reyes, Ariel L. Pola and Mario R. Hueda.

18:40 "Reduced power consumption in the FPGA-based Universal Link for LVDS Communications" Luis Sanchez, Giancarlo Patiño, Victor Murray and James Lyke.

19:00 "Multiband Ultra-Wideband Receiver Implementation in a Low Cost FPGA" Mário Véstias.

Monday 29th February, 18:00 –19:20

LASCAS Session 3E / Esmeralda Room

Circuits & Systems for Communication/ Session Chair: Claudio Reyes (Mentor Graphics)

18:00 "Hardware Implementation of FFT-based Spectrum Sensing Techniques for Cognitive Radio" Juan Felipe Medina Lee, Alexander López Parrado and Jaime Velasco Medina.

18:20 "Real-Time CPU-GPU Demodulator for the LTE Physical Layer" Ouajdi Brini and Mounir Boukadoum.

18:40 "WBAN, MBAN or WBSN?" Arturo Fajardo and Fernando Rangel de Sousa.

19:00 "A low-jitter DTC with look-ahead multi-phase DDS" Harishankar Sahu, Pallavi Paliwal, Vivek Yadav and Shalabh Gupta.

Monday 29th February, 18:00 – 19:20

LASCAS Session 3T.1 / Topazio Room 1

Sensor Circuits & Systems I / Session Chair: Franco Maloberti (University of Pavia)

18:00 "Photoresponse and color dependent crosstalk in an annular imager for an NDB Optical Encoder" Nicolás Calarco, Fernando Perez Quintián, Ariel Lutenberg and Jose Lipovetzky.

18:20 "A Capacitive Sensor Interface for High-Resolution Acquisitions in Hostile Environments" Dante Gabriel Muratore, Edoardo Bonizzoni, Franco Maloberti and Carlo Fiocchi.

18:40 "A low-cost microcontrolled dosimeter based on CD4007 devices for in vivo radiotherapy applications" Osmar Franca Siebel, Crystian Wilian Chagas Saraiva, Francisco Javier Ramirez-Fernandez, Marcio Cherem Schneider and Carlos Galup-Montoro.

19:00 "A 3.9 Compression-Ratio Huffman Encoding Scheme for the Large Ion Collider on 65nm and 130nm CMOS technologies" Edwin G. Carreño, Christian D. Hernandez, Oscar M. Diaz, Hector I. Gomez, Carlos A. Fajardo, Elkim F. Roa and Hugo Hernandez, Wilhelmus Van Noije.

Monday 29th February, 18:00 – 19:20

LASCAS Session 3T.2 / Topazio Room 2

Design methodology & CAD I / Session Chair: Ricardo Reis (UFRGS)

18:00 **"Analog Layout Automation via Self-organization: Enhancing the Novel SWARM Approach"** Daniel Marolt, Juergen Scheible, Goeran Jerke and Vinko Marolt.

18:20 **"A CAD-oriented simulation methodology for memristive circuits"** Arturo Sarmiento-Reyes, Jesús Jiménez-León, Luis Hernández-Martínez and Héctor Vázquez-Leal.

18:40 **"Topological Characteristics of Logic Networks Generated by a Graph-Based Methodology"** Maicon S. Cardoso, Regis Zanandrea, Renato S. De Souza, João J. Da S. Machado, Leomar S. Rosa Junior and Felipe S. Marques.

19:00 **"Optimizing Cell Area by Applying an Alternative Transistor Folding Technique in an Open Source Physical Synthesis CAD Tool"** Gustavo Smaniotto, Leomar Rosa Jr, Felipe S. Marques, João J. S. Machado, Adriel Ziesemer Jr. and Matheus Moreira.

Tuesday 1st March

Tuesday 1st March, 9:00 – 10:00

KEYNOTE 2D / Diamante Room

"Very-Low-Voltage and Ultra-Low-Power Analog Circuits for Nomadic Applications"

PROF. FRANCO MALOBERTI – University of Pavia, Italy

SESSION CHAIR: ROBERTO S. MURPHY (INAOE)

In recent years, there has been an increasing demand of so-called autonomous applications, that means applications that do not need and do not have the possibility of refueling the energy as it is commonly done with battery operated devices. This kind of systems harvests power from the environment by transforming what is available into electrical form. The source can be light, electromagnetic waves, temperature, vibration and energy generated by bacteria. In addition, there are systems that are not in the same spatial positions, but move around transported by a person or an object. In this case, we talk about nomadic electronics. In all the above situations, it is necessary to have harvested energy that is often very limited. Thus, in order to ensure a good autonomy, it is necessary to use electronic circuits consuming very low power. Moreover, the transducer used to transform the energy into electrical form generates very low voltage. Therefore, for autonomous and much more for nomadic applications, it is necessary to use electronic circuits operating with very low-voltage and consuming ultra-low power.

This presentation discusses about nomadic systems considering both the ones carried by human and the ones carried by animals or things. It presents different methods to harvest energy and finally discusses in some details about electronic systems suitable for those applications. Namely it reviews the state of the art and provides recently published examples of low power low voltage analog circuits, such as operational amplifiers, reference generators, and data converters.

Tuesday 1st March, 10:30 – 12:30

LASCAS Session 4D / Diamante Room

Analog Circuits II / Session Chair: Eric Fabris (UFRGS)

10:30 **"Analysis of Graphene Field Effect Transistor Based Current Mirrors"** Nİhat Akkan and Burcu Erkmen.

10:50 **"A High-Slope PTAT Temperature Sensor for Frequency Compensation of an RTC Oscillator"** Sergio Chaparro, Juan Carrillo and Heiner Alarcon.

11:10 **"Study of Layout Extraction Accuracy on W/L Estimation of ELT in Analog Design Flow"** Guilherme Cardoso and Tiago Balen.

11:30 **"High-Linearity Zero-Voltage Switching Current Memory Cell for Measurement Applications"** Eduardo Vilela Pinto Dos Anjos and Fernando Antonio Pinto Barúqui.

11:50 **"Revisiting the power-efficiency trade-off on a DC voltage source"** Arturo Fajardo and Fernando Rangel de Sousa.

12:10 **"Wireless Monitoring of Collagen Progression around Implantable Prostheses"** Ahmad Hassan.

Tuesday 1st March, 10:30 – 11:30

INVITED TALK 1E / Esmeralda Room

"Defect Reduction and Fault Tolerance in VLSI Integrated Circuits"

PROF. ISRAEL KOREN – University of Massachusetts at Amherst USA

SESSION CHAIR: JACOBUS SWART (IMEC)

Advances in VLSI technology allow now the integration of billions of devices in a single IC (e.g., a quad-core microprocessor) at an increasing device density. This trend unfortunately, also increases the likelihood of manufacturing defects, which if ignored, will result in a very low yield, where yield is the percentage of good ICs out of a manufactured wafer. Techniques to reduce the number of defects and tolerate the few that may still occur have been developed and are increasingly being used in the design of recent VLSI ICs, in general, and microprocessors, in particular.

In this talk we first describe the types of defects that modern VLSI ICs are experiencing. We then briefly discuss the approaches used to identify the areas of the chip that are most sensitive to manufacturing defects and present the way yields of future ICs are predicted. Finally, we describe the currently employed techniques for reducing the number of chip-kill defects and for tolerating the defects that still remain.

Tuesday 1st March, 10:30 – 12:30

IBERCHIP Session 4T.1 / Topazio Room 1

Digital Design and FPGA I / Session Chair: Gloria Huertas (Universidad de Sevilla)

10:30 **"Fixed-point FPGA Implementation and Comparative Analysis of Real-valued RBFNNs for the Behavioral Modeling of RF Power Amplifiers"** Walter Bastos Pfeffer, André Felipe Zanella, Caroline De França, Luiza Beana Chipansky Freire and Eduardo Gonçalves De Lima.

10:50 **"Avaliação da degradação causada pelo BTI em células de 32nm"** Rafael Schivittz, Cristina Meinhardt and Paulo F. Butzen.

11:10 **"Estudo Comparativo de Filtros Digitais FIR"** Leandro Dias Da Silva and Eduardo Gonçalves De Lima.

11:30 **"Interfaces Insensíveis a Latência para Sistemas Heterogêneos"** Duarte Oliveira, Kledermon Garcia and Lester Faria.

11:50 **"Uma Nova Arquitetura para Sistemas Pipeline Síncrono Insensíveis a Latência"** Duarte Lopes, Kledermon Garcia and Lester Faria.

12:10 **"Simple Control Architectures for Asynchronous Pipelines on FPGAs"** Duarte Oliveira, Kledermon Garcia and Lester Faria.

Tuesday 1st March, 10:30 – 12:30

IBERCHIP Session 4T.2 / Topazio Room 2

Analog Design and RF / Session Chair: Alfredo Arnaud (UCU)

10:30 **"Design of a Readout Circuit for Low-Cost Microbolometer Infrared Focal Plane Arrays"** Leonardo Sa, Germano Fonseca and Antonio Mesquita.

10:50 **"Reconfigurable switched-capacitor base band filters for Software Defined Radio transceivers"** Renato Macedo and Luis Lolis.

11:10 **"Design of a 135dB-Gain-Boosted Telescopic-Cascode OTA for a Precision Offset-Compensated SC Integrator"** Andre Aita.

11:30 **"Linearity characterization of a CMOS Power Amplifier for IEEE 802.15.4, IEEE 802.11n and LTE signals"** Marco Antonio Rios, Edson Santos, Bernardo Leite, Luis Lolis and Andre Mariano.

11:50 **"PVT Analysis of a 2.4 GHz 19.9 dBm Fully Integrated CMOS Power Amplifier with 23.5 dB Gain"** Fávero Santos, Andre Mariano and Bernardo Leite.

12:10 **"A CMOS implementation of the discrete time nonlinear energy operator based on current squarer circuit"** Julio Saldaña-Pumarica and Emilio Del-Moral-Hernandez.

Tuesday 1st March, 14:30 – 16:30

LASCAS Session 5D / Diamante Room

Design methodology & CAD II / Session Chair: Luiz Santos (UFSC)

14:30 "Improving a Design Methodology of Synthesizable VHDL With Formal Verification" Luis Gustavo Perpetuo Costa Marques, Max Hering De Queiroz and Jean-Marie Farines.

14:50 "Reducing the Number of Transistors with Gate Clustering" Calebe Conceicao, Gracieli Posser and Ricardo Reis.

15:10 "MOS-Only Circuit Design Automation" Deniz Ozenli and Hakan Kuntman.

15:30 "A Method for Quick Estimation of Optimum Bulk Bias Voltages for SoC Designs" Lucas Santis and Ronald Valenzuela.

15:50 "A Design Flow for Locally-Clocked XBM Asynchronous State Machines using Synchronous CAD Tools" Duarte Lopes, Felipe Tuyama, Tiago Curtinhas, Lester Faria and Jocemar Sousa.

16:10 "A New Methodology for Design and Simulation of NML Circuits" Thiago Rodrigues Barros Da Silva Soares, Isaias F. Silva, Luiz G. C. Melo and Omar P. Vilela Neto.

Tuesday 1st March, 14:30 – 16:30

LASCAS Session 5E / Esmeralda Room

Sensor Circuits & Systems II / Session Chair: Sergio Bampi (UFRGS)

14:30 "A Smart Pressure Sensor System Based on DSP-uC Combination for MEMS" Arturo Hernández González, Jorge Ramírez Beltrán, Luis Ernesto Farah Fernández and Edgar Charry Rodríguez.

14:50 "High-Voltage Pulse Generator with Variable Delay for Ultrafast Gating of Single Photon Detector" Sreenil Saha, Frederic Lesage and Mohamad Sawan.

15:10 Development of a Biotelemetry System with a Microcontrolled Sensing Unit Luian Halisson Zanoni and Fabio Luiz Bertotti.

15:30 "Surface Electromyography Measurements for Ingestive Behaviour Identification on Goats" Daniel P. Campos, Paulo J. Abatti, Fábio L. Bertotti, André L. F. Silveira and João A. G. Hill.

15:50 "Requirements for an Integrated Conditioning Circuit for Multiphase Flow Imaging Using Impedance Wire-Mesh Sensors" José Batista de Sales Filho, Carlos Antonio Mendes Da Costa Júnior, Gabriel Costa Leal Da Cunha, Diomadson Rodrigues Belfort, Sebastian Yuri Cavalcanti Catunda, Marco José Da Silva and Eduardo Nunes Dos Santos.

16:10 "Mismatch and Temperature Compensation for Subthreshold Seismic Sensor System" Uldric Antao, John Choma, Theodore Berger and Alireza Dibazar.

Tuesday 1st March, 14:30 – 16:30

IBERCHIP Session 5T.1 / Topazio Room 1

Digital Design and FPGA II / Session Chair: Tiago Balen (UFRGS)

14:30 **"Projeto de um Circuito Integrado para Auxílio ao Controle de Servo Motores"** Lucas R. Garcia and Roberto R. Neli.

14:50 **"Minimização Lógica por Fusão de Portas"** Luciana Mendes Da Silva, Calebe Micael de Oliveira Conceição, Guilherme Bontorin and Ricardo Reis.

15:10 **"Implementação de Baixa Latência do Modelo Simples de Izhikevich em FPGA"** Vitor Bandeira, Vivianne L. Costa, Guilherme Bontorin and Ricardo Reis.

15:30 **"Avaliação da robustez de somadores de 1 bit na tecnologia de 32nm a variabilidade PVT"** Stéphanie Ames, Vinícius Zanandrea and Cristina Meinhardt.

15:50 **"Optimized Design by Direct Mapping of Extended Burst-Mode Asynchronous State Machines"** Duarte Oliveira, Felipe Tuyama, João Figueiredo and Lester Faria.

16:10 **"FPGA Implementation of SPI-Slave for Microcontroller GPIO Port Expander"** Fernando Santin.

Tuesday 1st March, 14:30 – 15:10

IBERCHIP Session 5T.2 / Topazio Room 2

Internet of Things / Session Chair: Sergio Lima Netto (UFRJ)

14:30 **"Low-Cost Embedded Cooperative Cognitive Radio for Internet of Things"** Daniel Mazzer, Marília Martins Bontempo and Arismar Cerqueira Sodré Junior.

14:50 **"Factorial Design Analysis Applied to the Performance of Transmission Power Optimization Techniques for Wireless Sensor Networks"** Jonathan C. Silva, Felipe Andery, Daniel Mazzer, Edielson Prevato Frigieri, Arismar Cerqueira Sodré Junior and Lucas D. P. Mendes.

Tuesday 1st March, 16:30 – 18:30

IBERCHIP Poster Session 1H / Hall

SESSION CHAIR: MARCELO PORTO (UFPEL)

"Análise do Timing Vulnerability Factor em Flip-Flop D Mestre-Escravo em Nanotecnologias" Alexandra Lackmann Zimpeck, Fernanda Lima Kastensmidt and Ricardo Reis.

"IP core DALI" Bruno Valinoti, Rodrigo Alejandro Melo, Francisco Salomón and Leandro Tozzi.

"IP core FFT configurable en Runtime" Rodrigo Alejandro Melo and Francisco Salomón.

"A New Control for MOUSETRAP Asynchronous Pipelines" Duarte Lopes and Lester Faria.

"Uma Técnica para Avaliação da Confiabilidade em Circuitos Nanométricos" Rafaél Ígor Fritz and Denis Teixeira Franco.

"Efeitos da variabilidade PVT em diferentes técnicas de dimensionamento de transistores FinFET" Alexandra Lackmann Zimpeck, Cristina Meinhardt, Gracieli Posser and Ricardo Reis.

"Characterization of High Voltage MOS Transistors for Analog Design" Rafael Puyol, Matias Miguez and Joel Gak.

"NFAS-tool: avaliação da confiabilidade de células combinacionais sob falhas de radiação do tipo SET" Ygor Quadros De Aguiar, Alexandra Lackmann Zimpeck and Cristina Meinhardt.

"Revisiting battery modeling using the energy power supply concept" Arturo Fajardo and Fernando Rangel de Sousa.

"Controlador por Modos Deslizantes Aplicado ao Motor BLDC" Everson Siqueira, Vinicius Menezes De Oliveira and Rodrigo Azzolin.

"A Survey on Network-on-chip Implementations of Spiking Neural Networks" Priscila Holanda, Guilherme Bontorin and Ricardo Reis.

"High throughput FPGA camera interface for a vision based robotic welding system" Cristiano Steffens, Sidnei Silva, Bruno Leonardo, Valquiria Huttner, Vagner Rosa and Silvia Botelho.

Tuesday 1st March, 17:00 – 18:30

PANEL 2D / Diamante Room

INDUSTRY SESSION

SESSION CHAIR: VICTOR GRIMBLATT (SYNOPSYS)

Project presentations:
- **Chipus (Brazil) –** Murilo Pessatti
- **Tecnocal (Chile) –** Victor Grimblatt
- **BQN (Uruguay) –** Alfredo Arnaud
- **CCC (Uruguay)** – Stefano Ghiardo
- **CPqD (Brazil)** – Eudes Prado Lopes Filho
- **Eldorado (Brazil)** – Jose Eduardo Bertuzzo

Tuesday 1st March, 18:30 – 19:30

LASCAS Session 6D / Diamante Room

Imaging Techniques & Pattern Recognition / Session Chair: Arturo Sarmiento (INAOE)

18:30 "System-level Design for Human Detection in 3D Scenes" Amin Safaei and Q. M. Jonathan Wu.

18:50 "Audio Anomaly Detection on Rotating Machinery Using Image Signal Processing" Thiago Prego, Amaro Lima, Sergio Netto and Eduardo Silva.

19:10 "Combined Partial Differential Equation Filtering and Particle Swarm Optimization For Noisy Biomedical Image" Segmentation Salim Lahmiri and Mounir Boukadoum.

Tuesday 1st March, 18:10 – 19:30

LASCAS Session 6E / Esmeralda Room

FPGAs II / Session Chair: Frank Torres (UFMG)

18:10 "Digital Circuit for the Generation of Colored Noise Exploiting Single Bit Pseudo Random Sequence" Ettore Napoli, Gerardo Castellano, Darjn Esposito and Antonio G.M. Strollo.

18:30 "A 17 bits Pulse Width Modulation Circuit in FPGA" Lucas Salomon, Robson Moreno and Tales Pimenta.

18:50 "Online Terrain Classification for Mobile Robots using FPGAs" Rafael Tolentino Rabelo and Daniel Muñoz Arboleda.

19:10 "A Pulse Generator with Poisson-Exponential Distribution for Emulation of Radioactive Decay Events" Alejandro Veiga and Enrique Spinelli.

Tuesday 1st March, 18:30 – 19:30

LASCAS Session 6T / Topazio Room

Analog Circuits III / Session Chair: Gloria Huertas (Universidad de Sevilla)

18:30 "Distortion Analysis of Integrated Analog Multipliers: DC versus AC Approaches" Gabriele Costa Gonçalves, Fabian Souza de Andrade, Henrique Alves Gaspar Ribeiro, Shirlene De Santana Soares, Isan Mattos Nassiffe, Edson Pinto Santana and Ana Isabela Cunha.

18:50 "Characterization of Transmission Lines in a Novel High-Frequency Laminate" Abel Pérez, Diego Cortez, Reydezel Torres and Alfonso Torres.

19:10 "A CMOS implementation of the discrete time nonlinear energy operator based on a Transconductor-Squarer circuit" Julio Saldaña-Pumarica, Carlos Silva and Emilio Del-Moral-Hernandez.

Wednesday 2nd March

Wednesday 2nd March, 9:00 – 10:00

KEYNOTE 3D/ Diamante Room

"BRAINWAY: Cognitive Computing using Energy Efficient Physical Computational Structures, Algorithms and Architecture Co-Design"

PROF. ANDREAS ANDREOU – John Hopkins University, USA

SESSION CHAIR: ELKIM ROA (RAMBUS)

Since the invention of the integrated circuit – the chip in short – in the 1950's, the microelectronics industry has seen a remarkable evolution from the centimeter scale devices created Future projected needs in data centers are data intensive applications in Cognitive Computing Technology (CCT). CCT aims at advancing intelligent software and hardware that can process, analyze, and distill knowledge from vast quantities of text, speech, images and biological data ultimately with and as much nuance and depth of understanding as a human would. To meet the scientific demand for future data-intensive CCT for every day mundane tasks such as searching via images to the uttermost serious health care disease diagnosis in personalized medicine, we urgently need a new cloud computing paradigm and energy efficient i.e. green technologies. The TrueNorth platform from IBM is an excellent example of such as systems. The BRAINWAY project in my lab is aimed at the design of an energy efficient Cognitive Processor Unit (CogPU) that combines Ultra-Low-Voltage (ULV) circuit techniques with brain-inspired chip-multiprocessor network-on-chip (NoC) architecture, in 3D CMOS technology. The design of the CopPU architecture is based on the recently developed mathematical framework for architecture exploration and optimization, where neurons are abstracted as arithmetic units, processing information using stochastic or deterministic unary representations. Data in the system represent probabilities a choice that is well suited for probabilistic inference and machine learning. Such highly energy efficient CogPU inference engine will provide an energy efficiency gain of about ×65 by using ULV techniques and massive parallelism, a gain of about ×10 by relying on its SOC 3D DRAM, and a gain of about ×15 by relying on new memory based Bayesian inference computational structures. This yields an estimate aggregate improvement factor in energy efficiency of about ×10000, roughly four to five orders of magnitude with respect to present day state-of-the-art. Preliminary results from fabricated chips in the Global Foundries 55nm technology confirm our estimates and to the best of our knowledge these are the first CMOS computer architecture that computes natively with probabilities. I will discuss the design and experimental results from sub-systems of the architecture, representing processing units for exact and approximate Bayesian inference, multi-variate function approximation, including circuit details for mixed signal vector-vector multiplier units, physical random number generators. The final silicon for the BRAINWAY architecture is taping out in the Tezzaron 3D CMOS technology.

Wednesday 2nd March, 10:30 – 12:30

LASCAS Session 7D / Diamante Room

Low-Power Analog Circuits / Session Chair: Fernando Silveira (Universidad de la Republica)

10:30 **"1.5 ppm/°C Nano-Watt Resistorless MOS-Only Voltage Reference"** Jhon Alexander Gómez Caicedo, Hamilton Klimach, Eric Fabris and Sergio Bampi.

10:50 **"Low Voltage Low power Current Reference Circuit for Passive RFID applications"** Dalton Colombo, Rafael Soares and Fabricio Mattos.

11:10 **"A 150 nW 32 kHz mobility-compensated relaxation oscillator with +/- 30 ppm/ºC temperature stability"** Agossou Wilfried Zomagboguelou, Carlos Galup Montoro and Marcio Cherem Schneider.

11:30 **"Nano-Watt 0.3 V Supply Resistorless Voltage Reference with Schottky Diode"** Renato Campana, Hamilton Klimach and Sergio Bampi.

11:50 **"0.3 V Supply 17 ppm/oC 3-Transistor Picowatt Voltage Reference"** Arthur Campos De Oliveira, Jhon Gomez Caicedo, Hamilton Duarte Klimach and Sergio Bampi.

12:10 **"Stable Ring Oscillator for Ultra Low Voltage Supplies"** Luis Henrique Rodovalho, Eric Fabris and Hamilton Klimach.

Wednesday 2nd March, 10:30 – 12:30

LASCAS Session 7E / Topazio Room

Video Coding Architectures / Session Chair: Jorge Juan (Universidad de Sevilla)

10:30 **"Memory Access Profiling for HEVC Encoders"** Ana Clara Mativi de Souza, Eduarda Monteiro and Sergio Bampi.

10:50 **"Rate-Distortion-Complexity Analysis for Prediction Unit Modes in 3D-HEVC Depth Coding"** Ruhan Conceição, Giovanni D. de Ávila, Guilherme Corrêa, Luciano Agostini, Bruno Zatt and Marcelo Porto.

11:10 **"Squarer Exploration for Energy-Efficient Sum of Squared Differences"** Ismael Seidel, Marcio Monteiro, Jose Luis Güntzel and Luciano Volcan Agostini.

11:30 **"Energy Analisys of Motion Estimation Memory Transference on Embedded Processors"** Henrique Maich, Mateus Melo, Luciano Agostini, Bruno Zatt and Marcelo Porto.

11:50 **"Solutions for DMM-1 Complexity Reduction in 3D-HEVC Based on Gradient Calculation"** Mário Saldanha, Gustavo Sanchez, Bruno Zatt, Marcelo Porto and Luciano Agostini.

12:10 **"Wide Area Motion Imagery Processing Pipeline Using Bio-inspired, Probabilistic Event-Based Computational Structures"** Andreas Andreou.

Wednesday 2nd March, 10:30 – 11:50

IBERCHIP Session 7T / Topazio Room

Integrated Sensors & Energy Harvesting / Session Chair: Duarte Oliveira (ITA)

10:30 "Ultra low power integrated circuits for energy harvesting" Alison Lando, Romain Berges, Bernardo Leite, Thierry Taris and Andre Mariano.

10:50 "Diseño de nodos sensores para apoyo médico en situaciones críticas" Jorge Olarte, Mónica Vallejo, José Aedo, Eugenio Duque and Fredy Rivera.

11:10 "Pneumatic testing of an electro-optical MEMS device" Sergio Baron and Hyun Jung.

11:30 "Caracterización y reducción de artefactos debidos a materiales metálicos en sistemas de seguimiento electromagnéticos" Daniel Estrada, Mauricio Hernández, Felipe Vallejo, Helber Carvajal and Diego Lemos.

Wednesday 2nd March, 14:30 – 16:30

LASCAS Session 8D / Diamante Room

Energy Harvesting & Power Management / Session Chair: Stanislaw Piestrak (Université de Lorraine)

14:30 "Energy harvesting with 3D-printed electrostatic generators" Antonio Queiroz and Luiz Carlos Oliveira Filho.

14:50 "DC-DC Switching Converter as On-Field Self Energy Meter" Javier Schandy, Julián Oreggioni and Leonardo Steinfeld.

15:10 "Hybrid Dual-Mode Low Voltage Dropout Regulator with Infinite Impulse Response Digital Filters" David Kwong Heng Phoon, Torsten Lehmann, Tara Hamilton and Julian Jenkins.

15:30 "Design of a Low-Cost and High-Performance Digital PWM Controller for DC-DC Converters" Filipe Ramos, Tales Pimenta and Luis Ferreira.

15:50 Matching Networks for Maximum Efficiency in Two and Three Coil Wireless Power Transfer Systems Pablo Pérez-Nicoli and Fernando Silveira.

16:10 "An Energy Harvesting Chip designed to Extract Maximum Power from a TEG" Arun Sinha, Marcio Cherem Schnieder and Rafael Luciano Radin.

Wednesday 2nd March, 14:30 – 16:10

LASCAS Session 8E / Esmeralda Room

Logic Circuits & Neural Networks / Session Chair: Johanna Sepulveda (TU München)

14:30 **"Design of Optimized Radix-2 and Radix4 Butterflies from FFT with Decimation in Time"** Renato Neuenfeld, Mateus Fonseca and Eduardo Da Costa**.**

14:50 **"Performance Evaluation of Optimized Transistor Networks Built Using Independent Gate FinFET"** Andres Mauricio Asprilla Valdes, Vinicius Possani, Felipe Marranghello, Renato Ribas and André Reis.

15:10 **"A Modified Synapse Model for Neuromorphic Circuits"** Amirhossein Kazemi, Arash Ahmadi, Shahpour Alirezaee and Majid Ahmadi.

15:30 **"The Influence of Feature Vector on the Classification of Mechanical Faults using Neural Networks"** Denys Pestana-Viana, Rafael Zambrano-López, Amaro A. de Lima, Thiago De M. Prego, Sergio L. Netto and Eduardo A. B. Da Silva.

15:50 **"Neuromorphic Sampling on the SpiNNaker and Parallella Chip Multiprocessors"** Andreas Andreou and Daniel Mendat.

Wednesday 2nd March, 14:30 – 16:10

IBERCHIP Session 8T / Topazio Room

High Level and Cryptography / Session Chair: Andre Aita (UFSM)

14:30 **"Mecanismos de Autenticação em Smart Card utilizando Criptografia Totalmente Homomórfica"** Lucas Ladeira, Fábio Pereira and Edward Ordonez.

14:50 **"Melhorando o Desempenho da IPNoSys com Software Pipelining"** Denis F. L. Nunes and Silvio R. Fernandes.

15:10 **"Proposta de uma Hierarquia de Memória para a Arquitetura IPNoSys"** Alexandro Damasceno, Silvio Fernandes and Gustavo Girão.

15:30 **"Desempenho de Aplicações com OpenCV4Android em Smartphones"** Geison Quevedo and Vagner Santos Da Rosa.

15:50 **"Case study: performance and power analysis of a dynamically reconfigurable hardware/software"** Mauricio Fayula, Jorge Juan and Julian Viejo**.**

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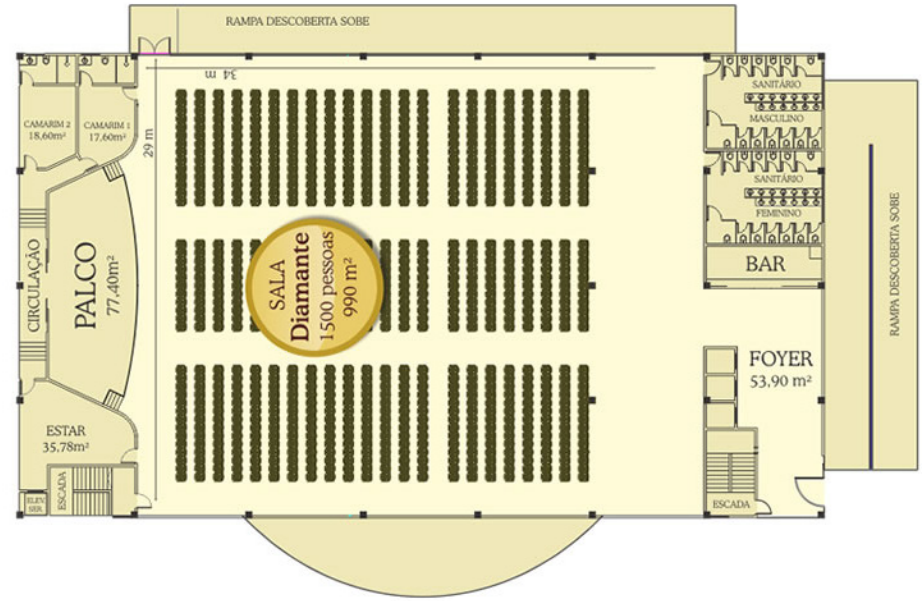

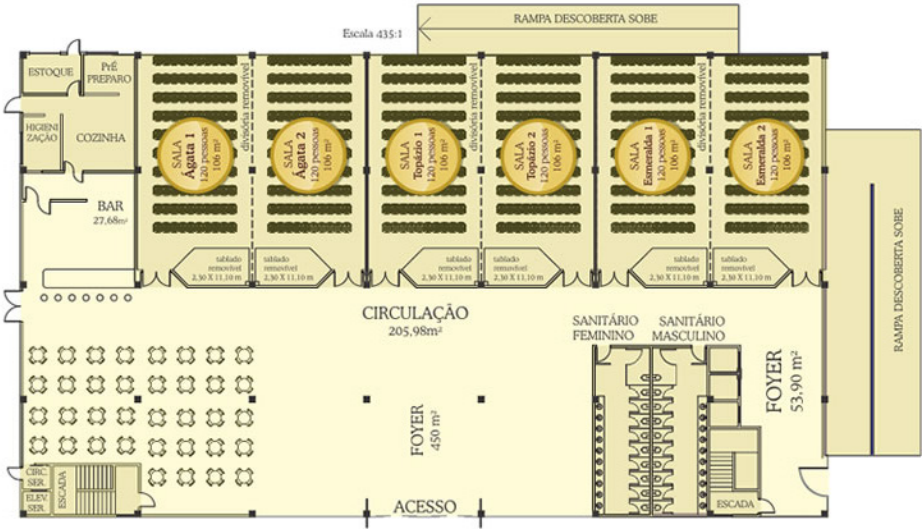

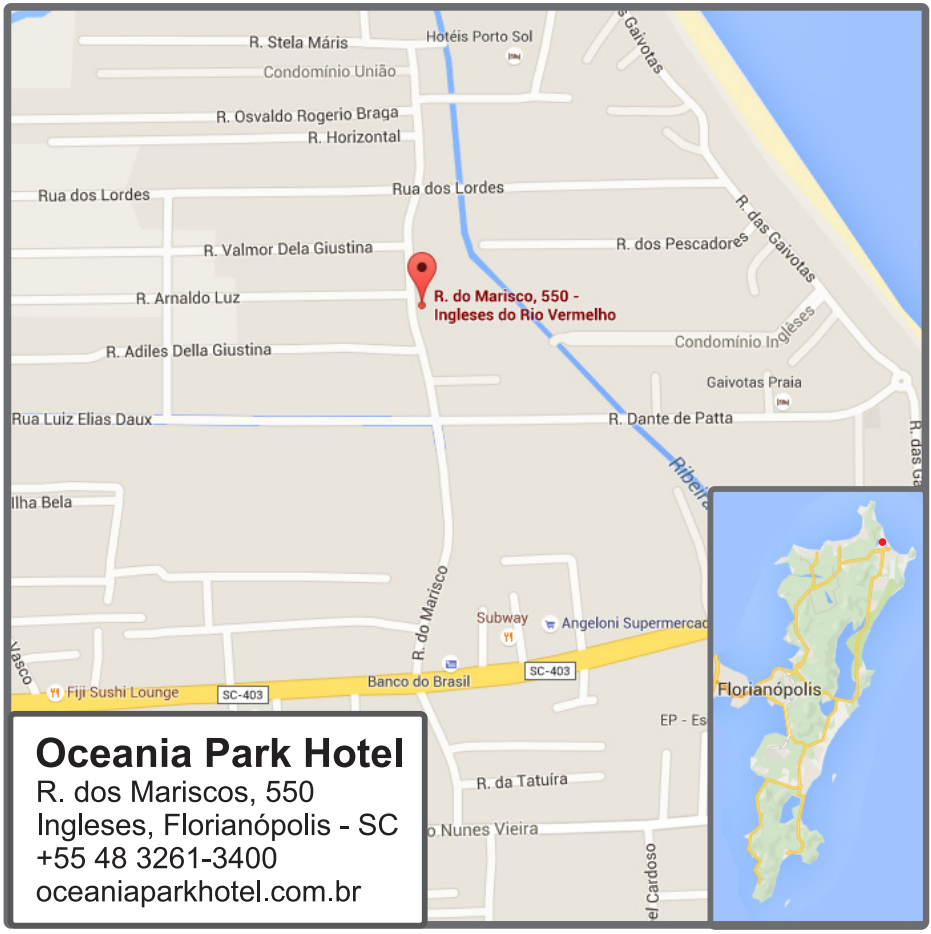

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