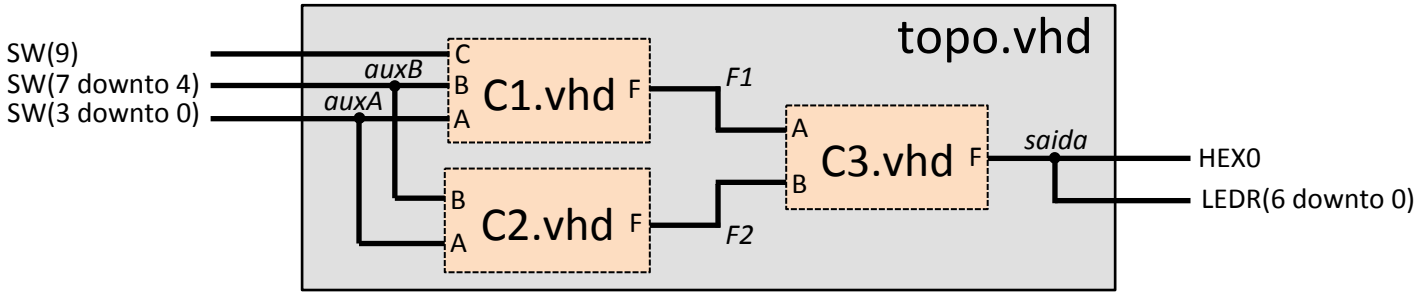
```
-- UFSC - EEL 5105 - Circuitos e Tecnicas Digitais
-- Prof. Eduardo Augusto Bezerra <Eduardo.Bezerra@ufsc.br>
-- Exemplo de uso de componentes em VHDL.   Data da ultima alteracao: 11 de setembro de 2019.
-- Arquivos componentes desse projeto: topo.vhd, C1.vhd, C2.vhd e C3.vhd
```




```
-- topo.vhd
library  ieee;
use  ieee.std_logic_1164.all;

entity topo is
  port ( SW: in std_logic_vector(9 downto 0);
         LEDR: out std_logic_vector(9 downto 0);
         HEX0: out std_logic_vector(6 downto 0)
       );
end topo;

architecture topo_bhv of topo is

  signal auxA,auxB: std_logic_vector(3 downto 0);
  signal F1,F2: std_logic_vector(3 downto 0);
  signal saida: std_logic_vector(6 downto 0);

  component C1
      port (A: in std_logic_vector(3 downto 0);
            B: in std_logic_vector(3 downto 0);
            C: in std_logic;
            F: out std_logic_vector(3 downto 0)
           );
   end component;
   component C2
      port (A: in std_logic_vector(3 downto 0);
            B: in std_logic_vector(3 downto 0);
            F: out std_logic_vector(3 downto 0)
           );
   end component;
   component C3
      port (A: in std_logic_vector(3 downto 0);
            B: in std_logic_vector(3 downto 0);
            F: out std_logic_vector(6 downto 0)
           );
   end component;

begin     -- BEGIN da architecture

   auxA <= SW(3 downto 0);
   auxB <= SW(7 downto 4);

   U1: C1 port map (auxA, auxB, SW(9), F1);
   U2: C2 port map (auxA, auxB, F2);
   U3: C3 port map (F1, F2, saida);

   LEDR(6 downto 0) <= saida;
   HEX0 <= saida;

end topo_bhv;    -- END da architecture
```

```
-- C1.vhd (expressoes logicas e mux)
library IEEE;
use IEEE.Std_Logic_1164.all;

entity C1 is
port (A: in std_logic_vector(3 downto 0);
      B: in std_logic_vector(3 downto 0);
      C: in std_logic;
      F: out std_logic_vector(3 downto 0)
     );
end C1;
architecture c1_bhv of C1 is
begin
  F <= (A or B) when C = '1' else
       (A and B);
end c1_bhv;
```

```
-- C2.vhd  (expressao logica)
library IEEE;
use IEEE.Std_Logic_1164.all;

entity C2 is
port (A: in std_logic_vector(3 downto 0);
      B: in std_logic_vector(3 downto 0);
      F: out std_logic_vector(3 downto 0)
     );
end C2;
architecture c2_bhv of C2 is
begin
  F <= A xor B;
end c2_bhv;
```

```
-- C3.vhd  (decodificador)
library IEEE;
use IEEE.Std_Logic_1164.all;

entity C3 is
port (A: in std_logic_vector(3 downto 0);
      B: in std_logic_vector(3 downto 0);
      F: out std_logic_vector(6 downto 0)
     );
end C3;
architecture c3_bhv of C3 is
begin
  F <= "1001000" when A = "0000" else
       "0000011" when B = "0000" else
       "0000110";
end c3_bhv;
```