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"Vending machine"

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Florianópolis, August 2020.

Additional task
A controller for a vending machine

Case study: A controller for a vending machine

by Prof. Ney Calazans

Design the control circuit (FSM) to manage the operations of a vending machine.

Description:

The machine supplies two types of sodas, called MEET and ETIRPS. They are available for the customer to choose by pushing one of the two keys on the panel with the name of the sodas. Both sodas cost $1.50 and there is a slot in the machine to insert coins with an electromechanical system capable of recognizing coins of $1.00, $0.50 and $0.25, and capable of automatically returning any other type of currency or unrecognized object. In addition, during the purchase, the customer can withdraw from the transaction and press the DEV button that returns the coins inserted so far. Only after accumulating a minimum credit of $1.50 the user can obtain a soda. The return of excess coins is automatic whenever the amount entered before obtaining a soda exceeds $1.50. Also, the exact composition of the coins inserted in the machine can be ignored, taking into account only the total amount inserted.

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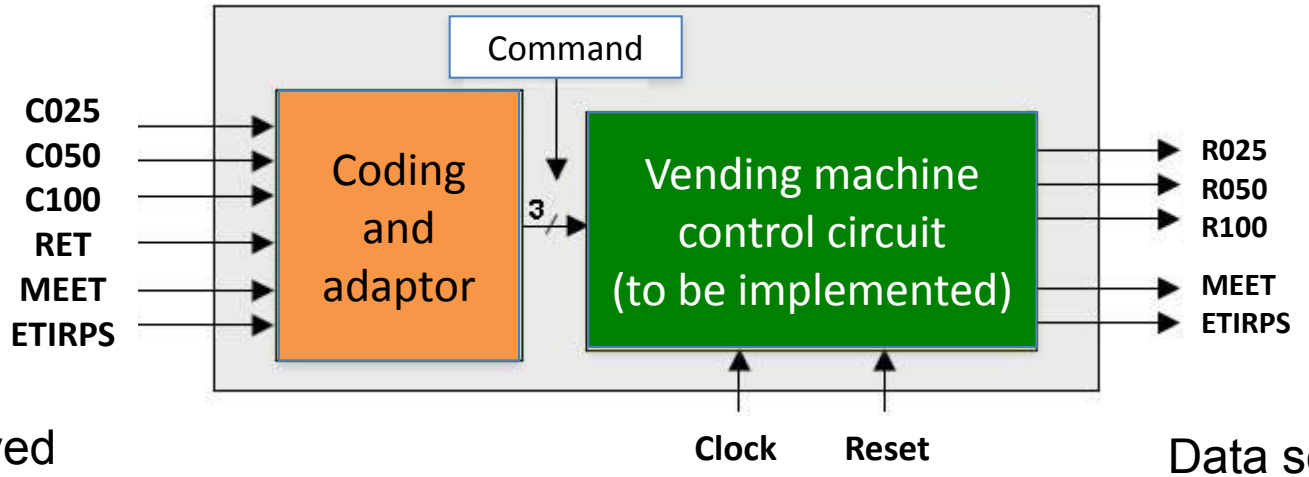
Solution: Block diagram



Data received from sensors

Data sent to the electromechanical actuators

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Solution: States table

Current state	Input command						
	Nothing	C025	C050	C100	RET	MEET	ETIRPS
S000		S025			S000	S000	
S025		S050			S000, R025		
S050						S050	
S075							
S100	S100			S150, R050			
S125							
S150							

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Solution: The 5 steps in the controller design (Frank Vahid)

FSM design – design an FSM to model the controller's behaviour.

Architecture definition – create an FSM's standard architecture, with a register to store the states, and a combinational logic responsible for generating the outputs and the next state (from the inputs and current state values).

State coding – Define a unique identification for the states.

Create the states table – Create the truth table for the combinational logic, in order to generate the proper values for the outputs and next state.

Combinational logic implementation.

When using VHDL for the FSM description, the 1, 2 or 3 processes approaches, will model the hardware behaviour according to these 5 design steps. The synthesis tool will generate the digital circuit for the modelled FSM.