



Designing with Quartus II



Class Agenda

Design Methodology in Quartus[®] II

- Exercise 1
- Projects
- Compilation
 - Exercise 2
- Single & Multi-Clock Timing Analysis
 - Exercise 3 &4
- Simulation
 - Exercise 5
- Programming/Configuration







Designing with Quartus II

Introduction to Altera & Altera Devices



The Programmable Solutions Company[®]



INNOVATION

Introduction to Altera Devices

- Programmable Logic Families
 - High & Medium Density FPGAs
 - Stratix[™] II, Stratix, APEX[™] II, APEX 20K, & FLEX[®] 10K
 - Low-Cost FPGAs
 - Cyclone[™] & ACEX[®] 1K
 - FPGAs with Clock Data Recovery
 - Stratix GX & Mercury[™]
 - CPLDs
 - MAX[®] 7000 & MAX 3000
 - Embedded Processor Solutions
 - Nios[™], Excalibur[™]
 - Configuration Devices
 - EPC









Introduction to Altera Design Software



Software & Development Tools:

– Quartus II

- Stratix II, Stratix, Stratix GX, Cyclone, APEX II, APEX 20K/E/C, Excalibur, & Mercury Devices
- FLEX 10K/A/E, ACEX 1K, FLEX 6000, MAX 7000S/AE/B, MAX 3000A Devices

- Quartus II Web Edition

- Free Version
- Not All Features & Devices Included

- MAX+PLUS® II

• All FLEX, ACEX, & MAX Devices









Designing with Quartus II

Quartus II Development System Feature Overview



Quartus II Development System

Fully-Integrated Design Tool

- Multiple Design Entry Methods
- Logic Synthesis
- Place & Route
- Simulation
- Timing & Power Analysis
- Device Programming



More Features

- MegaWizard[®] & SOPC Builder Design Tools
- LogicLock[™] Optimization Tool
- NativeLink[®] 3rd-Party EDA Tool Integration
- Integrated Embedded Software Development
- SignalTap[®] II & SignalProbe[™] Debug Tools
- Windows, Solaris, HPUX, & Linux Support
- Node-Locked & Network Licensing Options
- Revision Control Interface



What's New in Quartus II 4.0

- SOPC Builder
- LogicLock[™] Block-Based Methodology
- Assignment Editor
- Creating & Validating I/O Assignments
- IP Cores
- Integrated Synthesis
- Scripting
- Block Design Entry & Documentation
- MAX+PLUS® II Project Conversion



Quartus II Operating Environment





Main Toolbar & Modes



To Reset Views: Tools ⇒Toolbars>Reset All; Restart Quartus II

20 YEARS of





Designing with Quartus II

Design Methodology



PLD Design Flow



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PLD Design Flow









Designing with Quartus II

Design Entry



Design Entry Methods

Quartus II

- Text Editor
 - AHDL, VHDL, Verilog
- Memory Editor
 - HEX, MIF
- Schematic Design Entry
- 3rd-Party EDA Tools
 - EDIF
 - HDL
 - VQM

Mixing & Matching Design Files Allowed



Design Entry Files



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Text Design Entry

- Available Features
 - Line Numbering in the HDL Text Files
 - Preview of HDL Templates
 - Syntax Coloring
 - When Editing a Text File, an Asterisk (*) Appears Next to the Filename
 - Asterisk Disappears after Saving the File
- Enter Text Description
 - AHDL (.TDF)
 - VHDL (.VHD)
 - Verilog (.V)



Verilog & VHDL

VHDL- VHSIC Hardware Description Language 1987 & 1993 IEEE 1074 Standards Supported Verilog - 1995 & 2001 IEEE 1364 Standard HDL

- Create in Quartus II or any Standard Text Editor
- Use Quartus II Integrated Synthesis to Synthesize
- View Supported Commands in On-Line Help

Learn more about HDL in Altera HDL Customer Training Classes





- Altera Hardware Description Language
 - High-Level Hardware Behavior Description Language
 - Used in Altera Megafunctions
 - Uses Boolean Equations, Arithmetic Operators, Truth Tables, Conditional Statements, etc.
- Create in Quartus II or any Standard Text Editor



HDL Templates



Quartus II Options

Tools \Rightarrow **Options...**

ategory:	
Aregory: General Cicense Setup Programmer DA Tool Options DA Tool Options Disck/Symbol Editor General Colors Fonts Chip Editor General Colors Fonts Floorplan Editor General Colors Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts Fonts	 General Be-open current project and files at startup Show recently used files and projects on submenus Show 5 ≟ recently used files and projects Prompt to add files to project Default file location: Show introductory pages in wizards Display status bar Display toolbar buttons in menus Automatically name MegaWizard Plug-In output files and use the current output format
 □- Hesource Property Editor □- General □- Colors □- General □- General □- View □- Colors □- Fonts □- Printing □- Text Editor □- General 	



Schematic Design Entry

- Full-Featured Schematic Design Capability
- Schematic Design Creation
 - Draw Schematics Using Library Functions (Blocks)
 - Gates, Flip-flops, Pins & Other Primitives
 - Altera Megafunctions & LPMs
 - Create Symbols out of Verilog, VHDL, or AHDL Design Files
 - Connect All Blocks Using Wires & Busses
- Schematic Editor Uses
 - Create Simple Test Designs to Understand the Functionality of an Altera Megafunction PLL, LVDS I/O, Memory, Etc...
 - Create Top-Level Schematic for Easy Viewing & Connection



Create Schematic





Insert Symbols





Connect Wires & Buses





Change Names & Properties



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Create Symbols



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Optional Block Design Entity





Megafunctions

Pre-Made Design Blocks

- Ex. Multiply-Accumulate, PLL, Double-Data Rate
- Benefits
 - Accelerate Design Entry
 - Pre-Optimized for Altera Architecture
 - Add Flexibility
- Two Types
 - Altera-Specific Megafunctions
 - Library of Paramerterized Modules (LPMs)
 - Industry Standard Logic Functions



MegaWizard Plug-In Manager



MegaWîzard® Plug-In

Eases Implementation of Megafunctions & IP





MegaWizard Examples





MegaWizard Output File Selection

- Default
 - HDL Wrapper File
- Selectable
 - HDL Instantiation
 Template
 - VHDL Component Declaration (CMP)
 - Quartus II Symbol (BSF)
 - Verilog Black Box





Memory Editor

Create or Edit Memory Initialization Files in Intel Hex (.HEX) or Altera-Specific (.MIF) Format

Design Entry

 Use to Initialize Your Memory Block (Ex. RAM, ROM) during Power-Up

Simulation

Use to Initialize Memory Blocks before Simulation



Create Memory Initialization File

File \Rightarrow New \Rightarrow Other Files tab

		PMif1*									
		Addr	+0	+1	+2	+3	+4	+5	+6	+7	_
	New	0	255	255	255	255	255	255	255	255	
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	AHDL Include File	32	255	255	255	255	255	255	255	255	
	Block Symbol File	40	255	255	255	255	255	255	255	255	
	Chain Description File	48	255	255	255	255	255	255	255	255	
	Memory Initialization File	56	255	255	255	255	255	255	255	255	
	SignalTap II File	64	255	255	255	255	255	255	255	255	
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		88	255	255	255	255	255	2,5	255	255	
		96	255	255	255	255	255	255	255	255	
		104	0	0	0	0	0	0	0	0	
		112	0	0	0	0	0	0	0	0	
		120	0	0	0	0	0	0	0	0	
		128	0	0	0	0	0	0	0	0	
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Change Options

View Options of Memory Editor

– View \Rightarrow Select from Available Options

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Edit Contents

Edit Contents of the Memory File

Save the Memory File as .HEX or .MIF File





Memory Size Wizard

Need to Edit Size of Memory File?

Use the Memory Size Wizard (Edit Menu)

- Edit Word Size
- Edit Number of Words
- Specify How to Handle Word Size Change
 - Increasing Word Size
 - Pad Words
 - Combine Words
 - Decreasing Word Size
 - Truncate Words from Left
 - Truncate Words from Right



Using Memory File in Design

Specify MIF or HEX file in MegaWizard Interface





Memory Compiler

- Memory Functions are Organized by Type
- MegaWizard is Family-Aware
 - Select Memory Type & Parameters
 - Appropriate
 Megafunction Selected
 Automatically





FIFO Partitioner

- Map Multiple FIFOs into a Single Physical Memory Block
- Partition M-RAM Blocks into Multiple FIFOs

MegaWizard Plug-In Manager - FIFO partitioner	(page 1 of 5)	Jump to page for	X Global Ontions		
$\begin{array}{c c} \hline my_fifos \\ \hline wr_data_a_0[70] & rd_data_b_0[70] \\ \hline wr_en_a_0 & wr_empty_0 \\ \hline read_b_0 & wr_full_0 \\ \hline clk_port_a_0 & rd_empty_0 \\ \hline clk_port_b_0 & rd_full_0 \\ \hline FIFO0 & 8 bits x 128 words \\ \hline wr_data_a_1[70] & rd_data_b_1[70] \\ \hline wr_ead_b_1 & wr_empty_1 \\ \hline read_b_1 & wr_empty_1 \\ \hline clk_port_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & wr_full_1 \\ \hline clk_port_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & d_bits x 128 words \\ \hline wr_data_a_1[70] & a bits x 128 words \\ \hline wr_data_a_1[70] & d_bits x 128 words \\ \hline wr_data_a_1[70] & rd_data_b_1[70] \\ \hline wr_empty_1 & mr_empty_1 \\ \hline clk_port_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & rd_bundta_s x 128 words \\ \hline wr_data_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & a bits x 128 words \\ \hline wr_data_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & a bits x 128 words \\ \hline wr_data_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & a bits x 128 words \\ \hline wr_data_a_1 & rd_empty_1 \\ \hline clk_port_b_1 & a bits x 128 words \\ \hline wr_data_a_1 & rd_b_a words \\ \hline wr_data_a_a words \\ \hline wr_a_a_a_a words \\ \hline wr_a_a_a_a_ & words _a words \\ \hline wr_a_a_a_a_ & words _a words \\ \hline wr_a_a_a_a_ & words _a_a & words & words \\ \hline wr_a_a_a_a_ & words & words & words & words \\ \hline wr_a_a_a_ & words & words & words & words & words & words $	Global Configurations How many FIFOs would you like? 2 Use the same configuration for all virtual elements Make the asynchronous clear active low	RAM Status Virtual Element 0 FIFO 1 FIFO	Write Read 1.00 1.00 1.00 1.00		
tdm_clk aclr Total bits used: 2048		Write bandwidth Read bandwidth The minimum TDM RAM bits used	2 MHz 2 MHz 1 TDM clock rate is 3.00 MHz. 2048 / 524288 bits		
-		Cancel	<u> </u>		



Memory Behavioral Waveforms

- HTML file Generated by MegaWizard
- Description of Memory Functionality
 - Reviews Selected Parameters
 - Describes Read & Write Operations



Example Memory Waveform





EDA Interfaces Introduction

- Interface with Industry-Standard EDA Tools that Generate a Netlist File
 - EDIF 200
 - VHDL '87 or '93
 - Verilog
- NativeLink Interface Provides Seamless Integration with 3rd-party EDA Software Tools
 - Tools Pass Information/Commands in Background
 - Designers Can Complete Entire Design in One Tool



NativeLink

Comprised of Two Components

- External Files
 - WYSIWYG (What You See Is What You Get) ATOM Netlist Files (EDIF, Verilog, VHDL)
 - Cross Reference Files (Ex. XRF)
 - Timing Files (Ex. SDO)
- Application Programming Interface (API)
 - Pre-Defined Interface of Commands/Functions





WYSIWYG ATOM Primitives

- Set of Design Primitives that Support WYSIWYG Compilation
- Provide Direct Control of How a Design Is Technology-Mapped to a Specific Target Device
- Allow Synthesis Vendors to Provide an Optimal Realization of a Design for Each Architecture

00104 stratix lcell par err high 0 and2 62 Z (.combout(par err high 0 and2 62), 00105 00106 .dataa(ram out c 11), Synplify .vgm 00107 .datab(ram out c 10), 00108 .datac(ram out c 9), 00109 .datad(ram_out c_8) 00110); 00111 defparam par err high_0_and2_62_Z.operation_mode="normal"; 00112 defparam par err high 0 and2 62 Z.lut mask="9669"; 00113 defparam par err high 0 and2 62 Z.synch mode="off"; 00114 defparam par err high 0 and2 62 Z.sum lutc input="datac";



WYSIWYG Compilation Flow



48

Three EDA Design Flows

Quartus II Driven Flow

- User Launches other EDA Tools from Quartus II in the Background
- Messages Appear in Quartus II Message Window
- Vendor Driven Flow
 - User Runs Quartus II in the Background from the 3^{rd-} Party EDA Tool
- File Based Flow
 - Each Tool Ran Separately
 - Files Are Manually Transferred between Tools



Quartus II Driven Flow

Assignments \Rightarrow EDA Tool Settings



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EDA Driven Flow





File Based Flow

Work Separately in Individual Tools

- Synthesis
- Simulation
- Timing Analysis
- Board-Level
- Formal Verification
- Resynthesis





Third Party Tool Support

Synthesis Tools

- LeonardoSpectrum[™]
- Precision
- DesignCompiler
- FPGA Compiler II[™]
- FPGA Express[™]
- Synplify
- Synplify Pro
- Amplify

Verification Tools

- ModelSim[®]
- ModelSim-Altera
- Cadence Verilog-XL
- Cadence NC-Verilog
- Cadence NC-VHDL
- Innoveda BLAST
- PrimeTime[®]
- Synopsys[®] VCS & VSS
- Mentor Graphics[®] Tau
- Synopsys Scirocco



RTL Viewer

Graphically Represents Results of Synthesis





RTL Viewer Uses

- Visually Checking Initial HDL Synthesis Results
 - Before Any Quartus II Optimizations
- Locating Synthesized Nodes for Assigning Constraints
- Debugging Verification Issues
- Reading VQM/EDIF Netlist Files



Starting RTL Viewer

- Run Analysis & Elaboration (Processing 1. Menu or 🔽)
 - Any Processing that Performs Elaboration
- 2. Open RTL Viewer
 - Tools Menu or



Displays Last Successful Compilation



RTL Viewer Features

- Schematic View
- Hierarchy List
- Hierarchy Navigation
- Filter Schematic
- Page Control



Schematic View



- Represents Design Using Logic Blocks & Nets
 - Registers
 - Muxes
 - Gates
 - Adders



Hierarchy List

- Traverses between Design Hierarchy
- Views Logic Schematic for Each Hierarchical Level
- Breaks down Design into Netlist Elements



Netlist Elements

Instances

 Lower Hierarchy Levels that Can Be Expanded (Unless Encrypted)

Primitives

 Low-level Nodes/Blocks that Cannot Be Expanded

Pins

 I/O Ports in the Current Level of Hierarchy

Nets

Nets or Wires that Connect Nodes





Using Hierarchy List





Hierarchy Navigation

- Hierarchy List
 - 1. Click on Netlist Element (Ex. Instance)
 - 2. Schematic View Automatically Adjusts Hierarchical Level to Show Element
- Schematic View
 - Mouse Pointer Indicates Action
 - Descending Hierarchy
 - Double-Click on Instance
 - Right-Click & Select Hierarchy Down
 - ← Ascending Hierarchy
 - Double-Click in Empty Space
 - Right-Click & Select Hierarchy Up



Filter Schematic

Unfiltered: All Components & Paths Shown

Filtered: Only Selected Components & Related Paths Displayed



63

Filter Options



Between Selected Nodes





More on Filtering

- Displays Only Nodes on Current Hierarchy Level
- Stops Tracing Paths at
 - Hierarchical Ports
 - Registers
 - Option to Disable (Tools Menu \Rightarrow Options)
 - Specified Number of Logic Levels
 - 10 by Default (Tools Menu \Rightarrow Options)



Page Control

- Schematic Automatically Partitioned
- Option to Control Design Size Per Page (Tools Menu ⇒ Options)
 - Nodes Per Page
 - 1 1000 (Default: 50)
 - Ports Per Page
 - 1 2000 (Default: 1000)



Managing Pages

Title Bar Indicates Number of Pages



- Moving between Pages
 - Next Page/Previous Page
 - Moves between Partitioned Pages
 - Back/Forward
 - Displays Previously Viewed Design Views



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F

Nets between Pages

- Indicated by Special I/O Connectors
- Right-Click to Trace within Hierarchy
 - From Page (Source)
 - To Page (Destination)
 - Related (Other Parallel Connections)



Other Features

- Go to Net Driver
 - Traces Net Back to Source Driver
 - Changes Schematic View if Necessary
- Locate in Design File
 - Finds Node Definition in Source File



Exercise 1

Please go to Exercise 1 in the Exercise Manual



Exercise Summary

- Schematic Design Entry is Simple
- MegaWizard Makes It Easy
 - Implements Many Design Entities in AHDL, Verilog, or VHDL
 - Makes Best Use of the Device Architecture
 - Has Direct Link to Make IP Downloads Even Easier
- Analysis & Elaboration Option Checks the File



Summary

- Multiple Design Entry Methods
 - Text (Verilog, VHDL, AHDL)
 - Third Party Netlist (VQM, EDF)
 - Schematic
- Memory Editor
- MegaWizard
- EDA Tool Flows
- RTL Viewer






Designing with Quartus II

Quartus II Projects



Quartus II Projects

Description

- Collection of Related Design Files & Libraries
- Must Have at Least One Designated Top-Level Entity
- Target a Single Device or Can Be Partitioned into Multiple Devices
- Store Settings in Quartus Settings File (.QSF)
- Create New Projects with New Project Wizard
 - Can Be Created Using Tcl Scripts



New Project Wizard





Add Files

New Project Wizard: Add Files [page 2 of 6]	Add Design Files
Select the design files and software source files you want to include in your project. Click Add All to add all design files and software source files in the project directory. Note: it is optional to add files here unless you have design files not contained in the project directory, or files in which the file name is not the same as the entity name. File name:	 Graphic (.BDF, .GDF) AHDL VHDL Verilog EDIF
Properties Up Down	<u>Notes:</u> Files in project directory do not need to be added Add top level file if filename & entity name are not the same
If your project includes libraries of custom functions, specify their pathnames:	
Back Next Finish Cancel	Add User Library Pathnames & Files



User Libraries

Add User Library Paths

- User Libraries
- MegaCore®/AMPP Sm Libraries
- Pre-Compiled VHDL Packages

User Library Pathnames

Add any non-default libraries that you will use in the project. List the library names in the order you want to search them. Custom libraries can contain user-defined or vendor-supplied megafunctions, Block Symbol Files, AHDL Include Files, and pre-compiled VHDL packages.

ibrary name:	Add
Libraries: c:\megacore\fit.compiler.v2.5.0\lib	Hemove
c. (megacore (m_compile)-vz.0.0 MD	Up
	Down
ОК	Cancel



EDA Tool Settings

DA tools			
Tool type	Tool name		
Design entry/synthes	s <none></none>		
Simulation	<none></none>		
Fiming analysis	<none></none>		
30ard-level Formal vorification	<nune></nune>		
Besynthesis	<none></none>		
Tool settings			
Tool type: D	esign entry/synthesis		
Tool name:	<none></none>		
Run this tool auto	matically to synthesize the current desi	gn Settings	
		Advance	ed

Choose EDA Tools

Add or Change **Settings Later**



Device Selection

New Project Wizard: Device Family [page 4 of 6]	
Which device family do you wish to target?	
Do you want to assign a specific device? • Yes • No. I want to allow the Compiler to choose a device	
 No, I want to allow the complicit to choose a device 	Choose the Device Family
R	
	Auto Device or Choose a Specific Device
Back Next Finish Cancel	



Device Selection





Done!

friend you block i mitting your prop	
Project directory:	
c:/test_designs/memory/me	mory_test_4_0/
Project name:	Lab6_QII
Top-level design entity:	Lab6_QII
Number of files added:	0
Number of user libraries added:	0
EDA tools:	
Design entry/synthesis:	<none></none>
Simulation:	<none></none>
Timing analysis:	<none></none>
Board design:	<none></none>
Device assignments:	
Family name:	Stratix II
Device:	EP2S15F484C3

Review Results & Click on Finish



MAX+PLUS II to Quartus II

- Convert MAX+PLUS II Projects into Quartus II Projects
- Assignments Automatically Translated

File Edit View Project	Assignments	Proc
☐ Mew ☐ Open Close	Ctrl+C Ctrl+F4	Convert MAX+PLUS II Project
- New Project <u>W</u> izard Open P <u>r</u> oject Convert MAX+PLUS <u>I</u> I	Ctrl+: Project	This will create a new Quartus II project based on selected MAX+PLUS II project, and import the MAX+PLUS II project MAX+PLUS II project file:
Save Projec <u>t</u> Clos <u>e</u> Project		D:\max2work\chiptrip\chiptrip.acf
		Quartus II project name:
		chiptrip
		OK Cancel



Assignments Menu

- Accesses All Assignments & Settings
- Opens Settings Dialog Box

Settings - pipemult		
Category:		
; General		
Files		
User Libraries		
- Device		
- Timing Requirements & Options		
EDA Tool Settings		
- Design Entry & Synthesis		
Simulation		
- Timing Analysis		
- Board-Level		
- Formal Verification		
Resynthesis		
 Compilation Process 		
🚊 Analysis & Synthesis Settings		
VHDL Input		
Verilog HDL Input		
- Default Parameters		





Editing Project Settings

Open Existing Project First to Edit Settings



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Editing Project Settings (cont.)

• Assignments \Rightarrow Settings

tings - pipemult			
ategory:			
General	Files		
Files	Calast the desire files and soft		
Device	design files and software source	e files in the project directory to the project.	t. The Quartus II software
Timing Bequirements & Options	automatically detects relevant	design files and software source files that a	already exist in the project
= EDA Tool Settings	directory and adds them to the	project. You should add any design files r me file name as the entity name	not stored in the project
- Design Entry & Synthesis	or nics and do not have the sy	ine ne name as the entry name.	
Simulation		1	
Timing Analysis	File name	Туре	Add
Board-Level			IIA bbA
- Formal Verification			
			Remove
- Analusis & Sunthesis Settings			
- VHDL Input			Up
Verilog HDL Input			Down
Default Parameters			
Synthesis Netlist Optimizations			Properties
- Fitter Settings			
Physical Synthesis Optimizations			
Timing Analyzer			
Design Assistant SignalTap II Logic Analyzer			
- SignalProbe Settings			
- Simulator			
- Software Build Settings			
Stratix GX Registration			
HardCopy Settings			
			OK Cancel
			Cancer

Change Settings

- Rename
- Add/Remove Files
- Libraries
- VHDL '87, '93?
- Verilog '95, '01?
- EDA Tool Settings
- Timing Settings
- Compiler Settings
- Simulator Settings



Project Navigator – Hierarchy Tab



- Displays Project Hierarchy after Project Is Analyzed
- Uses
 - Set Top-Level Entity
 - Make Assignments
 - Locate in Design Files,
 Floorplan or Chip Editor
 - View Resource Usage
 - Drag & Drop
 Hierarchical Blocks



Project Navigator – Files Tab

🐝 Quartus II - C:/guartus4_0/gdesigns/fir_filter/con
File Edit View Project Assignments Processing Tools
🛛 🗅 🖆 🖬 🎒 👗 🖻 🛍 🗠 🗠 💦 🤰
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
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mult.v
w accum.v
Remove File from Project
sub.td
http://www.internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationality.com/internationalit
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📓///libraries/megafunctions/multcore.tdf
A/./libraries/megafunctions/mpar_add.tdf
Software Files
• •
🛆 Hierarchy 🖹 Files 🗗 Design Units

Shows All Files in Project

> All Source Files Appear under Design Files

Uses

- Open Files
- Remove Files from Project
- Set New Top-Level Entity



Project Navigator - Design Units Tab

- Displays each Design Unit & Type
 - VHDL Entity
 - VHDL Architecture
 - Verilog Module
 - AHDL Subdesign
 - Block Diagram Filename
- Details the File which Instantiates Design Unit

Quartus II - C:/quartus4_0/qdesigns/fir_filter/compile/compile_fi File Edit View Project Assignments Processing Tools Window Help		
🔁 Design Units		
🚊 🚾 a_csnbuffer (AHDL entity)		
🔄 🔝///libraries/megafunctions/a_csnbuffer.tdf		
ecc (Verilog HDL entity)		
acc.v		
erreilog HDL entity)		
accum.v		
addcore (AHDL entity)		
「「」」「「」」、「」、「」、「Ibraries/megafunctions/addcore.tdf		
Silve College discussion of the second section of the sectio		
Entrer (block diagram/schematic enticy)		
Interioul		
Harris Invalues (Veniog NDL entity)		
E mar add (AHDL entity)		
Error mpar_add (Arroc endry)		
The rest carding the state of t		
electraneseys termination of Testop Redefect 1.		
Hierarchy 🖹 Files 🗗 Design Units		



Project Files

Quartus Project File (QPF)

- Quartus II Version
- Time Stamp
- Active Revision
- Quartus Default File (QDF)
 - Project Defaults
 - Name: assignment_defaults.qdf
 - Local or Bin Directory
 - Local Read First



Project Archive & Restore



Archive Project Creates: 1. <project>.QAR • Compressed Archive File • Options to Choose which Files Get Archived 2. <project>.QARLOG • Log of Archive Activity Restore Archived Project:

> Restores Complete Project & Library Function Files from
> <project>.QAR File



Summary

- Use Project Wizard to Create New Projects
- Use Assignments Menu Dialog Boxes to
 - Edit Existing Project Settings
 - Edit Third-Party Tools
- Use Project Navigator to Study File & Entity Relationships within Project







Designing with Quartus II

Quartus II Compilation



Quartus II Compilation

- Synthesis
- Fitting
- Generating Output
 - Timing Analysis Output Netlist
 - Simulation Output Netlists
 - Programming/Configuration Output Files



Controlling Synthesis & Fitting

- Two Methods to Control Logic Synthesis & Fitting Operations
 - Settings
 - Project-Wide Switches
 - Assignments (i.e. Logic Options; Constraints)
 - Individual Entity/Node Controls



Settings

Examples

- Device Selection
- Pin Assignments
- Synthesis Optimization
- Fitter Optimization
- Physical Synthesis
- Located in Settings Dialog Box (Assignments Menu)



Editing Settings



Assignments \Rightarrow Settings

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Several Options Control Compilation & Device Options



Device Selection

		Device & Pin Options
Settings - pipemult	X	Dual-Purpose Pins Voltage Pin Placement
Category:		General Configuration Programming Files Unused Pins
Category: General Files User Libraries Device Timing Requirements & Options EDA Tool Settings Cosign Entry & Synthesis Simulation Timing Analysis Board-Level Formal Verification Resynthesis Compilation Process Analysis & Synthesis Settings VHDL Input Verilog HDL Input Oefault Parameters Synthesis Netist Optimizations Fitter Settings Fitter Settings Fitter Settings Signal Tap II Logic Analyzer Signal Tap II Logic Analyzer Signal Probe Settings Simulator	Device Select the family and device you want to target for compilation. Family: Stratix II Target device • Auto device selected by the Fitter from the 'Available devices' list • Specific devices selected in 'Available devices' list • Other: n/a Available devices: EP2515F484C3 (Advanced) EP2515F484C4 (Advanced) EP2515F484C4 (Advanced) EP2515F672C3 (Advanced) EP2515F672C4 (Advanced) EP2515F672C5 (Advanced) EP2530F484C4 (Advanced) EP2515F672C3 (Advanced) EP2530F484C4 (Advanced) EP2515F672C3 (Advanced) EP2530F484C5 (Advanced) EP2530F484C5 (Advanced) EP2530F6872C5 (Advanced) EP2540F6872C5 (Advanced) EP2540F6872C	General Contiguration Programming Files Unused Pins Specify general device options. These options are not dependent on the configuration scheme. Options: Auto-restart configuration after error Release clears before thi-states Enable device-wide reset (DEV_CLRn) Enable device-wide output enable (DEV_OE) Enable device-wide output Generate compressed bitstreams Auto usercode JTAG user code (32-bit hexadecimal): FFFFFFf* Description: Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to restart the configuration process if an error occurs. Reset DK Cancel
	Migration compatibility: 0 migration devices selected Migration Devices	Specify Device & Pin Options • General • Configuration • Programming Files • Unused Pins • Dual Purpose Pins • Voltage
	Migration Devices	20 YEARS of
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97

Compilation Process

Category:		
General Files User Libraries Device Timing Requirements & Options	Compilation Process Specify Compilation Process options. Use Smart compilation	
 EDA Tool Settings Compilation Process Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Synthesis Netlist Optimizations Fitter Settings Timing Analyzer Design Assistant 	 ✓ Preserve fewer node names to save di (This option is available for both Norma) ✓ Save a node-level netlist into a persiste File name: 	sk space I and Smart compilation) ent source file (Verilog Quartus Mapping File)
 SignalTap II Logic Analyzer SignalProbe Settings Simulator Software Build Settings Stratix GX Registration HardCopy Settings 	Ŀ3	Smart Compilation – Used for Incremental Re-Compilation – Saves Compiler Time
		 Uses More Disk Space Preserve Node Names Disable for VHDL (Varilage Symthesis)



Synthesis Options

Settings - filtref					
Category:					
General	Analysis & Synthesis Settings				
Files User Libraries	Specify options for analysis & synthesis. Note: The availability of some options depends on the current device family.				
 Timing Requirements & Options EDA Tool Settings Compilation Process Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Synthesis Netlist Optimizations Fitter Settings Physical Synthesis Optimizations Timing Analyzer Design Assistant Signal Tap II Logic Analyzer Signal Probe Settings Simulator Software Build Settings Stratix GX Registration HardCopy Settings 	Optimization Technique	for IP cores ment ng Auto Auto	Auto Global Options (MAX Devices Only) Clock Output Enable Register Control Signals Auto Open-Drain Pins Auto Parallel Expanders Auto Shift Register Replacement Power-Up Don't Care		
	More Settings Description: Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.				





Synthesis Netlist Optimizations

- Further Optimize Netlists during Synthesis
- Types
 - WYSIWYG Primitive Resynthesis
 - Gate-Level Register Retiming



WYSIWYG Primitive Resynthesis

- Unmaps 3rd-Party Atom Netlist Back to Gates & then Remaps to Altera Primitives
 - Unavailable when Using Integrated Synthesis
- Considerations
 - Node Names May Change
 - 3rd-Party Synthesis
 Attributes May Be Lost
 - Preserve/Keep
 - Some Registers May Be Synthesized Away



4-5 % Improvement



Gate-Level Register Retiming

- Moves Registers across Combinatorial Logic to Balance Timing
- Trades between Critical & Non-Critical Paths
- Makes Changes at Gate Level





Enabling Synthesis Optimizations



Created/Modified Nodes Noted in Compilation Report



Fitter Optimizations

	Settings - filtref	
	Category:	
Timing Driven Compilation• Optimize Internal Timing• Optimize I/O Register PlacementCompilation Speed/Fitter Effort• Standard Fit (Highest Effort)• Fast Fit (Faster Compile but Possibly Lesser Design Performance)• Auto Fit (Compile Stops after Meeting Timing)• One Fitting AttemptSeed• Controls Initial Placement Configuration	 General Files User Libraries Device Timing Requirements & Options EDA Tool Settings Compilation Process Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Synthesis Netlist Optimizations Fitter Settings Physical Synthesis Optimizations Timing Analyzer Design Assistant SignalT ap II Logic Analyzer SignalTor Build Settings Stratix GX Registration HardCopy Settings 	Fitter Settings Specify options for fitting. Note: The availability of some options depends on the current device family and Fitter. Timing-driven compilation



Physical Synthesis

Re-Synthesis Based on Fitter Output

- Makes Incremental Changes that Improve Results for a Given Placement in Altera Device
- Compensates for Routing Delays from Fitter
 - Routing Delays Large Part of Typical Critical Path Delay

Types

- Combinational Logic
- Registers
 - Register Duplication
 - Register Retiming



Combinational Logic

Swaps Look-Up Table (LUT) Ports within LEs to Reduce Critical Path LEs



Allows LUT Duplication to Enable Further Optimizations on the Critical Path



Register Duplication

High Fan-Out Register Is Duplicated & Placed to Reduce Delay

Combinational Logic May Also Be Duplicated



Enabling Physical Synthesis



Created/Modified Nodes Noted in Compilation Report


More Netlist Optimizations Info

- Disable Optimizations on Specific Entities/Nodes
 - Set Netlist Optimizations Logic Option to Never Allow
 - Entities/Nodes Cannot Be Altered
- Prevent Nodes from Being Optimized Away
 - HDL Attributes
 - Use **PRESERVE** (Registers) or **KEEP** (Combinational Logic)
 - Preserve Logic Option
- Unsafe Registers & Logic Remain Unaffected
 - Registers with Certain Timing Constraints
 - Registers that Feed Clocks, Asynchronous Controls
 - Registers Fed by Registers in Other Clock Domains



Processing Options

- Start Compilation
 - Perform Full Compilation
- Start Analysis & Elaboration
 - Check Syntax & Build Database Only
- Start Analysis & Synthesis
 - Synthesize Code & Estimate Timing
- Start Fitter
- Start Assembler
- Start Timing Analysis
- Start I/O Assignment Analysis
- Start Design Assistant







Status & Message Windows



Hit the Start Button

File Edit View Project Assignments Processing Tools Window Help		×
Image: Second	Image: Second	Successful - Wed Dec 03 17:11:55 2003 pipemult pipemult Stratix II 62 77 44 / 343 (12 %) 512 / 419,328 (<1 %) 0 / 96 (0 %) 0 / 6 (0 %) 0 / 2 (0 %) EP2S15F484C3 80 / 12,480 (<1 %)
Info: ************************************	× × • • • • • • • • • • •	× ×

Status Bars Scroll to Indicate Progress

Message Window Displays Informational,

Warning, & Error Messages



Compilation Report



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Resource Usage

pipemult Compilation Report										
🖗 🔄 Compilation Report 🛛 🔤	-	Inp	out Pins							
🗃 🖹 Legal Notice			Name	Pin #	1/O Bank	X coordinate	Y coordinate	Cell number	Combinational Fan-Out	Registered Fan
- 🚭 🖽 Flow Summary		1	clk1	X0_Y10_N1	1	0	10	1	1	0
Flow Settings		2	dataa[0]	X40_Y8_N2	6	40	8	2	8	0
Flow Elapsed Time		3	dataa[1]	X40_Y8_N0	6	40	8	0	8	0
		4	dataa[2]	X40_Y9_N2	6	40	9	2	8	0
Analysis & Synthesis		5	dataa[3]	X40 Y9 N1	6	40	9	1	8	0
		6	dataa[4]	X40 Y7 N3	6	40	7	3	8	0
		7	dataa[5]	X40 Y10 N0	6	40	10	0	8	0
Analysis & Synthesis B		8	dataa[6]	X40 Y10 N3	6	40	10	3	8	0
👍 🚓 🗛 🗛 🗛 🗛 🗛 🗛		9	dataa[7]	×40 Y7 N0	6	40	7	0	8	0
🚽 🗃 🔠 Analysis & Synthesis Fi		10	datab[0]	X40 Y10 N2	6	40	10	2	8	0
🗃 🎹 Analysis & Synthesis R		11	datab[1]	X40 Y10 N1	6	40	10	1	8	0
🚽 🗃 Analysis & Synthesis R.		12	datab[2]	X40 Y9N3	6	40	9	3	8	0
🗄 🚭 🦲 Analysis & Synthesis O		12	datab[2]	VAD V9 100	c	40	9	0	0	0
Analysis & Synthesis M		14	datab[3]	V40_13_N0	c	40	7	1	0	
Fitter		14		X40_17_N1	c	40	7	2	0	0
Fitter Summary		10	datab[0]	X40_17_N2	0	40	0	1	0	0
Fitter Settings		10	datab[6]	240_18_N1	0	40	0	1	0	0
Av-h Eitter Equations		17	datab[/]	X40_Y8_N3	6	40	8	3	8	
		18	rdaddress[U]	X40_Y24_N1	5	40	24	1	1	
		19	rdaddress[1]	X35_Y27_N2	4	35	27	2	1	0
Fitter Resource Us.		20	rdaddress[2]	X40_Y24_N0	5	40	24	0	1	0
Input Pins		21	rdaddress[3]	X40_Y25_N2	5	40	25	2	1	0
Output Pins		22	rdaddress[4]	X37_Y27_N3	4	37	27	3	1	0
- 🚑 🎹 I/O Bank Usage		23	wraddress[0]	X40_Y24_N2	5	40	24	2	1	0
- 🗃 🛄 Output Pin Load Fc		24	wraddress[1]	X37_Y27_N2	4	37	27	2	1	0
Fitter Resource Uti		25	wraddress[2]	X37_Y27_N0	4	37	27	0	1	0
Delay Chain Summa		26	wraddress[3]	X35_Y27_N1	4	35	27	1	1	0
Pad To Core Delay		27	wraddress[4]	X35_Y27_N0	4	35	27	0	1	0
Control Signals		28	wren	X40_Y24_N3	5	40	24	3	1	0
E A LAB and Routing St										
Fitter Messages]					
						Sever	al Secti	ons De	etail the Res	ource I
Assembler Summary						501010				
- 🚑 🎹 Assembler Settings										
🔄 🖅 Assembler Messages 📘	-									
		┛								<u> </u>



Floorplan



- Available Views
 - Last Compilation
 - Chip Editor
 - Timing Closure
- Uses
 - Make Assignments
 - View Placement
 - View Connections



Floorplan View





Assignments

- Assignment Editor
- Example Assignments
- I/O Assignments & Analysis

Perform Analysis & Elaboration before Obtaining Hierarchy & Node Information



Assignment Editor (AE)

Provides Spreadsheet Assignment Entry & Display

- Can Copy & Paste from Clipboard

	Node Filter:	Show assignments for	specific nodes:					Check All Uncheck All Delete All
rt o	n Co	This cell specifies wheth	er or not the assignment is	processed by the Compiler.				Enable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable/Disable
2		Source Name (From)	Destination Name (To)	Option	Value	Settings File	Enabled	Comment
×	1	i∎≥dk	irrlkx2	Multicycle	2	filtref.esf	Yes	
	2		I D clk	Clock Settings	clocka	filtref.esf	Yes	
	3		international contraction of the second seco	Clock Settings	clockb	filtref.esf	Yes	
	4		🐼 yn_out	Current Strength	Strength 16mA	filtref.esf	Yes	
	5		💿 yvalid	Current Strength	Min Strength	filtref.esf	Yes	
	6		🐼 yn_out	Termination	Series	filtref.esf	Yes	
	7		iii∂d	I/O Standard	GTL+	filtref.csf	Yes	
	8		🐼 yn_out	I/O Standard	2.5 V	filtref.csf	Yes	
	9		💿 yvalid	I/O Standard	LVTTL	filtref.csf	Yes	
	10		iiiid	Location	IOBANK_1	filtref.csf	Yes	
	11		🗇 yn_out	Location	IOBANK_2	filtref.csf	Yes	
	12		💷 yvalid	Location	Pin_A5	filtref.csf	Yes	
	13	< <new>></new>	< <new>></new>	< <new>></new>				
	12	< <new>></new>	yvalid < <new>></new>	Location < <new>></new>	Pin_A5 Displays File Wh	Filtref.csf	Yes	

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Opening Assignment Editor

File Edit View	Project Assignments Processing Tools Window	v ł
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	<u> </u>	Ľ
Entity	Logic Cells Registers Memory Bits D	SP
🔄 Compilation	n Hierarchies	
+- v pipemu	Settings Compiler Settings Wizard Simulator Settings Wizard	
	Assignment Editor	
	Locate in Timing Closure Floorplan Locate in Last Compilation Floorplan Locate in Chip Editor Locate in Design File	
	Create New LogicLock Region Export LogicLock Regions	Ŀ
	Print Properties	×
Module Processing Tot	✓ Enable Docking Restrict to Main Window Close	

Invoke the Assignment Editor by Highlighting an Entity in the Hierarchy View & Right- Clicking





Opening Assignment Editor (cont.)

Locate to Assignment Editor from Timing Report, Messages, Etc





Using Assignment Editor

.≍ Cat	All Locations Pin							Source Name	Destination N	Option	Value
g	LAB						1	_	sys_clk	Clock Settings	sys_clk
7	Logic cell					<u> </u>	2	_	♦ dqs	DQS Frequency	6.024N
	Cource Name	Destination N	Ontion	Value	2		3	-	♦ dqs	DQS Phase Shif	t Phase of
	Source Marile	Destination N		value			4	-	≪ aqs	DQS Input Ref	. SYS_C
							5	-	✓ uq[0]	I/O Stanuaru	SSIL-2
1		sys_ck	Clock Settings	sys_clk				-	♦ dq[1]	I/O Standard	SSTL-2
2		🔷 dqs	DQS Frequency	6.024NS				-	♦ dq[2]	I/O Standard	SSTL-2
3		🔷 dqs	DQS Phase Shift	Phase of 90 d			9	-	♦ dq[0]	I/O Standard	SSTL-2
•	1	🔷 das	DOS Input Ref	SYS CLK			10		♦ dq[5]	I/O Standard	SSTL-2
8	1	♦ da[0]	I/O Standard	SSTL-2 Class II			11		\$\overline{4} dq[6]	I/O Standard	SSTL-2
5	1		I/O Standard	SSTL-2 Class II			12		dq[7]	I/O Standard	SSTL-2
,	1		I/O Standard	SSTL-2 Class II			13		🔷 dqs	I/O Standard	SSTL-2
	1		I/O Standard	SSTL-2 Class II			14	< <new>></new>	< <new>></new>		·
	1		I/O Standard	SSTL-2 Class II							
0	1	♦ dq[5]	I/O Standard	SSTL-2 Class II						Add to LogicLoc	k Region
1		♦ dq[6]	I/O Standard	SSTL-2 Class II						Alias	on oupu
.2			I/O Standard	SSTL-2 Class II						Auto Carry Chai	ins
.3		das	I/O Standard	SSTL-2 Class II						Auto DSP Block	Replacen rk
14	< <new>></new>		Node Finde	r						Auto Global Mer Auto Global Reg Auto Open-Drai Auto Packed Re Auto RAM Repla Auto Shift Regis Carry Chain Len CLKLOCKX1 Inou	mory Con gister Con gisters acement ster Repla gth Sti ut Freque
	/									Clock Settings	arri oquo
					•					Current Strengt Cut Timing Path	
ou	ble-Cl	ick Ce	lls	L	aunches					Decrease Input Decrease Input	Delay to Delay to
	dit or	۸dd			lada Eindar					Decrease Input	Delay to
		Auu			Node Finder			/		DOS Innut Refe	rence Clo
~	/ Accid	anmon	+								

of 90 d.. K Class II t Waveforms nent ntrol Signals ntrol Signals Stratix acement ratix ency Input Register Internal Cells -- Stratix Output Register

Selecting an Option Determines which Fields Are Available for Editing

Assignment Editor*

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Locations

20 YEARS of

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Entering Assignments

Other Ways to Edit Cells

- Single-Click & Type Name Directly
 - Useful for Known Node Names
- Edit Menu
- Edit Bar 🖌

		🎸 Assign	nment Editor*								×
		≚ ± Ca	ategory: All					💌 🔂 All	🗈 Pin 🛛 💍 Timi	ing 🔹 Logic Options	
		× - I	Show assignments for s	specific nodes:							
		Node Filter:								Check All Uncheck All Delete All	
	8	비 Ec	formation: Specifies t	he I/O standard of a pin. O Standard	Different device famili	ies support different I/O sta	indards, and restrictio	ons apply to placing	g pins with differen	t I/O standards togethe	dit Bar
	-		Source Name (From)	Destination Name (To)	Option	Value	1				
	9	10	Source Name (From)	Descination Name (10)	Location	Dip V16					1
	2	11	-		Location						
	1.414	12	4	■ d[0]	Location	Pin_AC16					
		13	1	₩d[3]	Location	Pin_AC9					
		14		■ d[2]	Location	Pin T4					
		15		■ d[1]	Location	Pin W9					
		16			Location	PIN C1					
				∲ me	Reserve Pin	As input tri-stated					
Edit Ba	r R	utto	n	wn out	tco Requirement	5ns					
		ullu		₽ d[3]	I/O Standard	LVTTL					
		20	< <new>></new>	< <new>></new>	< <new>></new>						20 YEARS of

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INNOVATION

Editing Multiple Assignments

- Edit Multiple Constraints Simultaneously
 - Select Multiple Pins & Use Edit Bar (Click Check Mark to Accept)

×	Information: Specifie	s the I/O standard of a	pin. Different device f	amilies support different I/	O standards, and restriction	is apply to placing p	oins with a	different I/O standarc	ls toge
×	Edit: 🗙 🗸	2.5 V							-
	Name	Location	I/O Bank	1) 0 Sta ndard	tsu Requirement	Clock Settings		tco Requirement	Cui
1	d∎	IOBANK_6	6	1.8 V					
2	newt	IOBANK_8	8	2.5 V	5.2ns				
3	💿 next	IOBANK_7	7	1.8 V				4ns	
4	reset	EDGE_BOTTOM		1.8 V					
5	💿 yn_out[0]	IOBANK_1	1	2.5 V			Ear	ting multip	
6	💿 yn_out[1]	IOBANK_1	1	2.5 V			Sta	ndards at	Ond
7	vn_out[2]	IOBANK_1	1	2.5 V					
8	💿 yn_out[3]	IOBANK_1	1	2.5 V					
9	vn_out[4]	IOBANK_1	1	2.5 V					_
10	🔿 yn_out[5]	IOBANK_1	1	2.5 V					_
11	🔿 yn_out[6]	IOBANK_1	1	2.5 V					
12	💿 yn_out[7]	IOBANK_1	1	2.5 V					
13	💿 yvalid	Pin_B18	3	2.5 V					
14	■ Pclk	Pin_A4	4	1.8 V		clocka			
15	■ clkx2	Pin_A5	4	1.8 V		clockb			
_	2 Coours	< <pre>c<peixi>></peixi></pre>							









Creating a Custom Filter

					Select Customize	
Node Finder						
Named data*	_ Eilt	er: Pins: all		Qustomize Start OK		
Look (top)				💭 🔽 Include subentities 🛛 Stop		
Nodes Foun <u>d</u> :			Selected N	odes:		
Name	Assign Type	Creato	Name	Assign Type Creato		
data_out	Unassig Output .	Usere	🗇 top dat	Customize Filter 🔀		
<pre> data_out[0] data_out[1] </pre>	Unassig Output	User e		Films		
or data_out[2]	Unassig Output	User e		Einer: OK		
@data_out[3]	Unassig Output	User e		[my_filter	New Custom Filter 🛛 🔀	
๗ data_out[4]	Unassig Output	User e		View		
<pre> data_out[5] </pre>	Unassig Output	User e		C Ourrent accignments Delete	<u>Filter name:</u>	
@ data_out[6]	Unassig Output	Usere			mu filted	
odata_out[7]	Unassig Output	User e		Last compilation New		
@data_out[9]	Unassig Output	User e >>			Copy settlogs from filter:	
@data_out[10]	Unassig Output	User e		Use netlist	Copy settings from filter. Cancel	
🗇 data_out[11]	Unassig Output	Usere 🔽		Pre-synthesis	Pins 🗾	
data_out[12] data_out[12]	Unassig Output	Usere <<		Show only SignalTap II names		
<pre>@ data_out[13]</pre>	Unassig Output	User e	1	C Post-synthesis		_
data_out[15]	Unassig Output	Usere		C Pastifing		
@data_out[16]	Unassig Output	User e		· <u>Fostilang</u>		
@ data_out[17]	Unassig Output	User e		Show only Signal Lap II and Signal Probe names	N	
				Show hames matching	CIICK NEW.	
				Assignments	Nome Filter 8	
		Þ	•	C Assigned (positional)	Name Filler &	
				C Unassigned (no positional assignments)		
				C All	CIICK OK.	
				Type	\mathbf{N}	
				✓ Input pins ✓ Begistered		
				Combinatorial		
				Bidirectional pins Memory bit		
				Virtual input pins Memory word	Select Filter	
				Virtual output pins		
					Settings	
				I Groups & buses I Aij	Cottingo	
				Creator		
				User-entered		
				Compiler-generated		
					20 YEARS of	
Converse ht @		0.0000	tion			Λ
Copyright ©	2003 Altera	Corpora	uon			Ъ, И(

AE Dynamic Checking

Validity of Constraint Checked during Entry Color-Coded to Display Status

Grev – Assignment

INNOVATION

	Destination Name (To)	Option	Value	Settinas File	Enabled	
>clk	■ clkx2	Multicycle	2	filtref.esf	No	
	i i i i i i i i i i i i i i i i i i i	clock Settings	 CIOCNA	nicer.est	105	Black – Assig
	in allow?	Cleak Sattings	eloelite	filtrof.cof	Yes	Is Applied
	💿 yvalid	Current Strength	Min Strength	filtref.esf	Yes	
		East Output Enable Pegister	05	Filtrot oct	Var	
	Fred2	Fast Output Register	On	filtref.esf	Yes	
	[™] yn_out	njo standard	2.5 V	nicref.csi	res	Vollow Mr
	🐵 yvalid	I/O Standard	LVDS	filtref.csf	Yes	
	iiiid	Location	IOBANK_1	filtref.csf	Yes	Assignment
_	ave_out	Location	TOBANK_2	Filtrof ccf	Ver	Not Be Valic
	ii≥cl k	Location		filtref.csf	Yes	
-		Location		filtref.csf	res	
	₽ d[0]	Location		filtref.csf	Yes	
	₽ d[1]	Location		filtref.csf	Yes	Dark Da
	▶d[2]	Location		filtref.csf	Yes	Dark Red
	iiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	Location		filtref.csf	Yes	Assignm
	1	Location		Filtrof. ccf	Voc	Incomple
< <new>></new>	< <new>></new>	< <new>></new>				· · ·

125





Displays Information on Selected Cell

Can Be Hidden or Minimized

		Category:	Pin					🕶 🔽 All 🖻 Pin 💍	Timing 🔹 Logic Options
a	异, 봄 -	Show assignments	s for specific nodes:						
	_ z	D 🔎 d							Check All
U	💷 🛱								Unahaali All
l f	3月 끝								
	<u> </u>								Delete All
	.13 × -	Sets the drive stren	gth of a pin. Specific nur	merical strength settings (2, 4, 8, 12, 16, or 24 mA)	are appropriate only for pi	ns with LVTTL, LVCMC)5, 1.8-V, or 2.5-V I/O stand	ards. This option is 🛛 💈
		ignored if it is applie	d to anything other than	an output or bidirectiona	l pin.				
	8 주								
	🔛 mat								
	🝦 🛛 İn:								
	<u>ه اللہ</u>								
		Name	Location	I/O Bank	I/O Standard	General Function	Reserved	Current Strenath	Termination
	x Information	n bar	IOBANK 1	1	GTL+			-	
	2	🗇 vn out	IOBANK_2	2	2.5 V			Strength 16mA	Series
	3		Pin_A5	4	LVTTL	Column I/O		Min Strength	
olbar Button	3	vyvalid vyvalid	Pin_A5	4	LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5	yvalid clk clkx2	Pin_A5	4	LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6		Pin_A5	4	LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7	Image: wide wide wide wide wide wide wide wide	Pin_A5	4	LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8	Image: Control of the second	Pin_A5	4	LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9	yvald ck ck ck d(0) d(1) d(2) d(3)	Pin_A5	4	LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9 10	• yvalid • clk • clkx2 • d(0) • d(1) • d(2) • d(3) • d(4)	Pin_A5	4	LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9 10 11	yvaid vaid vaid	Pin_A5		LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9 10 11 12	Image: clk x2 Image: clk x3 <td>Pin_A5</td> <td></td> <td>LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL</td> <td>Column I/O</td> <td></td> <td>Min Strength</td> <td></td>	Pin_A5		LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9 10 11 11 12 13	Image: Constraint of the second sec	Pin_A5		LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9 10 11 11 12 13 14	yyald yyald w clkx2 w clxx2 w d(0) w d(1) w d(2) w d(3) w d(5) w d(5) w d(6) w d(7) w newt	Pin_A5	4	LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	
olbar Button	3 4 5 6 7 8 9 10 11 11 12 13 14 15	yyald yyald w clkx2 w clkx2 w d(0) w d(1) w d(2) w d(3) w d(3) w d(4) w d(5) w d(6) w d(6) w d(7) w newt w next	Pin_A5	4	LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL LVTTL	Column I/O		Min Strength	



AE Node Filter Bar



- Enables/Disables Selective Filtering of Constraints Displayed Based on Node Name
- Can Be Hidden or Minimized

)	Node F	Show assignments for s	specific nodes:					Check All
	ilter:	formation: Allows you	u to view and edit assignr	ments for specific nodes and entite	s. Specify one or more node or enl	tity names, using one nam	e per row, to allow the	spreadsheet to filter the assign
ľ		Course Name (Even)	Destination Name (Ta)	Onting	Uniter	Cattings Tile	Eashlad	Comment
Ē	-	Source Name (From)	Destination Name (To)	Option Multicycle	Value 2	Settings File	Enabled	Comment
	7 1 2	Source Name (From)	Destination Name (To) Clkx2 Clkx2	Option Multicycle Clock Settings	Value 2 clockb	Settings File filtref.esf filtref.esf	Enabled Yes Yes	Comment
	7 1 2	Source Name (From)	Destination Name (To) Clkx2 Clkx2 Clkx2 d	Option Multicycle Clock Settings I/O Standard	Value 2 clockb GTL+	Settings File filtref.esf filtref.esf filtref.csf	Enabled Yes Yes Yes	Comment
	7 1 2	Source Name (From)	Destination Name (To) Clkx2 Clkx2 d d d	Option Multicycle Clock Settings I/O Standard Location	Value 2 clockb GTL+ IOBANK_1	Settings File filtref.esf filtref.esf filtref.csf filtref.csf filtref.csf	Enabled Yes Yes Yes Yes Yes	Comment
	7 1 2 5	Source Name (From)	Destination Name (To) Clx2 Clx2 d d clx2 d clx2 clx2 clx2 d clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 c	Option Multicycle Clock Settings I/O Standard Location Location	Value 2 clockb GTL+ IOBANK_1	Settings File filtref.esf filtref.esf filtref.csf filtref.csf filtref.csf filtref.csf	Enabled Yes Yes Yes Yes Yes Yes	Comment
	▼ 1 2 5 6	Source Name (From) ™ clk	Destination Name (To) Clx2 Clx2 d d clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 clx2 c	Option Multicycle Clock Settings I/O Standard Location Location	Value 2 clockb GTL+ 1OBANK_1	Settings File filtref.esf filtref.esf filtref.csf filtref.csf filtref.csf	Enabled Yes Yes Yes Yes Yes Yes Yes	Comment



AE Category Bar



Selects Category of Assignments to View

- Ex. Pin Assignments, Timing Assignments
- Can Be Hidden or Minimized

	Category:	All Locations Pin I/O Bank Edge LAB Logic cell M512 M4K							
12		Source Name (From)	Destination Name (To)	Option	Value	Settings File	Enabled	Comment	
	1	🗈 clk	irrila and the second	Multicycle	2	filtref.esf	Yes		
13	2		🗩 clk	Clock Settings	clocka	filtref.esf	Yes		
	3		iiii iiii iiii iiii iiii iiiii iiiii iiii	Clock Settings	clockb	filtref.esf	Yes		
2			🐼 yn_out	Current Strength	Strength 16mA	filtref.esf	Yes		
T T	3		💿 yvalid	Current Strength	Min Strength	filtref.esf	Yes		
9	6		💿 yn_out	Termination	Series	filtref.esf	Yes		
2	7		íр€d	I/O Standard	GTL+	filtref.csf	Yes		
	8		🐼 yn_out	I/O Standard	2.5 V	filtref.csf	Yes		
	9		🐵 yvalid	I/O Standard	LVTTL	filtref.csf	Yes		
	10			Location	IOBANK_1	filtref.csf	Yes		
	11	Foolbar Butto	n p_out	Location	IOBANK_2	filtref.csf	Yes		
	12		valid	Location	Pin_A5	filtref.csf	Yes		
	13	8	ID clk	Location		filtref.csf	Yes		



AE Customizable Columns

- Each Category Has a Set of Customizable Columns
 - Ex. Include Common Timing Assignments in Pin Category
- Comment Column for Each Assignment

Customize Columns			×
Customize the columns for the Pin category			
Available columns:		Show these columns in this order:	
Special Function X Coordinate Y Coordinate Index Clock Settings tco Requirement th Requirement tsu Requirement tsu Requirement	▲ ≥ >> ✓ ✓	Name Location I/O Bank I/O Standard General Function Reserved Current Strength Termination	OK Cancel
Settings File SignalProbe Clock SignalProbe Source Name SignalProbe Enabled	_		Move <u>U</u> p Move <u>D</u> own



AE Tcl Commands

- Equivalent Tcl Commands Are Displayed as Assignments Are Entered
 - Manually Copy to Create Tcl Scripts
 - Export Command (File Menu) Writes All Assignments to a Tcl File

🎸 As	signment Editor*				
× +	Category:				
₩ +	Information: Assigns u:	ser-defined clock characte	ristics to a signal. To des	ionate a particula	r signal as a clock.
		1	1	1	
	Source Name (From)	Destination Name (To)	Option	Value	× i intervention
1		hvalues:inst2	Add to LogicLock Reg	. kdjff	J 🝈 🖬
2		👁 state_m:inst1	Add to LogicLock Reg	. kdjff	
3		iiii ⊂lkx2	Clock Settings	clk200	1 I 🕈 🖬
4		i∎>d[0]	Location	PIN_C1	1 I 🕈 🖫
5		iiii [1]	Location	Pin_W9	1
6		iiii d[2]	Location	Pin_T4	- III - 🕉 🖫
7		iiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	Location	Pin_AC9	- III - 🕉 🖫
8		iiii d[5]	Location	Pin_AC16	III 🕉 🖫
9		₽d[6]	Location	Pin_AD15	
10		₽d[7]	Location	Pin_Y16	1 II 🕺 🗒
11		🐵 yn_out[0]	Location	Pin_D20	38
12		🐵 yn_out[1]	Location	Pin_A21	- III - 🛪 🖱
13		🗇 yn_out[2]	Location	Pin_C21	1 🛛 🕺 🖱
14		🖤 yn_out[4]	Location	Pin_B20	1 II 🕺 🖞
15		wn_out	tco Requirement	5ns	_ <u>⊰</u> !!!
16		i 🕪 clk	Clock Settings	clk100	1 🛛 🕺 🖄
17			Location	Pin_E3	🔄 🛛 😤 Inf
18			Location	Pin_E4	🔄 🔍 🖓 İnf
110			Location	ING KA	Processing

20 YEARS of INNOVATION

Example Assignments

- Optimization Technique
- PCI I/O
- Output Pin Load



OPTIMIZATION TECHNIQUE

- Selects Synthesis Optimization Goal
 - Speed (Default)
 - Area
- Applies Only to Hierarchical Entities
- Effects Synthesis & Logic Mapping
- Only Applies to Quartus II Integrated Synthesis



PCI I/O

Turns on PCI Compatibility for Pins

- Ignored If Applied to Anything other than a Pin or a Top-Level Design Entity
- Controls Clamping
 Diode Located in the
 I/O Elements





Output Pin Load

Compilation Report	Out	tput Pin Load For Reported TCO		
E Legal Notice		1/D Standard	Load	Termination Resistance
Flow Summary	1	LVTTL	10 pF	Not Available
Flow Settings	2	LVCMOS	10 pF	Not Available
Flow Elapsed Time	3	2.5 V	10 pF	Not Available
Maiysis & Synthesis	4	1.8V	10 pF	Not Available
Fitter	5	1.5V	10 pF	Not Available
	6	GTL	30 pF	25 Ohm
	7	GTL+	30 pF	25 Ohm
and Fitter Equations	8	3.3-V PCI	10 pF	25 Ohm
🚽 🖉 🖉 Floorplan View	9	3.3-V PCI-X	8 pF	25 Ohm
- 🗃 Pin-Out File	10	Compact PCI	10 pF	25 Ohm
🗃 🔄 Resource Section	11	AGP 1X	10 pF	Not Available
Resource Usage Summary	12	AGP 2X	10 pF	Not Available
LogicLock Region Resource Usage	13	СТТ	30 pF	50 Ohm
	14	SSTL-3 Class I	30 pF	50 Ohm (Parallel), 25 Ohm (Seria
	15	SSTL-3 Class II	30 pF	25 Ohm (Parallel), 25 Ohm (Serial
	16	SSTL-2 Class I	30 pF	50 Ohm (Parallel), 25 Ohm (Serial
- 🚰 🛄 Output Pin Load For Reported TCO	17	SSTL-2 Class II	30 pF	25 Ohm (Parallel), 25 Ohm (Serial
Fitter Resource Utilization by Entity	18	SSTL-18 Class I	30 pF	50 Ohm (Parallel), 25 Ohm (Serial
- 🚭 🎹 Delay Chain Summary	19	SSTL-18 Class II	30 pF	25 Ohm (Parallel), 25 Ohm (Serial
Control Signals	20	1.5-V HSTL Class I	20 pF	50 Ohm
Global & Other Fast Signals	21	1.5-V HSTL Class II	20 pF	25 Ohm
I AR and Deutine Section	22	1.8-V HSTL Class I	20 pF	50 Ohm
	23	1.8-V HSTL Class II	20 nF	25 Ohm
	24	IVDS	4 nF	100 Obm
Timing Analyzer	25	Differential LVPECL	4 nF	100 Ohm
	26	3.3-V PCML	4 oF	50 Ohm
	27		4 nF	100.0bm
	20	Differential SETL 2 (PLL CLK, OUT aims only)	20 -5	(Con CCTL 2)

- Specifies Output Pin Loading in picoFarads (pF)
 - Changes Default Loading Value of I/O Standard
 - Changes t_{co} of Output Pins
- Allows Designer to Accurately Model Board Conditions
- Must Be Applied to Output or Bidirectional Pins



I/O (Pin) Assignments

- Make I/O Assignments Quickly
 - Assignment Editor
 - Settings Dialog Box (Device)
 - Scripting
 - Floorplan
- Specific Pin Location Unnecessary
 - IO Bank & Chip Edge Location Assignments
 - Reserved Pins with or without Locations



Assignment Editor I/O Assignments



INNOVATION



AE Show All Known Pin Names



Populate Spreadsheet with List of All Pin Names in Design

Assigned & Not Assigned

		Name	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved
周	1	🕩 d[0]	PIN_C1	2	LVTTL	Row I/O	DIFFIO_RX21p	
(2	i∎≥dk			LVTTL			
	3	ir alkx2			LVTTL			
	4	li∎id			LVTTL			
12	5	₽d[1]			LVTTL			
	6	₽d[2]			LVTTL			
	7	₽d[3]			LVTTL			
₽	8	IIII d[4]		2	LVTTL			0
	9	III d[5]			LVTTL			~
	10	₽d[6]			LVTTL			
5	11	₽d[7]	1		LVTTL			1
	12	newt			LVTTL	5	5	1
\$ II	13	next			LVTTL			
<u>í </u>	14	Preset			LVTTL			
	15	yn_out			LVTTL			
21	16	💿 yn_out[0]	2		LVTTL	-	~	
<u>/</u>	17	💿 yn_out[1]			LVTTL			
	18	💿 yn_out[2]			LVTTL			
	19	💿 yn_out[3]			LVTTL			
	20	💿 yn_out[4]		5	LVTTL			
	21	💿 yn_out[5]			LVTTL			
	22	💿 yn_out[6]			LVTTL			
	23	💿 yn_out[7]			LVTTL			
	24	💿 yvalid		2	LVTTL			2
	25	< <new>></new>	< <new>></new>					1.1



AE Assignable Pin Numbers



Show All Assignable Pin Numbers

 Populate Spreadsheet with All Pin Numbers Available for Assignment

111	0.000								
6		Name	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved	Sig
-	1	🗇 d[0]	PIN_C1	2	LVTTL	Row I/O	DIFFIO_RX21p		
	2		Pin_C1	2	LVTTL	Row I/O	DIFFIO_RX21p		
	3		Pin_D2	2	LVTTL	Row I/O	DIFFIO_RX21n		
	4		Pin_E3	2	LVTTL	Row I/O	DIFFIO_TX21p		
	5		Pin_E4	2	LVTTL	Row I/O	DIFFIO_TX21n		
日日	6		Pin_K4	2	LVTTL	Row I/O	DIFFIO_RX20p/RUP2		
I KI I	7		Pin_K3	2	LVTTL	Row I/O	DIFFIO_RX20n/RDN2		
	8		Pin_F3	2	LVTTL	Row I/O	DIFFIO_TX20p		
	9		Pin_F4	2	LVTTL	Row I/O	DIFFIO_TX20n		
	10		Pin_F1	2	LVTTL	Row I/O	DIFFIO_RX19p		
14	11		Pin_F2	2	LVTTL	Row I/O	DIFFIO_RX19n		
-8	12		Pin_G5	2	LVTTL	Row I/O	DIFFIO_TX19p		
	13		Pin_G6	2	LVTTL	Row I/O	DIFFIO_TX19n		
-8	14		Pin_G1	2	LVTTL	Row I/O	DIFFIO_RX18p		
0	15		Pin_G2	2	LVTTL	Row I/O	DIFFIO_RX18n		
X	16		Pin_G3	2	LVTTL	Row I/O	DIFFIO_TX18p		
0	17		Pin_G4	2	LVTTL	Row I/O	DIFFIO_TX18n		
2	18		Pin_K6	2	LVTTL	Row I/O	DIFFIO_RX17p		
T	19		Pin_K5	2	LVTTL	Row I/O	DIFFIO_RX17n	-	
	20		Pin_H3	2	LVTTL	Row I/O	DIFFIO_TX17p		
$ \checkmark $	21		Pin_H4	2	LVTTL	Row I/O	DIFFIO_TX17n		
2	22		Pin_L3	2	LVTTL	Row I/O	DIFFIO_RX16p		
1 M M	In the second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second second s second second seco								



AE Show I/O Banks in Color



Enable/Disable I/O Color Coding of Spreadsheet **Based upon Floorplan**

Assignment Editor*								
× ∏ ⊕ c	ategory: Pin				•	🕇 All 📄 Pin 👌 Timir	ng 🔹 Logic O	ptions
× ± Ir	formation: This cell s	pecifies the pin nam	e to which you want to n	nake an assignment.				
	Name	Location	I/O Bank	I/O Standard	General Function	Special Function	Reserved	-
1	🗇 d[0]	PIN_C1	2	LVTTL	Row I/O	DIFFIO_RX21p		
2	₽d[1]	Pin_W9	8	LVTTL	Column I/O	DQ7B1		
3	₽d[2]	Pin_T4	1	LVTTL	Row I/O	DIFFIO_RX5n		
4	III d[3]	Pin_AC9	8	LVTTL	Column I/O	DQ6B7		
5	III≥d[5]	Pin_AC16	7	LVTTL	Column I/O	PGM1		
6	III d[6]	Pin_AD15	7	LVTTL	Column I/O	RUnLU		
7	I → d[7]	Pin_Y16	7	LVTTL	Column I/O	nRS		
8	👁 yn_out[0]	Pin_D20	4	LVTTL	Column I/O	DQ1T2		
9	🖤 yn_out[1]	Pin_A21	4	LVTTL	Column I/O	DQS1T		
10	🗇 yn_out[2]	Pin_C21	4	LVTTL	Column I/O	DQ1T3		
11	🖤 yn_out[4]	Pin_B20	4	LVTTL	Column I/O	DQ1T4		
12		Pin_C1	2	LVTTL	Row I/O	DIFFIO_RX21p		
13		Pin_D2	2	LVTTL	Row I/O	DIFFIO_RX21n		
14		Pin_E3	2	LVTTL	Row I/O	DIFFIO_TX21p		
15		Pin_E4	2	LVTTL	Row I/O	DIFFIO_TX21n		
16		Pin_K4	2	LVTTL	Row I/O	DIFFIO_RX20p/RUP2		
17		Pin_K3	2	LVTTL	Row I/O	DIFFIO_RX20n/RDN2		
18		Pin_F3	2	LVTTL	Row I/O	DIFFIO_TX20p		
19		Pin_F4	2	LVTTL	Row I/O	DIFFIO_TX20n		
20		Pin_F1	2	LVTTL	Row I/O	DIFFIO_RX19p		
21		Pin_F2	2	LVTTL	Row I/O	DIFFIO_RX19n		
22		Pin_G5	2	LVTTL	Row I/O	DIFFIO_TX19p		
23		Pin_G6	2	LVTTL	Row I/O	DIFFIO_TX19n		_
24		Pin_G1	2	LVTTL	Row I/O	DIFFIO_RX18p		-
1								•



Setting Dialog Box - Device

	Settings - filtref		×
	Category: General Files User Libraries Device Timing Requirements & Options EDA Tool Settings Compilation Process Analysis & Synthesis Settings - VHDL Input - Verilog HDL Input	Device Select the family and device you want to target for Family: Stratix Target device O Auto device selected by the Fitter from the 'A O Specific device selected in 'Available device	compilation. Device & Pin Options Routing Options wailable devices' list s' list
ign Pins		×	Assign Pins
Number of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the stress of the	ndard: Type: SignalProbe Source Na Row I/O Row I/O	me Enabled Status Clt	 Show in 'Available devices' list Package: Any Pin count: Any Pin Assignments I/O Standards Reserve Pins SignalProbe
Pin game: CIKI I/O standard: LVTTL Beserve pin (even if it does not exist in the design f As input tri-stated As input tri-stated As output driving ground As output driving an unspecified signal As SignalProbe output		uting Disable All SignalProbe Routing	OK Cancel
As bidirectional		OK Cancel	20 YEARS of (入) 日 中 の)/。



Drag & Drop I/O Assignments

Drag & Drop from Node Finder to Floorplan





I/O Assignment Problems

- I/O Selected & Verified Too Far into Design Cycle
- Variety of Complex I/O Standards on Single Device
 - Not All Supported on Every I/O Block
- I/O Placement Limitations
 - Current Strength
 - Single-Ended vs. Differential
 - Single-Ended vs. V_{ref}



I/O Assignment Solution

I/O Assignment Analysis Command

- Quickly Checks Legality of I/O Assignments
 - Checks All Assignments
 - Does Not Stop at First Failure
- Allows User to Identify & Correct Pin-Related Issues without Full Compilation
- Has Two Usages
 - Performing Legality Checks Based on User Reserved Pin Assignments with Partial or No Design Files
 - Performing Legality Checks Based on User I/O Assignments with a Complete Design



I/O Assignment Analysis

🧭 File Edit View Project Assignments	Processing Tools Window Help
🛛 🗅 🚅 🖬 🕼 🕼 🕼 🕼 🕼 🕼	🐨 Stop Processing Ctrl+Shift+C 📐 🕘 📗 🌚 🕨 🗞
💥 🤀 🔟 😰 📾 📰 🎨 📗 🎨 🤹	Start Compilation Ctrl+L Analyze Current File
Entity Logi Regi Mem	Start Start Analysis & Elaboration Compilation Report Ctrl+R Start Analysis & Synthesis Ctrl+K
Compliation Hier 	Start Compilation & Simulation Ctrl+Shift+K Generate Functional Simulation Netlist Start Assembler Start Simulation Ctrl+I Simulation Debug Start EDA Netlist Writer Simulation Report Ctrl+Shift+R
	Start Software Build Ctrl+Q Compile Current File
Hierarchy Files Pogress Time	Image: Start VQM Writer Image: Start VQM Writer Image: Start EDA Synthesis Image: Start EDA Resynthesis


I/O Analysis Requirements

I/O Declaration

- HDL Port Declaration
- Reserved Pin
- Pin-Related Assignments
 - I/O Standard
 - Current Strength
 - Pin Location (Pin, Bank, Edge)
 - PCI Clamping Diode
 - Toggle Rate



Legality Checks

Rule (subset of the rules)	Incomplete Design	Complete Design
Differential Pin Spacing		•
# of Output/Bidirs Toggling with a VREF		•
Blocks Directly Feeding or Fed by I/O pins		•
Current Strength	•	•
DC Current Draw	•	•
Pin Location	•	•
I/O Bank Capacity	•	•
Voltage Conflict (Vref, VCCIO)	•	•
On-Chip Termination	•	•



I/O Assignment Analysis Notes

Uses Toggle Rate Assignment

- Set Toggle_rate = 0 for Very Low Frequency Output Pins
- Allows Single Ended Pins to be Placed Closer to Differential Pins
- Invokes Smart Recompile for I/O Features
 - Delay Chains
 - Drive Strengths
 - Bus Hold



I/O Assignment Analysis Output

Detailed Messages on

- Incorrect I/O Assignments & Problem Description
- Compiler Assumptions that User did Not Specify
- Pins Changing Functionality with Pin-Migration
- Used I/O Standards & Voltages per I/O Bank
- Compilation Report (Fitter Section)
 - I/O Pin Tables
 - Show User & Fitter Assigned I/O
 - Shows Partial Placement Results in Floorplan to Help Debug Fitting Errors
- Messages Locate to Assignment Editor & Floorplan to Explain Placement Failure



I/O Assignment Analysis Messages



Example Error Message

× -	 Info: ************************************



Using I/O Assignment Analysis

- 1. Use Complete Design Files or Reserve Pins if Incomplete
- 2. Make Pin-Related Assignments
- 3. Start I/O Assignment Analysis
- 4. Review Report File for Errors
- 5. Modify & Correct Illegal Assignments, if Any
- 6. Re-Run Analysis until Errors Are Resolved
- 7. Back-Annotate Pins to Lock Locations



Quartus Settings File (QSF)

Stores All Settings & AssignmentsUses Tcl Syntax

pipemult.qsf*	
29	
30 # Project-Wide Assignments	
31 # ===================================	
32 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 4.0	
33 set_global_assignment -name PROJECT_CREATION_TIME_DATE "11:30:40 JANUARY 19, 2004"	
34 set_global_assignment -name LAST_QUARTUS_VERSION 4.0	
-35 Mar 104 Mar 104	
36 # Pin & Location Assignments	
37 #	
38 set_location_assignment IOBANK_2 -to aa ca	
39 set_location_assignment IOBANK_2 -to datab	
40	
41 set_location_assignment PIN_L2 -to clk1	
42 set_location_assignment PIN_F22 -to wren	
43 set_location_assignment PIN_L8 -to ~DATAO~ Organi	zed by Assignment Type
44	
45 # Timing Assignments	
46 # ===============	
47 set_global_assignment -name INCLUDE_EXTERNAL_PIN_DELAYS_IN_FMAX_CALCULATIONS OFF	
48	
49 # Analysis & Synthesis Assignments	
-50 #	
51 set_global_assignment -name FAMILY Stratix	
52 set_global_assignment -name DEVICE_FILTER_SPEED_GRADE ANY	
53 set_global_assignment -name TOP_LEVEL_ENTITY pipemult	
.54	
55 # Fitter Assignments	
56 # ===========	
57 set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_RETIMING ON	
58 set_global_assignment -name DEVICE EP1S10F484C5	
59 set_instance_assignment -name IO_STANDARD "2.5 V" -to dataa	
60 set_instance_assignment -name IO_STANDARD "2.5 V" -to datab	
61	
62 · #	
	20 YEARS

20 YEARS of

Design File Management

Project Archive & Restore

- Stores All Project Files
 - Design Files
 - Settings File
 - Output Files
- Revisions
 - Stores Only QSF
 - Allows Designer to Try Different Options



Creating a Revision

• Project \Rightarrow Revisions



Base Revision on Any Previous Revision

Treate Revision Specify a name and de You can base the revis	scription for the ne ion on an existing r	w revision. evision, and
Revision name:	filtref_new	
Based on revision: Description:	filtref filtref	_
	filtref_150 filtref_phys_syn	
Type Revi	<mark>sion Descrip</mark>	tion
Set as current revis	ion	
	ОК	Cancel
		20 YEARS of

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INNOVATION



Project Revision Support

Active Revision Names Stored in QPF

QSF Created for Each Revision

- <Revision_name>.QSF

Text File Created for Each Revision

-<Revision_Name>_description.TXT



INNOVATION

Compiling a Submodule

- 1. Create a New Revision
- 2. Disable "Based on revision"

Specifu a name an		
You can base the r specify the revision	as the acc as the Top-Level	les
Revision name:	acc	
Based on revision	on: filtref	
This is to compile a	submodule independently	
Set as current r	evision	

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- 1. Open Submodule File
- Select "Set as Top-Level Entity" from Project Menu

Quartus II - c	:/develo	ping_classe	s/adv_vhdl	/adv_vt
<u>File E</u> dit <u>V</u> iew	Project	Assignments	Processing	Tools
	Add Add, <u>R</u> evi	Curre <u>n</u> t File to /Remove <u>Files i</u> isions	Project n Project	
Entity Compilation	Arch Rest	iive <u>P</u> roject :ore Archi <u>v</u> ed P	roject	
• > cntr_m	<u>G</u> en Gen	erate Tcl File fo erate Po <u>w</u> er Es	or Project timation File	
	Hard	l <u>C</u> opy Utilities		•
	Loca	ite		+
	R Set	as Top-Level <u>E</u> r	ntity Ctrl+Shif	t+J
	Hier	archy		+

Reuses Current .QSF File



Exercise 2

Please go to Exercise 2 in the Exercise Manual



Exercise Summary

- Created Project
- Compiled Design
- Gathered Information from the Compilation Report
- Used Assignment Editor to Change Logic Usage
- Used I/O Analysis to Check I/O Placement



Compilation Summary

- Compiling a Design
 - Compiler Settings
 - Synthesis & Fitting Options
 - Compilation Report
- Assignments
 - Assignment Editor
 - I/O Assignment Analysis
- Managing Revisions







Designing with Quartus II

Timing Analysis



Features

- Built-In Static Timing Analysis
- Single & Multi-Clock Timing Analysis
- Standard & Minimum Timing Analysis
- Timing Export for Analysis in Another EDA Tool



Timing Analysis Agenda

- Single Clock Analysis
- Timing Assignments
 - Global & Individual
- Multi-Clock Analysis
- Multi-Cycle Analysis
- Minimum Timing



Running Timing Analysis

Automatically

- Use Full Compilation
- Manually
 - Processing Menu \Rightarrow Start \Rightarrow Start Timing Analysis
 - Tcl Scripts
 - Uses
 - Changing Speed Grade
 - Annotating Netlist with Delay Information



Timing Analysis

Prile Edit View Project Assignments Processing Tools Window Help	<u>- 8 ×</u>
D 😅 🖬 😂 X 🖻 🛍 🕫 ా 🖂 🕺 🕨 📐 📩 👜 🧶 🕀 😻 🕸 🚸	
🗙 ♦ 🖿 🎦 📾 🚍 😌 🚽 🕹 ♦ ♦ ♦ ♥ ♥ 🖉 ♥ 💈 🖉 😫	3 🕸 🖄 🥶
► 🐨 🕆 🕫 🖆 🍋 诸 🐝 🎽 😵 🦕 pipemult	
🖆 🛋 🖉 🔄 Compilation Report	Clock Setup: 'clk1'
Entity Logic Cells Registers Memory Bits Legal Notice	Slack Actual fmax (period)
Compilation Hierarchies	1 N/A 246.73 MHz (period = 4.053 ns)
i i pipemult 134 (0) 88 512 i i i i i i i i i i i i i i i i i i i	2 N/A 248.51 MHz (period = 4.024 ns)
i i i i i i i i i i i i i i i i i i i	e de = 3.983 ns)
altsyncram:altsyncr 0 (0) 0 512	
📄 🖻 🔿 multinst 🛛 134 (0) 🛛 88 🛛 0 🔄 🔂 🔂 Assembler	bd = 3.970 ns)
🗼 🗄 🗢 Ipm_mult:Ipm_mult 134 (0) 🛛 88 🛛 0 👘 🖓 🔂 Timing Analyzer	6 N/A 252.33 MHz (period = 3.963 ns)
Timing Analyze	rer Settings 7 N/A 252.78 MHz (period = 3.956 ns)
Timing Analyze	8 N/A 255.23 MHz (period = 3.918 ns)
Clock Setup: 'c	'dk1' 9 N/A 256.02 MHz (period = 3.906 ns)
	10 N/A 256.15 MHz (period = 3.904 ns)
	11 N/A 256.21 MHz (period = 3.903 ns)
Be Linux him B Film A Denim Links	12 N/A 256.28 MHz (period = 3.902 ns)
Timing Analyze	ter Messages 13 N/A 256.67 MHz (period = 3.836 hs)
	256.87 MHz (period = 3.893 ms)
Module Progress % Time © Fmax of All Cl	
Processing Total 100% 00:01:19	VCA 25/10/ MHz (period = 3.890 ns)
E-Full Compilation 100% 00:01:19 Automatically	N/A 208.33 MH2 (period = 3.87 i ns)
Analysis & Synthesis 100 % 00:00:16	N/A 259.60 MHz (period = 3.66/ ns)
Fitter 100% 00:00:54 Displayed in th	N/A 250.67 MHz (period = 3.655 ms)
Assembler 100 2 00:00:07 DISplayed III (1	KA 259.13 Mit2 [period = 3.053 ns] N/A 259.94 Mit2 [period = 2.047 ns]
Timing Analyzer 100 2 00:00:01 Message Wind	N/A 200.54 MHz (period = 2.94 km)
Wessage wind	N/A 200.13 MHz (period = 3.044 hs)
	24 N/A 20021 MHz (period = 3.043 ns)
	25 N/A 250.42 MHz (period = 3.64 ms)
	26 N/A 260.48 MHz (period = 3.839 ps)
	27 N/A 260.62 MHz (period = 3.837 ns.)
	28 N/A 260.62 MHz (period = 3.837 ps)
Compile Simulate	
 Info: Clock clk1 has Internal fmax of 246.73 MHz between source register multinstllpm_multipm_m Info: + Longest register to memory delay is 3.575 ns Info: + Micro clock skew is -0.212 ns Info: + Micro clock to output delay of source is 0.156 ns Info: + Micro clock to output delay of source is 0.110 ns Info: to register multinstllpm_multipm_mult_component[multcore:mult_core]decoder_node[4][5 Info: to form clock clk1 to destination pin q[1] through memory raminst1]altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:altsynctam:alt	mult_component multcore:mult_core mpar_add:padder mpar_add:sub_par_add drop_bits_node[1][1] and destination memory ra 5] (data pin = datab[4], clock pin = clk1) is 0.759 ns _component/ram_block(0][15]" portb_address_reg0 is 9.971 ns 1] (data pin = datab[3], clock pin = clk1) is 0.561 ns syncram_component/ram_block(0][15]" portb_address_reg4 is 9.384 ns

20 YEARS of INNOVATION

Reporting Timing Results

- Timing Analyzer Section of Compilation Report
 - Summary
 - Timing Analyses
 - Clock Setup (fmax)
 - Clock Hold
 - tsu (Input Setup Times)
 - th (Input Hold Times)
 - tco (Clock to Out Delays)
 - tpd (Pin to Pin Delays)
 - Minimum tpd & tco





Clock Setup (fmax)

Worst-Case Clock Frequency

- Without Violating Internal Setup & Hold Times







Clock Setup (fmax) Tables

						Fmax Valu	ues Are Lis	sted in Asc	ending) Orde	er;	
		Woi	rst f	max		Worst Fm	ax Is Liste	d on the To	ac			
	🗣 two_d_dct	Compilation Report										
F	🎒 🔄 Compilati	on Report	Cloc	k Setup: 'cl	lk'							
	- 🚑 🖹 Legal	Notice		Slack	Actual fr	nax (period)	From	To	From Clock	To Clock	Required Se 🔺	
	Flow Summary 1 N/A		231.11 MH	lz (period = 4.327 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None			
			2	N/A	231.96 MH	lz (period = 4.311 ns)	transport_matrix:tp	rowrow_dct_instl	clk	clk	None	
	Flow	Liapsed Lime	3	N/A	233.05 MH	lz (period = 4.291 ns)	transpose_maaiv:tp	row_dct:row_dct_instl	clk	clk	None	
		LUY voic 8: Supthecic	4	N/A	235.02 MH	lz (period = 4.255 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
	E - Analy	,	5	N/A	237.02 MH	lz (period = 4.219 ns)	transpose_matrix:tp	row_dat:row_dat_instl	clk	clk	None	
	+ Asser	mbler	6	N/A	238.72 MH	lz (period = 4.189 ns)	transpose_matrix:tp	row_dct:row_dct_instl	clk	clk	None	
	🗄 🚑 🔄 Timin	g Analyzer	7	N/A	238.95 MH	lz (period = 4.185 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
	Anning Analyzer Settings Analyzer Settings Analyzer Summary Analyzer Summary		N/A	239.06 MH	lz (period = 4.183 ns)	transpose_matrix:tp	row_dct:row_dct_inst	Sourc		stination		
			9	N/A	239.23 MH	lz (period = 4.180 ns)	transpose_matrix:tp	row_dct:row_dct_inst				
			10	N/A	239.52 MH	lz (period = 4.175 ns)	transpose_matrix:tp	row_dct:row_dct_inst	Registe	rs & A	ssociated	
			11	N/A	239.64 MH	lz (period = 4.173 ns)	transpose_matrix:tp	row_dct:row_dct_inst	Fr	nax Va	lues	
		su	12	N/A	239.87 MH	lz (period = 4.169 ns)	transpose_matrix:tp	row_dct:row_dct_inst				
			13	N/A	240.44 MH	lz (period = 4.159 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
0.0		inimum too	14	N/A	240.79 MH	lz (period = 4.153 ns)	transpose_matrix:tp	row_dct:row_dct_instl	clk	clk	None	
Se	iect	ming Analyzer Messages	15	N/A	241.02 MH	lz (period = 4.149 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
Clock	Setup		16	N/A	241.08 MH	lz (period = 4.148 ns)	data_valid_state~22	column_dct:col_dct_in	clk	clk	None	
	•		17	N/A	241.14 MH	lz (period = 4.147 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
			18	N/A	241.31 MH	z (period = 4.144 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
			19	N/A	241.60 MH	z (period = 4.139 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
			20	N/A	242.90 MH	z (period = 4.117 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
			21	N/A	243.13 MH	z (period = 4.113 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None	
			22	N/A	243.25 MH	z (period = 4.111 ns)	column_dct:col_dct	column_dct:col_dct_in	clk	clk	None	
L	×	•							-		► //.	



fmax Analysis

To Analyze the Path More Closely

two_d_dct Compilation Report	2015								
🗃 🔁 Compilation Report									
- 🗃 🖹 Legal Notice		Slack Actual fmax (period) From To From Cloc				From Clock	To Clock	Required Se 🔺	
Flow Summary				231.11 MHz (period = 4.327 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None
Flow Settings	2	N/A		231.96 MHz (period = 4.311 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None
Flow Elapsed Time	3	N/A	T	233.05 MHz (period = 4.291 ns)	transpose_matrix:tp	row_dct:row_dct_inst	clk	clk	None
	4	N/A	Τ	235.02 MHz (period = 4.255 ns)	1		- 1	clk	None
Haraysis & Synthesis	5	N/A	T	237.02 MHz (period = 4.219 ns)	Copy	Ctrl+0		clk	None
Assembler	6	N/A		238.72 MHz (period = 4.189 ns)	Select All Ctr		-д	clk	None
E analyzer	7	N/A		238.95 MHz (period = 4.185 ns)	🗸 Align Left		10.0	clk	None
Timing Analyzer Settings	8	N/A		239.06 MHz (period = 4.183 ns)	Align Right			clk	None
🛛 🎒 🎹 Timing Analyzer Summary	9	N/A		239.23 MHz (period = 4.180 ns)				clk	None
Clock Settings Summary	10	N/A		239.52 MHz (period - 4.175 m	List Paths			clk	None
Clock Setup: 'clk'	11	N/A		239.64 MHz (period = 4.173 ns)	Assignment Editor	Ctrl+5	5hift+A	clk	None
High	liah	it.		239.87 MHz (period = 4.169 ns)	Locate in Chip Edito	r		clk	None
Right Mous Selec		ick			Locate in Timing Clo	sure Floorplan			
					Locate in Last Comp	bilation Floorplan			
		se a			Save Current Report Section As				
		IST		-					
Path	S								

Similar Steps for All Timing Path Analysis in Quartus II



fmax Analysis Details



fmax Analysis Details (cont.)





Locate Delay Path in Floorplan





Locate Delay Path in Floorplan





Clock Hold Analysis

Checks Internal Register-Register Timing

- Report Occurs Only When Hold Violations Occur
- Results Usually When Data Delay (B) is Greater than Clock Skew (E-C)
 - Non-Global Clock Routing
 - Gated Clocks



Hold Time Violations Table



I/O Setup Time Analysis (tsu)



tsu = data delay - clock delay + intrinsic tsu



I/O Hold Time Analysis (th)



th = clock delay - data delay + intrinsic thold



I/O Clock-to-Output Analysis (tco)





I/O Timing Analyzer



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<u>Note</u>: Timing Analysis of tpd is similar



Timing Analysis Options

- Used to Limit which Paths Are Displayed
- Global Cut Timing Options (On by Default)
 - Cut Paths between Unrelated Clock Domains
 - Cut Off Feedback from I/O Pins (Next Slide)
 - Cut Off Clear & Preset Signal Paths
 - Cut Off Read during Write Signal Paths
- Timing Analyzer Options
 - Display Paths that Do Not Meet Timing Only



Cut Off Feedback from I/O Pin

Breaks Bidirectional I/O Pin from Analysis

- When On, Paths A & B Are Valid; C Is Not
- When Off, Paths A, B, & C Are Valid




Cut Options

Assignments \Rightarrow Settings \Rightarrow Timing Requirements & Options



Timing Analyzer Options

Assignments \Rightarrow Settings \Rightarrow Timing Analyzer

Settings - pipemult Category: General Files User Libraries Device Timing Requirements & Options EDA Tool Settings Design Entry & Synthesis Simulation Timing Analysis Board-Level Formal Verification Resynthesis Compilation Process Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Synthesis Netlist Optimizations Fitter Settings	Fining Analyzer Specify the range of information to be reported in the timing analyses included in the Compilation Report. Show 10 slowest destination registers per clock Show 200 worst-case paths in slack reports Exclude paths Exclude paths with fmax greater than: Exclude paths with slack greater than: Exclude paths with slack greater than: Exclude paths with slack greater than: Exclude paths with slack greater than: Exclude paths with tsu less than: The paths with the stant:
 Synthesis Netlist Optimizations Fitter Settings Physical Synthesis Optimizations Timing Analyzer Design Assistant SignalT ap II Logic Analyzer SignalProbe Settings Simulator Software Build Settings Stratix GX Registration HardCopy Settings 	Exclude paths with the less than: Image: Control in the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the set of the s



Single-Clock Timing Analysis

- Performed Automatically during Each Compile
- Detects Clocks Automatically If No Assignments Are Made
 - Single or Multiple Asynchronous Clock
 Domains
 - Still Important to Specify Clock Frequencies
- Displays Results in the Timing Analyzer Report



Exercise 3

Please go to Exercise 3 in the Exercise Manual



Exercise Summary

Single Clock Timing Analysis

List Timing Paths & View Details

Locate in Floorplan



Timing Assignments

VERY IMPORTANT!!

- Have a Major Impact on Design Compilation
 - Specify ALL Timing Requirements for Your Design
 - Fitter Works Hardest on the Worst Timing
 - Timing Will Be Reported in Red If Not Met
- Types
 - Internal & I/O Timing
 - Maximum & Minimum
- Can Be Assigned Globally or Individually
 - Individual Assignments Better



Timing Driven Compilation (TDC)

- Directs Fitter to Place & Route Logic to Meet Timing Assignments
 - Optimize Timing
 - Placing Nodes in Critical Paths Closer Together
 - Optimize I/O Cell Register Placement
 - Moving Registers into I/O Cells



Optimize Hold Timing

- Modifies Place & Route to Meet Hold or Minimum Timing Requirements
 - May Add Additional Routing in Path
 - Supported in Stratix II, Stratix, Stratix GX, Cyclone Devices

Settings



- Any I/O Paths
- All Paths (I/O & Internal)



Optimize Hold Time Examples





Global Clock Assignments

ttings - filtref	2	×	
Category:			
General Files User Libraries Device Timing Requirements & Options EDA Tool Settings Design Entry & Synthesis Simulation Timing Analysis Board-Level Formal Verification Resynthesis Compilation Process Analysis & Synthesis Settings VHDL Input VeriL Input Default Parameters Synthesis Netlist Optimizations	Timing Requirements & Options Specify timing requirements and options. Individual timing assignments can be made through the Assignment Editor. Delay requirements tsu: ns tco: ns tco: ns tpd: ns Minimum teo: ns Minimum tpd: ns Clock Settings Clock Settings		Global Clock Assignme for a Single Clock Desi
 Fitter Settings Physical Synthesis Optimizations Timing Analyzer Design Assistant SignalTap II Logic Analyzer SignalProbe Settings Simulator Software Build Settings Stratix GX Registration HardCopy Settings 	 Settings for individual clock signals Clocks Cut Options Cut off feedback from I/O pins Cut off clear and preset signal paths Cut off read during write signal paths Cut off read during write signal paths Cut paths between unrelated clock domains Report I/O paths separately 		For Designs with Multiple Asynchronous Clocks, En Required Fmax for Each Individual Clock



Asynchronous Global Clocks

Clock Settings	
C Default required fmax: 5.0	ns 💌
• <u>S</u> ettings for individual clock signals	
٥	ocks Specify settings for ea in clock that is part of the project. You must assign the settings to input clock signals.
	Existing clock settings: Name Type fmax Period Offset Node(s) New clk absolute 250 4.000 ns clk Edit
	New Clock Settings
	Clock settings name:
	Applies to node:
	Relationship to other clock settings
	OK
-	Required fmax: 250 MHz 💌 Resulting period: 4.000 ns
	Duty Cycle (%): 50
	C Based on: clk Derived Clock Requirements
	OK Cancel
	20 YEARS of
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Global Maximum I/O Delay







Global Minimum I/O Delay

Assignments ⇒ S Settings - filtref Category: General Files User Libraries Device	Settings ⇒ Timing Requirements & Options Timing Requirements & Options Specify timing requirements and options. Individual timing assignments can be made through the Assignment Editor.	X	Global th All Inputs or Bidirectional Pins Driving Registers Must Have a th Less Than This Value
Timing Requirements & Options	Delay requirements tsu: ns tco: ns tpd: ns Minimum tco: ns Minimum tpd: ns Clock Settings		Global Minimum tco All Registers Driving Outputs or Bidirectional Pins Must Have a tco Greater Than this Value
 Synthesis Netlist Optimizations Fitter Settings Physical Synthesis Optimizations Timing Analyzer Design Assistant SignalTap II Logic Analyzer SignalProbe Settings Simulator Software Build Settings 	 ○ Default required fmax: 45.0 MHz ✓ Settings for individual clock signals Clocks Cut Options ✓ Cut off feedback from I/O pins ✓ Cut off clear and preset signal paths ✓ Cut off read during write signal paths ✓ Cut off read during write signal paths 		Global Minimum tpd All Direct Pin-to-Pin Path Delays Must Be Greater Than This Value
Stratix GX Registration HardCopy Settings	Cut paths between unrelated clock domains Cut paths separately OK Cancel		



Slack Calculations

- Timing Margin Comparing Actual Timing to Timing Requirements
- Appear Only When Timing Assignments Are Made

Slack = Required Time – Actual Time

Positive Slack

Timing Requirement Met (BLACK)

Negative Slack

Timing Requirement Not Met (RED)



Global Timing Assignments Examples

Clock Setup: 'clk1'								
E	Slack	Actual fmax (period)	From	To	From Clock	To Clock	Required Setup Relationsh	
1	1.165 ns	304.97 MHz (period = 3.279 ns)	multinst lpm_mult	ram:inst2 altsy	clk1	clk1	4.444 ns	
2	1.205 ns	308.74 MHz (period = 3.239 ns)	multinst lpm_mult	ram:inst2 altsy	clk1	clk1	4.444 ns	
3	1.215 ns	309.69 MHz (period = 3.229 ns)	multinst lpm_mult	ram:inst2 altsy	clk1	clk1	fmox Timing Accidement	
4	1.247 ns	312.79 MHz (period = 3.197 ns)	multinst pm_mult	ram:inst2 altsy	clk1	clk1	Values Are BLACK	
5	1.253 ns	313.38 MHz (period = 3.191 ns)	multinst pm_mult	ram:inst2 altsy	clk1	clk1	Because Actual fmax	
6	1.266 ns	314.66 MHz (period = 3.178 ns)	multinst pm_mult	ram:inst2 altsy	clk1	clk1	Exceeds the Required fm	
7	1.293 ns	317.36 MHz (period = 3.151 ns)	multinst pm_mult	ram:inst2 altsy	clk1	clk1	4.444 ns	
8	1.300 ns	318.07 MHz (period = 3.144 ns)	multinst pm_mult	ram:inst2 altsy	clk1	clk1	4.444 ns	

	teu			LLE DH I			
l		Slack	Required tsu	Actual tsu	From	To	To Clock
ļ	73	-0.003 ns	0.200 ns	0.203 ns	dataa[1]	multinst[lpm_mult:lpm_mult_component]mult_9up;au.	clk1
	74	-0.002 ns	0.200 ns	0.202 ns	dataa[5]	multinstlpm_multipm_mult_component/mult_9up;au.	clk1
	75	-0.001 ns	0.200 ns	0.201 ns	dataa[1]	multinstlpm_multipm_mult_component/mult_9up;au.	clk1
1	76	U.UU1 ns	0.200 ns	0.199 ns	dataa[4]	multinstilpm_multilpm_mult_componentimult_9up;au	ck1
	77	0.002 ns	0.200 ns	0.198 ns	dataa[2]	multinst pm_mult pm_mult_component tout	iming assignment
	78	0.004 ns	0.200 ns	0.196 ns	datab[3]	multinstlpm_multipm_mult_component	los Aro BED
	79	0.007 ns	0.200 ns	0.193 ns	datab[6]	multinstlpm_multipm_mult_component	
	80	0.009 ns	0.200 ns	0.191 ns	dataa[1]	multinstlpm_multlpm_mult_component	ause Actual t _{su} Falls
	81	0.009 ns	0.200 ns	0.191 ns	dataa[2]	multinst pm_mult pm_mult_component belo	w Required t _{su}
	82	0.009 ns	0.200 ns	0.191 ns	datab[5]	multinstlpm_multipm_mult_componentlmult_9up;au.	ck1



Individual Timing Assignments

Available Settings

- tsu (Max)
- th (Max)
- tco (Max & Min)
- tpd (Max & Min)
 - Pin-to-Pin
 - Point-to-Point (I/O→Reg; Reg→Reg; Reg→I/O)
- Available Assignment Types
 - Single-Point
 - Point-to-Point
 - Wildcard (* or ?)



Individual Assignment Targets

- Registers (all)
- Clock Pins (tsu, tco, th)
- Input Pins (tsu, th, tpd)
- Output Pins (tco, tpd)
- Bi-Directional Pins (all)



Single-Point tsu/th

Setup/Hold Timing Required on Every Register Fed by Pin





Point-to-Point tsu/th

Setup/Hold Timing Required Only on the Specified Path





Single-Point tco

Clock-to-Out Timing Required on All tco Paths Starting from the Specified Clock





Single-Point tco (cont.)

Clock-to-Out Timing Required on All Paths from Any Clock to Specified Output Pin





Point-to-Point tco

Clock-to-Out Timing Required Only on the **Specified Path**



to Source Register or Clock **Pin & Output Pin**



Wildcard Assignment

Indicates All Targets with a Character or String

- '*' Zero or More Characters
- '?' Single Character



Point-to-Point Setup Using Wildcard:

Assign Setup Requirement from "data" to "Rg*" or "Rg?"



Ex. Assigning Setup Requirement





External Delay Assignments

- Specify System-Level Timing Constraints
- Constrain I/O Timing
 - Same as tsu, th, tco & Minimum tco
- Include I/O Timing as Part of Clock Timing Analysis Report
 - Clock Setup(fmax)
 - Clock Hold
- Settings
 - Input Minimum/Maximum Delay
 - Output Minimum/Maximum Delay



Input Maximum Delay

Maximum Delay from External Device to Altera I/O

- Represents External Device tco + Board Delay
- Constrains Input Pin tsu





Input Minimum Delay

Minimum Delay from External Device to Altera I/O

- Represents External Device tco + Board Delay
- Constrains Input Pin th





Output Maximum Delay

Maximum Delay from Altera I/O to External Device

- Represents External Device tsu + Board Delay
- Constrains Output Pin tco





Output Minimum Delay

Minimum Delay from Altera I/O to External Device

- Represents External Device th Board Delay
- Constrains Output Pin Minimum tco





Example Input Maximum Delay

4

🚭 filtref Compilation Report	,							
😂 🔁 Compilation Report	Cloc	k Setup: 'clk'						
🛛 🚭 🖹 Legal Notice		Slack	Actual fmax (period)	From	То	From Clock	To Clock	Required Setur -
Flow Summary	13	0.173 ns	261.30 MHz (period = 3.827 ns)	multinst6 lpm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns 📃
Flow Settings	14	0.207 ps	263.64.MHz (period = 3.793.ps)	multinstEllom mult	accrimet3laccumrimet	clk	clk	4 000 ps
Flow Elapsed Time	15	0.219 ns	264.48 MHz (period = 3.781 ns)	d[6]	taps:inst xn[6]~reg0		clk	4.000 ns
Flow Log	њ	0.219 ns	264.48 MHz [period = 3.781 ns]	multiinst6/ipm_multi	acc:instalaccum:inst	CIK	CIK	4.000 ns
H	17	0.231 ns	265.32 MHz (period = 3.769 ns)	multinst6llpm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns
	18	0.235 ns	265.60 MHz (period = 3.765 ns)	multinst6 pm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns
	19	0.239 ns	265.89 MHz (period = 3.761 ns)	mult:inst6 lpm_mult:	acc:inst3 accum:inst	clk	clk	4.000 ns
Timing Analyzer Settings	20	0.244 ns	266.24 MHz (period = 3.756 ns)	multinst6llpm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns
- 🗃 🎹 Timing Analyzer Summary	21	0.246 ns	266.38 MHz (period = 3.754 ns)	multinst6 pm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns
Clock Settings Summarv	22	0.255 m	267.02 MHz (pariod = 2.745 ps.)	multipatellara mult	acovinet@lacovinvinet	alk	alk	4.000 mg
Clock Setup: 'clk'	23	0.263 ns	267.59 MHz (period = 3.737 ns)	d[3]	taps:inst[xn[3]~reg0		clk	4.000 ns
A tsu	24	0.263 ns	267.59 MHz (period = 3.737 ns)	mult inst6 lpm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns
	25	0.276 ns	268.53 MHz (period = 3.724 ns)	multinst6 lpm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns
	26	0.283 ns	269.03 MHz (period = 3.717 ns)	mult:inst6 lpm_mult:	acc:inst3 accum:inst	clk	clk	4.000 ns
A Timing Analyzer Messages	27	0.291 ns	269.61 MHz (period = 3.709 ns)	mult:inst6 lpm_mult:	acc:inst3 accum:inst	clk	clk	4.000 ns
	28	0.292 ns	269.69 MHz (period = 3.708 ns)	mult:inst6 lpm_mult	acc:inst3 accum:inst	clk	clk	4.000 ns

Notice:

1) Input Pin d(6) & d(3) Timing Information Is Included with **Clock Setup (fmax) Analysis** 2) Input Delay Has Been Added to List Path Calculation

🖃 抉 Info: Slack time is 219 ps for clock clk between source pin d[6] and destination register taps:inst(xn[6]~reg0 Info: Fmax is 264.48 MHz (period= 3.781 ns) ⊡ ⊕ Info: + Largest pin to register requirement is 2.450 ns. 😟 🚯 Info: + Setup relationship between source and destination is 4.000 ns 😟 🚯 Info: + Shortest clock path from clock clk to destination register is 2.543 ns Info: - Micro setup delay of destination is 0.093 ns. 🖳 🕄 Info: - Max Input delay of pin is 4.0 ns 🕤 🗄 🚯 Info: - Longest pin to register delay is 2.231 ns Processing & System

Input Maximum Delay (d) = 4 ns

20 YEARS of INNOVATION

Clock Setup/Hold (I/O Paths)

- External (System-Level) I/O Timing Reported Separately in Timing Analyzer
 - Option Found in Assignments ⇒ Settings ⇒
 Timing Requirements & Options

	-		.к зесор	(1/O paciis): Cik					
🚑 🖹 Legal Notice			Slack	Actual fmax (period)	From	To	From Clock	To Clock	Required Setup Rela
🗃 🛅 Flow Summary		1	0.219 ns	264.48 MHz (period = 3.781 ns)	d[6]	taps:inst xn[6]~reg0		clk	4.000 ns
Flow Settings		2	0.263 ns	267.59 MHz (period = 3.737 ns)	d[3]	taps:inst[xn[3]~reg0		clk	4.000 ns
Flow Elapsed Time		3	0.715 ns	304.41 MHz (period = 3.285 ns)	d[4]	taps:inst[xn[4]~reg0		clk	4.000 ns
- 🗃 🖺 Flow Log		4	0.773 ns	309.89 MHz (period = 3.227 ns)	d[1]	taps:inst[xn[1]~reg0		clk	4.000 ns
Synthesis		5	0.808 ns	313.28 MHz (period = 3.192 ns)	d[0]	taps:inst[xn[0]~reg0		clk	4.000 ns
		6	0.875 ns	320.00 MHz (period = 3.125 ns)	d[7]	taps:inst[xn[7]~reg0		clk	4.000 ns
Timing Analyzer		7	0.986 ns	331.79 MHz (period = 3.014 ns)	d[2]	taps:inst xn[2]~reg0		clk	4.000 ns
- 🗃 🎹 Timing Analyzer Settings		8	0.999 ns	333.22 MHz (period = 3.001 ns)	d[5]	taps:inst xn[5]~reg0		clk	4.000 ns
- 🗃 🎹 Timing Analyzer Summary		9	4.820 ns	None	taps:inst xn[0]~reg0	taps:inst[xn_1[0]~reg0	clk	clk	4.000 ns
Clock Settings Summary		10	5.267 ns	None	taps:inst xn[7]~reg0	taps:inst[xn_1[7]~reg0	clk	clk	4.000 ns
Clock Setup: 'clk'		11	5.282 ns	None	taps:inst xn[1]~reg0	taps:inst[xn_1[1]~reg0	clk	clk	4.000 ns
Clock Setup (I/O paths): 'clk'		12	5.314 ns	None	taps:inst xn[5]~reg0	taps:inst[xn_1[5]~reg0	clk	clk	4.000 ns
		13	5 398 pc	None	tans:instlyn[2]~red0	tanstinstlyn 1/21~reg0	clk	clk	4 000 ps



Other Individual Timing Assignments

Cut Timing Path

- Removes Paths from TDC & Timing Analysis
- Ex. Test Logic
- Not a Clock
 - Disables Clock Identification
 - Ex. Gate Inputs to Gated Clocks
- Inverted Clock
 - Marks Inverted Clocks Generated with Complex Logic



Report Delay Assignment



Reports Delay between Selected Nodes

- Pin-Register
- Register-Register
- Register-Pin

Reports Results in Custom Delay Section of Timing Analyzer



Multi-Clock Frequency Analysis

- Analyzes Timing on Register-to-Register Paths **Controlled by Different Synchronous Clocks**
 - Individual Clocks Treated as Same Frequency & Phase Unless Specified



Slack Equations for Multi-Clock

Slack = Required Time - Actual Time Slack = Slack Clock Period - (tco + Data Delay + tsu)





Steps for Multi-Clock Analysis

- 1) Create Clock Settings & Assign to Clock Node
 - Define a Base Clock
 - Define Clock(s) Relative to the Base Clock
- 2) Recompile or Restart Timing Analysis
- 3) Examine Results in Timing Analyzer Report

Note: May Also Use Timing Wizard


1) Create Clock Settings

Set Clock Relationships

- Assign Base Clock
- Assign Derived Clock(s) Referenced to Base

derived clock = base clock x (ratio) + offset

Note: Multiple Base & Derived Clocks Allowed





Base Clocks

Timing Requirements & Options	Assignments \rightarrow Settings \rightarrow Timing Settings
Specify timing requirements and options. Individual timing assignments can be made through the Assignment Editor.	
Delay requirements tsu: ns tco: ns tpd: ns Minimum delay requirements Image: tpd: ns Image: tpd: Image: tpd: Image: tpd: Image: tpd: <td></td>	
Clock Settings Specify settings for each clock O Default required fmax: 5.0 O Settings for individual clock signals Clocks	ick that is part of the project. You must assign the settings to input clock signals.
Cut Options Cut off feedback from I/O pins Cut off clear and preset signal paths Cut off read during write signal paths Cut paths between unrelated clock domains Report I/O paths separately	New Clock Settings Image: Clock settings name: Image: Clock settings Image: Clock s
	OK Independent of other clock settings DK MHz Resulting period: Duty Cycle (%): 50 Based on: Derived Clock Requirements
	20 YEARS of

Base Clocks (cont.)





Derived Clocks



220

Derived Clocks (cont.)

Derived Clock Requirements	×
Specify the timing requirements for derived clock	settings 'clk2'
Absolute timing requirements Clock settings name: clk1 Required fmax: 50.0 MHz Resulting period: 20.000 ns Include delays to/from pins: Off Invers	t Base Ratio, Cycle, Offset & sion Settings
Multiply base absolute clock fmax by: Divide base absolute clock fmax by: Duty cycle: 50	Existing clock settings: Name Type fmax Period Offset Node(s) New clk1 absolute 50 20.000 clk1 clk2 derived 33 30.000 2.0 ns clk2 Edit Delete
Resulting fmax: 33.3333333 MHz Resulting period: 30.000 ns Offset from base absolute clock fmax: 2.0	ns 💌
Invert base clock OK Cance Click OK to Add Setting	el DK Cancel



3) Examine Timing Analyzer Report

- Positive Slack Timing Was Met (BLACK)
- Negative Slack By How Much Timing Was Not Met (RED)
- Must Alter Design or Use Timing Assignments (Multi-Cycle) to Resolve Negative Slack

🚑 🔄 Compilation Report	Cloc	k Setup: 'cll	،2'				
🗕 🖨 🖹 Legal Notice		Slack	Actual fmax (p	Source Name	Destination Name	Source Clock Name	Destination Clock Name
- 🗃 🛅 Flow Summary	1	-0.512 ns	None	mult:inst/lpm_mult:lpm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
Flow Settings	2	-0.506 ns	None	multinst/lpm_mult/pm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
Flow Elapsed Time	3	-0.441 ns	None	multinst pm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
Harden Analysis & Synthesis	4	-0.436 ns	None	multinst pm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	5	-0.428 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	6	-0.428 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
Timing Analyzer Settings	7	-0.428 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
- 🚑 🎹 Timing Analyzer Summary	8	-0.428 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	9	-0.428 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
- 👍 🔣 Clock Setup: 'clk2'	10	-0.384 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
tsu	11	-0.358 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
tco	12	-0.358 ns	None	multinstlpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	13	-0.358 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
Timing Apalyzer Messages	14	-0.358 ns	None	multinstlpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	15	-0.358 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	16	-0.340 ns	None	multinstlpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	17	-0.329 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	18	-0.320 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	19	-0.313 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	20	-0.289 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	21	-0.263 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	22	-0.253 ns	None	multinst lpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	23	-0.242 ns	None	mult:inst lpm_mult:lpm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	24	-0.242 ns	None	multinstlpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	25	-0.242 ns	None	multinstlpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2
	26	-0.242 ns	None	multinstlpm_multipm_mult	flip:inst2llpm_ff:lpm_ff_co	clk1	clk2



Multi-Cycle Paths

- Intentionally Require More Than One Clock Cycle to Become Stable
 - Must Be Considered in Design Implementation
 - Must Tell Timing Analyzer to Account for Multiple
 Clock Edges in Clock Setup Calculation





Assigning Multi-Cycle Paths

- Destination/Source Register
 - Applies to All Paths Leading from/to Register
- Register-to-Register
 - Applies to All Paths between One Source & One Destination Register
- Two Clock Domains
 - Applies to All Signals Traveling between Clock Domains
- Register Clock Enables
 - Applies to All Registers Controlled by Clock Enable



Multi-Cycle Assignment

Maximum Point-to-Point Tming

- Data Cannot Arrive after Number of Cycles
- Ex: One Path Is < 1 Cycle, Other Path Is > 1 Cycle
 - Circuit Requires Enables for Proper Operation





Multi-Cycle Hold Assignment

Minimum Point-to-Point Timing

- Data Must Arrive after Hold Time
- Used in Conjunction with a Multi-cycle Assignment





Clock Enable Multi-Cycle Assignments

Assigns Multi-Cycle to Source of Clock Enable

- I/O Pin
- Register
- Settings
 - Clock Enable Multicycle (Maximum)
 - Clock Enable Multicycle Hold (Minimum)





Source Mult-Cycle Assignments

- Used When Source Clock is Higher Frequency
- Settings
 - Source Multicycle & Multicycle Hold
 - Source Clock Enable Multicycle & Muticycle Hold





Ex. Assigning a Multi-Cycle

Assignments \Rightarrow Assignment Editor...





Minimum Timing Analysis

Reports Best-Case I/O Results

- Minimum tco
- th
- Minimum tpd
- Uses Fastest Timing Model
 - Fastest Process
 - Highest Voltage
 - Lowest Temperature



Running Minimum Timing Analysis

- Processing \Rightarrow Start \Rightarrow Start Minimum Timing Analysis
- Must Re-Run Standard Timing Analysis Afterwards
 - Netlist Annotated with Minimum Values
 - Previous Standard Analysis Overwritten



Timing Wizard

- Easy Way to Enter Timing Assignments
- Consolidates Timing
 Settings into One Menu
 - Individual Clock Settings OR
 Overall Circuit Frequency
 - Default System Timing
 - Default External Input/Output Delays
 - Enable/Disable Timing Analysis during Compilation
 - TDC





Exercise 4

Please go to Exercise 4 in the Exercise Manual



Exercise Summary

Multi-Clock Timing Analysis

- Slack Analysis
- Used Timing Wizard to Define Clocks
- Making Multi-Cycle Timing Assignments
 - Used the Node Finder



Timing Analysis Summary

- Single-Clock Timing Analysis
- Timing Assignments
- Multi-Clock Timing Analysis
- Multi-Cycle Timing Assignments
- Minimum Timing Analysis



More Timing Analysis Info

Quartus II Handbook: Using Quartus II Timing Analysis







Designing with Quartus II

Simulation



Quartus II Simulation

- Simulator Method & Features Overview
- Simulator Settings
- VWF File Creation
- Simulation Output
- 3rd Party Simulation



Supported Simulation Methods

Quartus II

- VWF (Vector Waveform File)
 - Primary Graphical Waveform File
- VEC (Vector File)
 - Text-Based Input File
- SCF (Simulator Channel File)
 - MAX+PLUS II Graphical Waveform File
- TBL (Table File)
 - Text-Based Output File from Quartus II or MAX+PLUS II
- Tcl/TK Scripting
- 3rd Party Simulators
 - Verilog/VHDL Testbench



Simulator Features

- Supports 9 Signal Values
 - 1 Forcing '1'
 - 0 Forcing '0'
 - XForcing Unknown
 - U Uninitialized
 - ZHigh Impedance
 - H Weak '1'
 - L Weak '0'
 - W Weak Unknown
 - DC Don't Care



Simulator Features (cont.)

- Performs PowerGauge[™] Analysis
- Converts VWF into HDL Testbench
- Generates HDL Testbench Template
- Supports Breakpoints
- Performs Automatically
 - Adding Output Pins to Output Waveform File
 - Checking Outputs at End of Simulation



Simulator Settings

Mode
Input File
Period
Options

General	Simulator
 Files User Libraries Device Timing Requirements & Options EDA Tool Settings Design Entry & Synthesis Simulation Timing Analysis Board-Level Formal Verification Resynthesis Compilation Process Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Synthesis Netlist Optimizations Fitter Settings Physical Synthesis Optimizations Timing Analyzer Design Assistant Signal ap II Logic Analyzer Simulator Stratix GX Registration HardCopy Settings 	Select options for simulations. Simulation mode: Timing Simulation input: C:/Documents and Settings/mmendoza/Desktop/Q40/1quartus/ppt_test/fir. Simulation period Run simulation until all vector stimuli are used End simulation at: Image: Image: Im



Simulator Mode

- Functional*
 - Type: RTL
 - Uses Pre-Synthesis
 Netlist
- Timing
 - Type: Gate-Level or Post-Place & Route
 - Uses Fully
 Compiled Netlist

ategory:	
General	Simulator
 Files User Libraries Device Timing Requirements & Options EDA Tool Settings Design Entry & Synthesis Simulation Timing Analysis Roard Level 	Select options for simulations. Simulation mode: Timing Simulation input: Timing Graphic for the first start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start is the start
Formal Verification Resynthesis Compilation Process	End simulation at:
Analysis & Synthesis Settings - VHDL Input - Verilog HDL Input - Default Parameters Synthesis Netlist Optimizations Fitter Settings - Physical Synthesis Optimizations Timing Analyzer SignalTap II Logic Analyzer SignalTap II Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer SignalTap E Logic Analyzer HardCopy Settings	Simulation options Automatically add pins to simulation output waveforms Check outputs Setup and hold time violation detection Glitch detection: Simulation coverage reporting Overwrite simulation input file with simulation results uPCore Transaction Model File Name: Power Estimation
	OK Cancel

* Must Generate Functional Simulation Netlist (Processing Menu) before Performing Functional Simulation



Simulator Input & Period

Specifies Stimulus & Length of Simulation Period

	Settings - filtref		×
	Category:		
		Simulator	
Run Simulatio	on until	Select options for simulations.	
End of Stimul		Simulation mode: Timing Simulation input: C:/Documents and Settings/mmendoza/Desktop/Q40/1quartus	/ppt_test/fir.
	- Simulation - Timing Analysis - Board-Level - Formal Verification - Resynthesis	Simulation period Simulation until all vector stimuli are used End simulation at:	
		Simulation options Automatically add pins to simulation transforms	Specify Stimulus File
Enter End	Verilog HDL Input Aragineers s Netlist Optimizations s Timing Analyzer Design Assistant SignalTap II Logic Analyzer SignalProbe Settings Simulator Software Build Settings Stratix GX Registration HardCopy Settings	Check outputs Check outputs Setup and hold time violation detection Glitch detection: Simulation coverage reporting Overwrite simulation input file with simulation results uPCore Transaction Model File Name: Power Estimation	
	1	OK	Lancel //



Simulator Options

Settings - filtref		×
Category:		
Automatically Add Output	Simulator Select options for simulations.	
PINS to Simulation - Design Entry & Synthesis - Simulation - Timing Analysis - Timing Analysis - Verilog HDL Input - Verilog HDL Input - Verilog HDL Input - Verilog HDL Input - Default Parameters - Synthesis Netlist Optimizations - Design Assistant - SignalT ap II Logic Analyzer - SignalT ap II Logic Ana	Simulation mode: Timing Simulation input: C:/Documents and Settings/mmendoza/Desktop/Q4 Simulation period Run simulation until all vector stimuli are used End simulation at: ns v Simulation options Automatically add pins to simulation to tput waveforms Check outputs Setup and hold time violation detection Glitch detection: 1.0 ns v Simulation coverage reporting Overwrite simulation input file with simulation results uPCore Transaction Model File Name: Power Estimation	Compares Simulation Outputs to Outputs in Stimulus File Monitors & Reports Simulation for Glitches



Create New Vector Waveform File

Select File ⇒ New ⇒ Vector Waveform File (Other Files Tab)

File Edit View Project As	signments Ctrl+N Ctrl+O Ctrl+F4	
 New Project Wizard Open Project Convert MAX±PLUS II Project Close Project Save Save As Save Current Report Section Save All Eile Properties Create / Update Export Convert Programming Files 	New Device Design Files Software Files Other Files AHDL Include File Block Symbol File Chain Description File Hexadecimal (Intel-Format) File Memory Initialization File Signal Tap II File Tcl Script File Text File Vector Waveform File	×
	OK Cancel	

INNOVATION

Insert Nodes

Select Insert Node or Bus (Edit Menu)

- VWF Must Be Open
- Use Node Finder



Specify End Time

Maximum Length of Simulation Time

Edit Menu



Insert Time Bars

- Set One Time Bar as Master
- Insert Other Time Bars
 - Relative to Master
 - Absolute



249

Draw Stimulus Waveform

- Highlight Portion of Waveform to Change
- Overwrite Value with Desired Value



INNOVATION

Create Clock

Highlight Waveform & Enter Period



C <u>C</u> lock se	ttings:		_
l C Timo por			
Period:			-
Lenou.			
P <u>h</u> ase:	0.0	ns	-
<u>D</u> uty cyc	:le (%): 50	-	

Select Clock Defined as Timing Setting or Specify Clock Period



Creating Counting Pattern

Highlight Waveform & Enter Pattern

<u> I</u> File	Edit View Project	Assignments	Processing Tools Window Help	Count Value
🗅 🖬	⊾⊃ Undo	Ctrl+Z	/ N? K 🔭 🗇 🕀 🥋	Counting Timing
	r≃ <u>R</u> edo	Ctrl+Y	1	
	👗 Cu <u>t</u>	Ctrl+X		<u>R</u> adix: <u>Binary</u>
<u> ► @</u>	E <u>C</u> opy	Ctrl+C	🖀 😵 🍉 pipemult	Start value: 0
	Paste	⊂trl+V	05 ns • Pointer:	End value: 1
A	Paste Special		100	
₩ ®,	Repeat Paste	Del	10.0	Increment by:
	Select	•		Count type Count Value
#4 2.5		culue.		Binary Counting Timing
VTT ×	gra Eind	Ctri+F F3		O Gray code
_∧≌ ∞∞	A Replace	Ctrl+H		<u>S</u> tart time: D
±rri z √a	→ <u>G</u> o To	Ctrl+G	00	<u>E</u> nd time: 500.0 ns ▼
	Value	Þ		
	Grow or Shrink	Ctrl+Alt+G	Sector Alt + X	Transitions occur
	Group		⁰ _r Forcing Low (0) Ctrl+Alt+0	C <u>B</u> elative to clock settings:
	Ungroup		Forcing High (<u>1</u>) Ctrl+Alt+1	C Eostive edge
<u>^2</u>	Insert Node or Bu	15	Z High Impedance (Z) Ctrl+Alt+Z	OK O Megative edge
^B ₽; 2 ↓	Insert Time B <u>a</u> r		Weak Unknown (W) Ctrl+Alt+W	<u>O</u> ffset:
	Insert <u>W</u> aveform	Interval	XL Weak Low (L) Ctrl+Alt+L	At absolute times:
	Time Bar Organiz	er	VE Dop't Care (DC) Ctrl+Alt+H	
	End Time		INV Invent	
	Grid Size	<	Count Value Ctrl+Alt+V	
	≜ ↓ Sort <u>.</u>		Clock Ctri+Alt+K	
	Properties		X? Arbitrary Value Ctrl+Alt+B	


Waveform to Testbench Generator

Converts VWF into HDL Testbench

Ŀ	File	Edit	View	Project	Assignments			
11 0	D	<u>N</u> ew			Ctrl+N			
11	2	Open			Ctrl+O			
≯		⊆lose			Ctrl+F4			
	图	New Pr	oject <u>V</u>	<u>V</u> izard		-		
	R	Open F	roject.					
		Conver	t MAX ₃	<u>+</u> PLUS II F	Project			
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		Save <u>A</u>	s					
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Xū	ø	Save A	ļļ.					
- <mark>0</mark> -7		<u>F</u> ile Pro	perties	5				
- 		Create	/ Upda	ate				
\sim		Export	<u>.</u>					
- <u>X</u> e - XG		Conver	rt Progr	ra <u>m</u> ming F	ile			
_X <u>S</u>		Include	Repor	t Section	in	F		
<u>X</u> ?	m	Page S	etyp		File name:	pipemult.vt		Export
믱	D.	Print Pr	re <u>v</u> iew		Save as type:	Verilog Test Bench File (*.vt)	•	Cancel
	6	Print				Add self-checking code to file	_	
		Recent	Files					1
		Recenț	Projec	:ts	•	_		
		E⊻it			Alt+F4			

Courier New 🔽 10 🔽 🛤 🍇 🔂 🐺 事 🔺 ۶ 券 🚪 🛯 🔽 🔯 🕺
26 // **********************************
27 // Generated on "07/10/2003 10:53:25"
28
29 // Verilog Self-Checking Test Bench (with test vectors) for design :
30 //
31 // Simulation tool : 3rd Party
32 //
33
34 `timescale 1 ps/ 1 ps
35 module pipemult_vig_sample_tst(
36 81,
37 34,
30 a3,
40 85.
41 \$6.
42 sampler tx
43);
44 input s1;
45 input [7:0] s2;
46 input [7:0] s3;
47 input [4:0] s4;
48 input [4:0] s5;
49 input s6;
50 output sampler_tx;
51
52 reg sample ;
50 Edialwaya Biatar at ar at ar at ar at
22 01 01 01 01 01 02 01 03 01 01 01 02 01 00)
56 begin
57 if (stime > 0)
58 begin
59 if (sample === 1'bx)
60 sample = 0;
61 else
62 sample = ~sample;
I



Testbench Template Generator

Generates HDL Testbench Template User Inserts Test Stimulus

Processing Tools Window Help		
Etop Processing Ctrl+Shift+C	😻 🗞 ⊗	simulation\modelsim\dac_demo_ver.vt
Start Compilation Ctrl+L Analyze Current File	🎸 a 📠 🗟 📎 🖄 🖬	<pre>// assign statements (if any) 78 // assign (t_wire_indata622,t_wire_in_deskew,t_wire_in_clock, 80 dac_demo_ver tb (</pre>
Start Compilation Report Ctrl+R	V Start Analysis & Elaboration Start Analysis & Synt <u>h</u> esis Ctrl+K	81 // port map - connection between master ports and signals/regist 82 .indata622(t_wire_indata622),.in_deskew(t_wire_in_deskew),.i 83 initial
Start Compilation & Simulation Start Simulation Ctrl+I Simulation Debug Simulation Report Ctrl+Shift+R Start Software Build Ctrl+Q Compile Current File	 Start Fitter Start Assembler Start Timing Analyzer Ctrl+Shift+L Start EDA Netlist Writer Start Design Assistant Start Incremental Fitting Start SignalProbe Compilation Ctrl+Shift+S Start I/Q Assignment Analysis Start Minimum Timing Analysis Start VQM Writer Start Test Bench Template Writer 	<pre>84 // code that executes only once 85 // insert code here> begin 86 87 //> end 88 \$display("Running testbench"); 89 end 90 always() 91 // optional sensitivity list 92 // @(eventl or event2 or eventn) 93 begin 94 // code executes for every event on sensitivity list 95 // insert code here> begin 96 97 @eachvec; 98 //> end 99 end 100 endmodule 101</pre>



Starting Simulation

Processing Menu \Rightarrow Start Simulation



	_0\qdes	signs\fir_f	ilter\cor	npile\o	ompile	_fir
File Edit View Project Assig	gnments	Processing	Tools	Window	w Help	
0 🛎 🖬 🎒 🕺 🖻	ß	Top P	rocessing	Ctrl+:	Shift+C	
🛛 💥 🗢 🖿 🔁 📾 📰 🌏		Start (Analyz Church Start)	Compilatio e Current	n Ele	Ctrl+L	
Entity Compilation Hierarchies	Logic Ce	Compil	ation Rep	ort	Ctrl+R	
🗄 秒 filtref	96 (2)	S <u>t</u> art (Compilatio	n & Sim	ulation	
		🚬 Start S	Simulation		Ctrl+I	
		Simula ج	tion <u>D</u> ebu tion Repo	g rt Ctrl+:	Shift+R	•
		L Start S Compi	oftware (e Cyrrent	<u>B</u> uild File	Ctrl+Q	

Scripting



Simulator Report

Displays Simulation Result Waveform

 □ □ 0 /ul>	秋皇					
imulator Report 을 Legal Notice 을 Project Settings 문을 Results for "pipemult" Simulator Se	Simulation Waveform Master Time Bar: 1	ms 12.05 ns Pointer: 0 ps	83 ps In	terval: -11.97 ns	Start: E	nd:
Simulator Settings Simulation Waveforms Discrete Settings Messages Processing Time	ck1 dataa dataa datab wwaddress			X 02 X 02	X 03	× 04 × 04
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Naveform			F	Result Wav	<mark>reform</mark>	



Comparing Waveforms

Select Compare to Waveforms (View Menu)

- Simulation Waveform Must Be Open

Select VWF Comparison File

Qu	lartus	11 -	C:\Docume	ents and Sett	ings\ggooda	irz\My			
ile	<u>E</u> dit	∐⊻i	ew <u>P</u> roject	Assignments	Processing	Tools			
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		- 12 - 12	Sn <u>a</u> p to Tra	nsition	-				
		咒	Snap to Grig	1					20



Compared Waveforms (Simulator Report)

Original (Ctrl+1)



Actual (Ctrl+2)



Compared (Ctrl+3)



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INNOVATION

Using Message Window to Debug



Breakpoints

Interrupts Simulation at Specified Points

- Consists of 2 Parts
 - Equation (Condition)
 - Action
 - Stop
 - Give Error
 - Give Warning
 - Give Info





Breakpoint Conditions

<Node> <Operator1> <Value>

- Single Condition
- Ex. ena = 1
- Time = <Value>
 - Single Condition
 - time = 500ns
- <Condition> <Operator2> <Condition>
 - Complex Tests
 - ena = 1 && time > 500ns

			OK
			Cancel
			Rename
			Сору
			Delete
Move <u>L</u>	lp .	Move Do <u>w</u> n	
Equation Break if this e condition	equation is tr	ue: tor1 value	



Breakpoint Equations (cont.)

reakpoints	>
<u>B</u> reakpoints:	
✓ bp9: stop when (node operator1 value) opera	OK
click here to insert new breakpoint	Cancel
	R <u>e</u> name
	<u>С</u> ору
	<u>D</u> elete
Move <u>U</u> p Move Do <u>w</u> n	
Equation	
Break if this equation is true:	
(<u>node operator1 value</u>) <u>operator2</u> (<u>node operator</u>	or1 value)
Action	
Then do this:	
Stop	-
A start to	

Node

- Opens Node Finder
- Operator1
 - <, >, =
- Operator2
 - && (AND)
 - || (OR)



Example Breakpoint





PowerGauge Analysis Software

Estimates Power Consumption Based on Toggle Rates

- Derives Toggles Rate from Simulation Stimulus
- Uses Quartus II Simulator
- Supports Multiple I/O Standards
- Supports Stratix, Stratix GX, Cyclone MAX 7000AE, MAX 7000B, MAX 3000 Families
- 3rd Party Simulation Tools Output PWF File that Can Be Read by Quartus II Simulator



Power Analysis

Settings - filtref		×		
Category:				
General Files User Libraries Device Timing Requirements & Options	Simulator Select options for simulations.		2) Enter Simulation Dr	riod
Analysis EDA Tool Settings Design Entry & Synthesis Simulation Timing Analysis Board-Level Formal Verification Resynthesis Compilation Process Analysis Synthesis Settings Synthesis Netlist Optimizations Fitter Settings Physical Synthesis Optimizations Fitter Settings Physical Synthesis Optimizations Fitter Settings SignalTap II Logic Analyzer SignalProbe Settings Simulator Software Build Settings Stratix GX Registration HardCopy Settings	Simulation mode: Timing Simulation input: C:/Documents and Settings/mmendoza/Desktop/Q40/1qu Simulation period Run simulation until all vector stimuli are used End simulation at: ns End simulation at: ns Simulation output waveforms Setup and hold time violation detection Glitch detection: 10 ns Simulation coverage reporting Overwrite simulation input file with simulation results UPCore Transaction Model File Name: Power Estimation	artus/ppt_test/fir Power Estimatic Select options for ✓ Estimate power estin Start time: End time: (Cancel	2) Enter Simulation Performance on or power estimation. wer consumption imation period 0.0 10 ms OK Cancel	riod
		1.		



Power Analysis (cont.)





Using 3rd Party Simulators

- Mentor Graphics
 - ModelSim
- Cadence
 - VERILOG-XL
 - NC-Verilog
 - NC-VHDL
- Synopsys
 - VCS
 - VSS
 - Scirocco





Specify Simulator

Select EDA Tools Settings

Assignments Menu



INNOVATION

3rd Party Simulation Files

Functional Simulation

- Use 220models & altera_mf Megafunction Model Files
- VHDL Timing Simulation
 - Use Quartus II-Generated VHO & SDO Files
 - Use <device_name>_ATOMS.VHD & <device_name>_ATOMS_COMPONENTS.VHD Files
 - Located in eda\sim_lib Directory
- Verilog Timing Simulation
 - Use Quartus II-Generated VO & SDO Files
 - Use <device_name>_ATOMS.VO File
 - Located in eda\sim_lib Directory



Exercise 5

Please go to Exercise 5 in the Exercise Manual



Exercise Summary

- Learn about Quartus II Simulator
- Draw Signals in VWF Files
- Functional Simulation
 - View Simulation Results



Simulation Summary

- Functional & Timing Simulation
- Creating a Vector Waveform File
- Power Analysis







Designing with Quartus II

Programming/Configuration



Programming/Configuration

- Setting Device Options
- Assembler Module
- Programmer & Chain Description File
 - Programming Directly with Quartus II
- File Conversion
 - Creating Multi-Device Programming Files



Setting Device Options

■ Assignments ⇒ Device ⇒ Device & Pin Options Button





General Tab

vice & Pin Opt	ions		
Dual-Purp	ose Pins	Voltage	Pin Placement
General	Configuration	Programming File	les 🔰 Unused Pins
Specify general scheme.	device options. These	e options are not depe	ndent on the configuration
Options:			
Auto-restart	configuration after error		
Release clea	ars before tri-states		
Enable user-	supplied start-up clock	(CLKUSR)	
Enable devid	ce-wide reset (DEV_CL	Rn)	
Enable devidence	ce-wide output enable (DEV_OE)	
✓Enable INIT.	_DONE output		
, 			
Generate co	ompressed bitstreams		
🗖 Auto userco	ode		
JTAG user code	e (32-bit bexadecimal):	FFFFFFF	-
-	o (oz ok nondacosinal).		
Description:			
Specifies user- an extension of USERCODE in	defined information abo f the option register. Th istruction.	ut the target device. T is data can be read wi	Гhe JTAG user code is _▲ ith the JTAG
			.
			Beset
			100

- Device Options Not Dependent on Configuration Scheme
 - Enable Device-Wide Clear
 - Enable Device-Wide
 Output Enable
 - Enable Initialization
 Done Output Pin



Configuration Tab

De	evice & Pin Options		×
	Dual-Purpose Pins General Configuration	Voltage Programming F	Pin Placement Files Unused Pins
	Specify the device configuration sche	me and the configura	ition device
	Configuration scheme: Fast Passive	Parallel (can use Con	figuration Device)
	Configuration mode: Standard	년	
	Use configuration device:	EPC16	
		<u>C</u> onfiguration	Device Options
Dptions Files Allows you to set Configuration de JTAG user coo C Auto usero C Auto usero C Configurat Autom	t configuration device options. vice: EPC16 de settings code ion device JTAG user code (32-bit hexadecimal): atically increment JTAG user code for multiple cont and OE pull-ups on configuration device	FFFFFFFF iguration devices	the means of configuring 🔺
Compression Low-voltage Clock settings Clock source: Clock frequen	mode mode Internal V 66 MHz V		
Divide clock fr	requency by: 1.0		OK Cancel
Allows you to co (.pof) for a confi	mpress SRAM Object Files (.sof) stored in a Progra guration device.	ammer Object File	
)K Cancel	

- Choose Device Configuration Mode & Available Options
 - Generates Correct
 Configuration &
 Programming Files Every
 Compilation
- Enables Special Features of Configuration Devices
 - Enable Programming File Compression
 - Set Configuration Clock
 Frequency



Programming Files Tab

- Output Files Always
 Created
 - POF (Programming Object File)
 - SOF (SRAM Object File)
- Other Selectable Output Files
 - JAM (JEDEC STAPL)
 - JBC (JAM Byte-Code)
 - RBF (Raw Binary File)
 - HEXOUT (Intel Hex Format)

Dual-Purpose Pins	Voltage	Pin Placement
General Configuration	Programming File	es Unused Pins
elects the optional programming file l ultiple configuration schemes, if you onfiguration tab, the Quartus II softw id either a Partial SRAM Object File spending on the configurable device	formats to generate. Fo select a passive config vare always generates a (.psof) or a Programmer e you are targeting. mat) File (.hex) into the d	r device families with uration scheme in the n SRAM Object File (.sof) Object File (.pof), putput files:
n/a in Stratix II		
Tabular Text File (.ttf)	□ <u>S</u> erial Vector	Format File (.svf)
Ra <u>w</u> Binary File (.rbf)	🔲 In System Co	nfiguration File (.isc)
Jam STAPL Byte Code 2.0 File (.jt	bc) 🔲 JEDEC STAF	PL Format File (.jam)
Compressed		
Hexadecimal (Intel-Format) Output	t File (.hexout)	
Start address: 0	C <u>o</u> unt: []]p	x
J	1	
escription. enerates a Tabular Text File (.ttf) co xternal controller can use to configu	ontaining configuration o rre the target device.	lata that an intelligent 🔺
		<u>R</u> eset



Unused & Dual-Purpose Pins Tabs

- Selects Usage of Dual-Purpose Pins after Configuration Is Complete
- Indicates State of All Unused I/O Pins after Configuration Is Complete



20 YEARS of



Quartus II Assembler Module

- Generates All Configuration/Programming Files
 - As Selected in Device & Pin Options Dialog Box
- Ways to Run Assembler
 - Full Compilation
 - Execute Assembler Individually
 - Processing Menu \Rightarrow Start \Rightarrow Start Assembler
 - Generates Files without Full Compilation
 - Switching Configuration Devices
 - Enabling/Disabling Configuration Device Feature
 - Scripting



Open Programmer

🐇 Quartus II - C:/quartu	ıs4 0/qdes	igns/fir_fil	ter/compile/compile fir filter-filtref
File Edit View Project	Assignments	Processin	g Tools Window Help
□ ☞ 및 를 % X � [] � []	₽a 🖻 · 9 🎨	¤ ≈ ¥	Run EDA Simulation Tool Run EDA Timing Analysis Tool Launch Software Debugger Ctrl+Shift+D
Entity Compilation Hierarc	LC Combi	LC Regi	≚ Gompiler Tool M ∰ Simulator Tool M ∰ Timing Analyzer Tool
EUT			Chip Editor RTL Viewer SignalTap II Logic Analyzer Programmer MegaWizard Plug-In Manager SOPC Builder Tcl Scripts Customize Options
			License Setup

Enables Device
 Programming

- ByteBlaster[™] II or
 ByteBlasterMV[™] Cables
- USB-Blaster
- MasterBlaster[™] Cable
- APU (Altera Programming Unit)
- Opens Chain Description File (.CDF)
 - Stores Device Programming Chain Information



CDF File

Lists Devices & Files for Programming or Configuration

Programs/Configures in Top-to-Bottom Order

iltref.cdf									- 🗆 ×
🔔 Hardware Setup	. ByteBlasterMV [LPT1]		Мо	de: JTAG		•	Progress:		0%
Mu Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit
🖬 Stop	1fir_filter/simulate/filtref.sof	EP1C3T100	00055D30	FFFFFFF		Ц			
Auto Detect	 o_restored/counter_1.pof o_restored/counter_2.pof o_restored/counter_3.pof QII3.0_labs/lockit/lockit.sof 	EPC2 EPC2 EPC2 EPC2 EP1510F780	00087168 0007AEA4 0008A3B3 02C511EE 002AF707	FFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF					
Add File Change File Save File									
Add Device		nen Addi evice for utomatic	ng File that F ally Cl	es, the file is nosen					



Programmer Toolbar

- Start Programming
- Auto Detect Devices in JTAG Chain
- Add/Remove/Change Devices in Chain
- Add/Remove/Changes Files in Chain
- Change Order of Files in Chain
- Setup Programming Hardware

<u>Note:</u> All Options are available the Edit Menu except Start Programming & Auto Detect which are available in the Processing Menu





Setting up Programming Hardware

Click on the Hardware Setup Button

📕 Hardware Setu	p ByteBlasterMV [LPT1]		N	Node: JTAG		•	Progress:		0%
M Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Secu Bit
🖬 Stop	1fir_filter/simulate/filtref.sof	EP1C3T100	00055D30	FFFFFFF					
Auto Detect	2emo_restored/counter.pof 3o_restored/counter_1.pof 4o_restored/counter_2.pof	EPC2 EPC2 EPC2	000B716B 0007AEA4 000843B3	FFFFFFF					
🗙 Delete	5o_restored/counter_3.pof 6OII3.0 labs/lockit/lockit.so	EPC2 f EP1510F780	02C511EE 002AF707	FFFFFFF	2	2			
📛 Add File									
Hardware Settings JTA Select a programming H hardware setup applies	G Settings hardware setup to use when program only to the current programmer windo	ming devices. This pro ow.	ogramming						
Hardware Settings JTA Select a programming h hardware setup applies Currently selected hard Available hardware its	G Settings ardware setup to use when program only to the current programmer windo ware: ByteBlasterMV [LPT1] ems:	ming devices. This pro ow.	ogramming t Hardware						
Hardware Settings JTA Select a programming h hardware setup applies Currently selected hard Available hardware its Hardware ByteBlasterMV	G Settings ardware setup to use when program only to the current programmer windo ware: ByteBlasterMV [LPT1] ems:	ming devices. This pro ow.	bgramming It Hardware Hardware						



Chain Programming Modes

🖥 my_chain.cdf					
🚖 Hardware Setup.	ByteBlasterMV [LPT1]		м	ode: JTAG 💌	Pro
M Start	File	Device	Checksum	U In-Socket Programming Passive Serial	y
Stop	1 Fir filter/simulate/filtref.cof	FD1C3T100	00055D30	EPActive Serial Programming	<u> </u>

- Altera FPGAs, CPLDs & Non-Altera Devices
 JTAG
- Altera FPGAs Only
 - Passive Serial
 - Active Serial
- CPLDs & Configuration Devices in APU
 - In-Socket



Programming Options

- Program/Configure
 - Applies to All Devices

Verify, Blank-Check & Examine

- Configuration Devices
- MAX 7000 & MAX 3000
- Security Bit

– MAX 7	& 000	MAX	3000
---------	-------	-----	------

To Program, Verify, Blank-Check, or Examine the Device, Check the Appropriate Boxes

🖥 my_chain.cdf										JN
🌲 Hardware Setup	ByteBlasterMV [LPT1]			Mode: JTAG		•	Progress:		0%	
M Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Slank- Check	Examine	Security Bit	
🖬 Stop	1fir_filter/simulate/filtref.sof	EP1C3T100	00055D30	FFFFFFF						
Auto Detect	 emo_restored/counter.pof o_restored/counter_1.pof o_restored/counter_2.pof o_restored/counter_3.pof 	EPC2 EPC2 EPC2 EPC2	00087168 0007AEA4 0008A3B3 02C511EE	FFFFFFF FFFFFFF FFFFFFF FFFFFFF	N N N N N	হাবে	> > > >			
	6QII3.0_labs/lockit/lockit.sof	EP1S10F780	002AF707	FFFFFFF						





Bypassing Devices in JTAG Chain (1)





Bypassing Devices in JTAG Chain (2)




Adding Non-Altera Device to Chain



Starting the Programmer





Converting SOF Programming Files

K Quartus II - C:/quart	us4_0/qdesi	igns/fir_filter/co				
File Edit View Project	Assignments	Processing Too				
<u> </u>	Ctrl+N	Q N 6			Creates M	
🗃 Open	Ctrl+O				• Creates Mit	LITI-Device .POF for
⊆lose	Ctrl+F4				Enhanced	Configuration Devices
PA New Design Uland					Enables Co	ompression & Other
		Per IN			Configurat	ion Dovigo Ontions
皆 Open Project	Ctrl+. Co	nvert Programming Fi	les		Connigurat	ion Device Options
Convert MAX+PLUS II Project		pecify the input files to convert and the type of programming file to generate.			n information created here for	
Save Projec <u>t</u>	, fi	uture use.	ie information nom other nies and	save the conversion setup	p information created here for	
Clos <u>e</u> Project	Γ	Conversion setup files				
🖬 Save	Ctrl+5	Open Con <u>v</u> e	ersion Setup Data	Save Cor	nversion Setup	
Save <u>A</u> s	F	- Output programming file -				
Save Current Report S	ection As	Programming file type:	Programmer Object File (.pof)		T	
		Options	Configuration device: EPC1	6UC88 Mode: 2	2-bit Passive Serial	
File Properties		File name:	C:\QuartusII3_0\adesians\fir	filter\compile\output_file.pd	of	
Create (Update			Bemote/Local undate difference	se file: NONE		
Export,			Memory Man File	in the prove		
Convert Programming	Files		i inginal map i no			
		Input files to convert				
🛄 Page Setyp		File/Data area	Prop	erties	<u>A</u> dd Data	
🔄 Print Preview		E SOF Data	Page	0	Add File	
🖨 Print	Ctrl+F	⊡Bit 0	EP19	108672		
		E-Bit 1	Errs	100012	<u>H</u> emove	
Recent Files		Line lockit.sof Bottom Boot Data	EP19	10F780	р	
Recent Projects					Down	
Recenteriojects					Properties	
E <u>x</u> it	Alt+F4				Tishaugaa	
📥 Hierarchy j 🖹 Files j 🗈	🗜 Design U				OK Cancel	
						20 YEARS of

of INNOVATION

Creating Jam[™] STAPL



INNOVATION

292

Exercise 6 or 7 (Optional)

Please go to Exercise 6 or 7 in the Exercise Manual



Programming/Configuration Summary

- Setting Device Options
- Generating Programming Files
- Programming Device or Devices in Chain
- Converting Programming Files



Class Summary

- Design Entry Techniques
- Project Creation
- Compiler Settings & Assignment Editor
- Timing Analysis
- Simulation
- Programming/Configuration



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- Chip Editor
- FPGA Optimization
- SignalTap II & SignalProbe
- Command-Line & Tcl Scripts
- HardCopy Software Support



Altera Technical Support

- Reference Quartus II On-Line Help
- Consult Altera Applications (Factory Applications Engineers)
 - MySupport: http://www.altera.com/mysupport
 - Hotline: (800) 800-EPLD (7:00 a.m. 5:00 p.m. PST)
- Field Applications Engineers: Contact Your Local Altera Sales Office
- Receive Literature by Mail: (888) 3-ALTERA
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