



# Nios Embedded Processor Development Board

July 2003, ver. 2.2

Data Sheet

## Introduction

This data sheet describes the features and functionality of the Nios<sup>®</sup> CPU development board included in the Nios Development Kit, APEX Edition featuring the Nios embedded processor.

## Development Board Features

- An APEX<sup>™</sup> 20K200E device
- 1 Mbyte (512 K x 16-bit) of flash memory
  - pre-configured with the 32-bit Nios reference design and software
- 256 Kbytes of SRAM (in two 64 K x 16-bit chips)
- On-board logic for configuring APEX device from flash memory
- 3.3-V expansion/prototype headers (access to 40 user I/Os)
- 5-V-tolerant expansion/prototype headers (access to 40 user I/Os)
- Small outline DIMM (SODIMM) socket, compatible with standard SDRAM modules
- Two IEEE-1386 peripheral component interconnect (PCI) mezzanine connectors
- One RS-232 serial connector
- One user-definable 8-bit DIP switch block
- Four user-definable push-button switches
- Dual 7-segment LED display
- Two user-controllable LEDs
- Joint test action group (JTAG) connector for ByteBlaster II<sup>™</sup> and MasterBlaster<sup>™</sup> download cables
- Oscillator and zero-skew clock distribution circuitry
- Power-on reset circuitry
- Power-supply circuitry (Input: 9-V unregulated, center-negative)

## Functional Overview

The Nios development board provides a hardware platform to immediately start developing embedded systems based on Altera<sup>®</sup> APEX devices. The Nios development board is pre-loaded with a 32-bit Nios embedded processor system reference design. A Quartus<sup>®</sup> II project directory containing the reference design example is installed with the Nios development software. The reference design and software are pre-loaded in flash memory, and boot on power-up. The reference design software includes a monitor that can be used to download and debug programs.

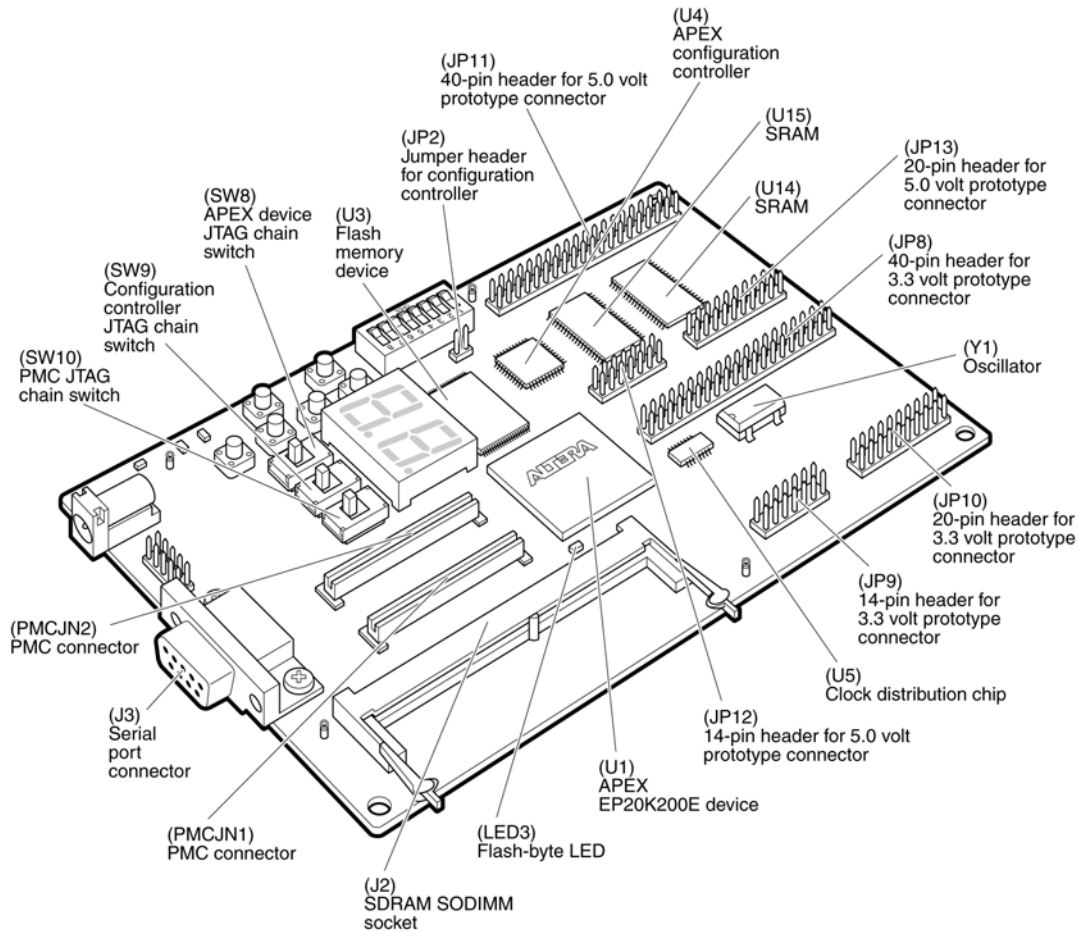
## Nios Development Board Components

This section contains a brief overview of several important components on the Nios development board. A more complete list of components appears in [Table 3 on page 20](#). A complete set of schematics, a physical layout database, and GERBER files for the Nios development board are installed as documentation for the Nios embedded processor software.



Choose **Programs > Altera > Nios Development Kit** *<installed version>* **Altera Nios Documentation** (Windows Start menu) for board-related files.

Figure 1. Nios Development Board



See [Table 3 on page 20](#) for a complete list of the Nios development board components.

## The APEX 20K200EFC484 Device

U1 is an APEX 20K200E device in a 484-pin FineLine BGA™ package. A useful Nios system module (CPU and peripherals) typically occupies between 25% and 35% of the logic on this device.

Maximum system gates	526,000
Typical gates	211,000
LEs	8,320
ESBs	52
Maximum RAM bits	106,496
Maximum macrocells	832
Maximum user I/O pins	382

The development board provides two separate methods for configuring the APEX device:

1. A JTAG connection (JP3) that can be used with Quartus II software via a ByteBlaster II or MasterBlaster download cable.
2. A configuration controller (U4) that configures the APEX device at power-up from hexout files stored in the flash memory (U3). See [“Configuration Controller” on page 15](#) for more information.

## Flash Memory Chip

U3 is an Advanced Micro Devices (AMD) AM29LV800BB 1 Mbyte flash memory chip. It is connected to the APEX device so that it can be used for two purposes:

1. A Nios processor implemented on the APEX device can use the flash as general-purpose readable, memory and non-volatile storage.
2. The flash memory can hold an APEX device configuration file that is used by the configuration controller to load the APEX device at power-up. See [“Configuration Controller” on page 15](#) for related information.

A hexout configuration file that implements the 32-bit Nios reference design is pre-loaded in this flash memory. The 32-bit reference design, once loaded, can identify the 1 Mbyte flash in its address space, and includes monitor software that can download files (either new APEX device configurations, Nios software, or both) into flash memory. The Nios software includes subroutines for writing and erasing this specific type of AMD flash memory.

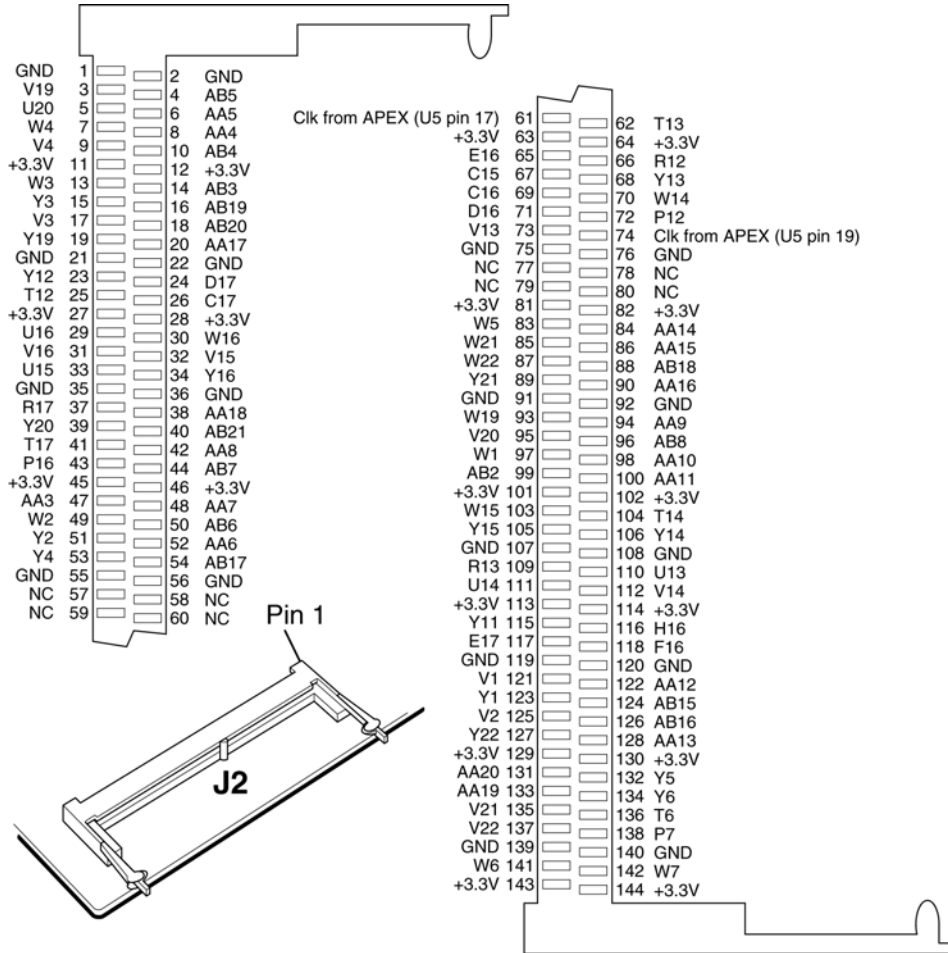
## **Dual SRAM Chips**

U14 and U15 are 256 Kbyte (64 K x 16-bit) asynchronous SRAM chips. They are connected to the APEX device so they can be used by a Nios processor as general-purpose zero-wait-state memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The pre-loaded Nios reference design identifies these SRAM chips in its address space as a contiguous 256 Kbyte, 32-bit-wide, zero-wait-state main memory.

## **SODIMM Connector**

J2 is a 144-pin SODIMM socket that is compatible with standard single-data-rate, 64-bit-wide SDRAM modules. J2 is connected to the APEX device so that user logic can access SDRAM. The pre-loaded reference design does not make use of this connector.

Figure 2. SODIMM Connector



## Expansion Prototype Connector Header: 3.3-V

Headers JP8, JP9, and JP10 collectively form a standard-footprint, mechanically-stable connection that can be used (for example) as an interface to a special-function daughter card. Contact your Altera sales representative for a list of available expansion daughter cards that can be used with the Nios board.

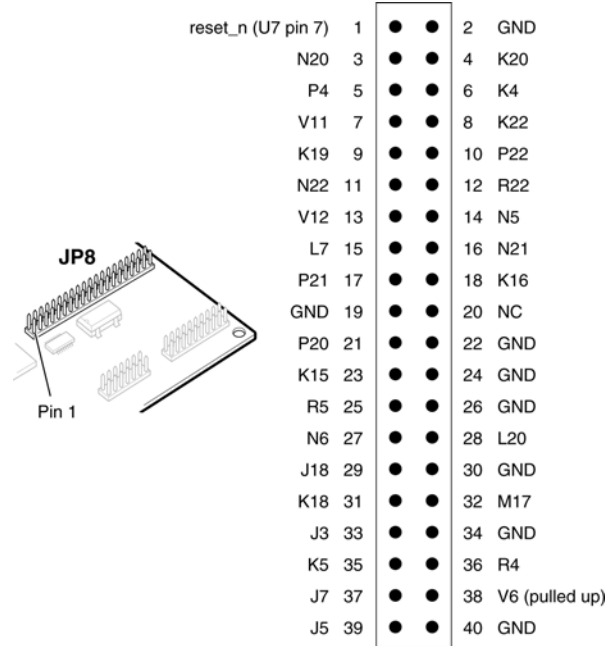
The 3.3-V expansion prototype connector interface includes:

- 40 APEX device general-purpose I/O signals.
- A buffered, zero-skew copy of the on-board OSC output (from U5).
- A buffered, zero-skew copy of the APEX's phase-locked loop (PLL)-output (from U5).
- An APEX device clock-input (for daughter cards that drive a clock to the programmable logic device (PLD)).
- A logic-negative power-on-reset signal.
- Two regulated 3.3-V power-supply pins (500 mA total max load).
- Unregulated power-supply pin (connects directly to J1 power-input plug).
- Numerous ground connections.

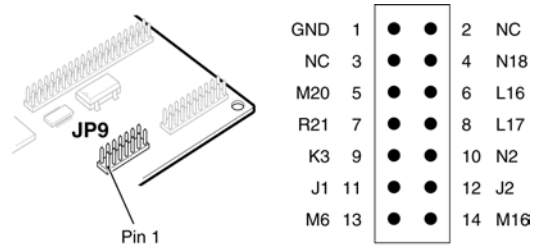


The pre-loaded Nios reference design does not use the 3.3-V expansion prototype connector.

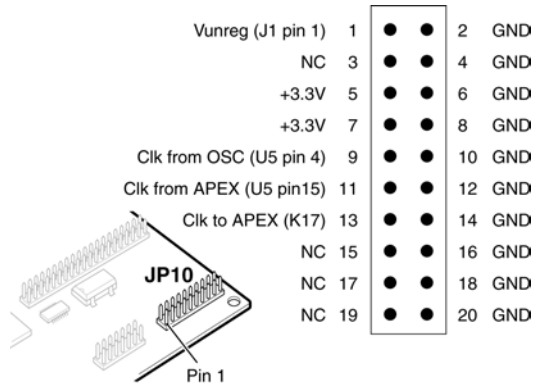
**Figure 3. 3.3-V Expansion Prototype Connector - JP8**



**Figure 4. 3.3-V Expansion Prototype Connector - JP9**





**Figure 5. 3.3-V Expansion Prototype Connector - JP 10**

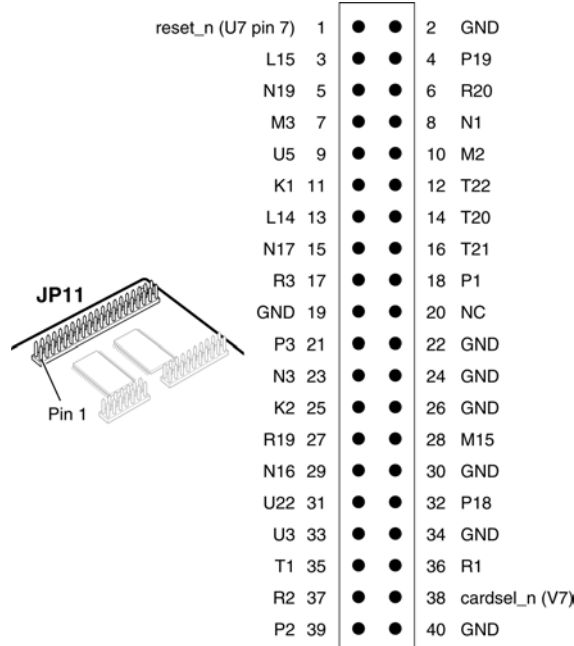
## Expansion Prototype Connector Header: 5-V tolerant.

Headers JP11, JP12, and JP13 collectively form a standard-footprint, mechanically-stable connection that can be used (for example) as an interface to a special-function daughter card. The pre-loaded Nios reference design uses JP12 as an interface to the dual 7-segment LCD display included with the Nios kit. The 5-V-tolerant expansion connector is similar to the 3.3-V expansion connector, except as indicated herein below:

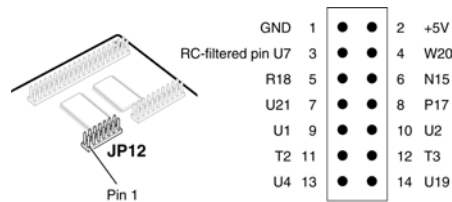
- JP11 (pin 38) is used as a global card-enable signal. All 40 I/O connections pass through analog switches (U8, U9, U11, and U12) to protect the APEX device from 5-V logic levels. These analog switches are globally enabled (switched-on) by APEX device I/O pin V7 (logic-0 on V7 enables switches).
- A low-current 5-V power supply (50 mA max load) is presented on pin 2 of JP12 (the corresponding pin on the 3.3-V expansion connector is not connected).
- An RC-filtered connection to APEX device I/O pin (U7). This circuit is suitable for producing a high-impedance, low-precision analog output if U7 is driven with a duty-cycle-modulated waveform by user-logic. The corresponding pin on the 3.3-V expansion connector is not connected.
- The Vref-voltage for the analog switches (3.3-V plus one diode-drop) is presented on pin 3 of JP13. The corresponding pin on the 3.3-V expansion connector is not connected.

The pre-loaded Nios reference design uses JP12 as an interface to the dual 7-segment LCD display included with the Nios Development Kit, featuring the Nios embedded processor.

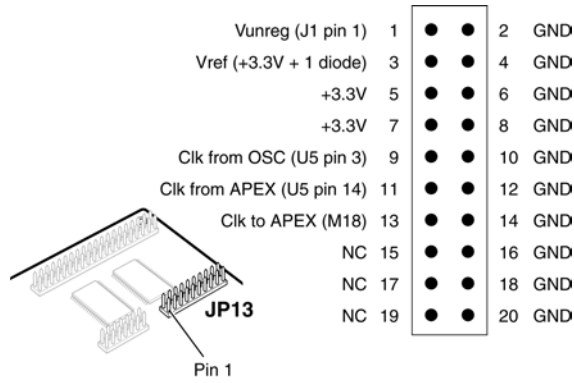
**Figure 6. 5-V Expansion Prototype Connector - JP11**



**Figure 7. 5-V Expansion Prototype Connector - JP12**



**Figure 8. 5-V Expansion Prototype Connector - JP13**

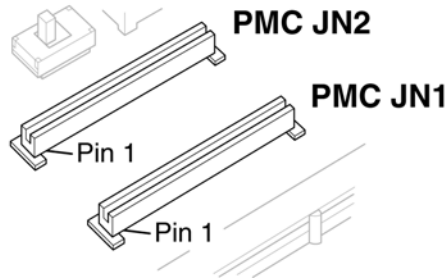


## PMC Connectors

PMCJN1 and PMCJN2 are IEEE1386-compliant PMC connectors. User logic in the APEX device can access PMC daughter cards through these connectors. The pre-loaded Nios reference design does not use the PMC connectors.

Figure 9. PCI Mezzanine Connectors (PMC)

PMC JN1				PMC JN2			
JTAG TCK	1	□ □	2 NC	NC	1	□ □	2 1K pullup to +3.3V
GND	3	□ □	4 B12	JTAG TMS	3	□ □	4 JTAG TDO (PMC)
B13	5	□ □	6 B14	JTAG TDI (PMC)	5	□ □	6 GND
A15	7	□ □	8 NC	GND	7	□ □	8 F7
B15	9	□ □	10 A16	G6	9	□ □	10 G18
GND	11	□ □	12 B16	H17	11	□ □	12 +3.3V
Clk from APEX (U5 pin 18)	13	□ □	14 GND	reset_n	13	□ □	14 F22
GND	15	□ □	16 A17	+3.3V	15	□ □	16 H22
B17	17	□ □	18 NC	H20	17	□ □	18 GND
NC	19	□ □	20 A18	F1	19	□ □	20 H1
B18	21	□ □	22 A19	GND	21	□ □	22 L8
B19	23	□ □	24 GND	G2	23	□ □	24 +3.3V
GND	25	□ □	26 A20	H3	25	□ □	26 H18
D21	27	□ □	28 E21	+3.3V	27	□ □	28 H21
A21	29	□ □	30 NC	H19	29	□ □	30 GND
NC	31	□ □	32 F21	G22	31	□ □	32 J16
C22	33	□ □	34 GND	GND	33	□ □	34 G4
GND	35	□ □	36 C12	J4	35	□ □	36 +3.3V
D22	37	□ □	38 B20	GND	37	□ □	38 K7
GND	39	□ □	40 C21	G5	39	□ □	40 GND
C20	41	□ □	42 D19	+3.3V	41	□ □	42 G1
C13	43	□ □	44 GND	J17	43	□ □	44 GND
NC	45	□ □	46 E18	G21	45	□ □	46 L21
D20	47	□ □	48 G19	GND	47	□ □	48 B9
E19	49	□ □	50 NC	J21	49	□ □	50 +3.3V
GND	51	□ □	52 F19	J22	51	□ □	52 H6
E5	53	□ □	54 M7	+3.3V	53	□ □	54 H4
E22	55	□ □	56 GND	H2	55	□ □	56 GND
NC	57	□ □	58 G20	L3	57	□ □	58 K6
F20	59	□ □	60 F18	GND	59	□ □	60 J19
E20	61	□ □	62 NC	J20	61	□ □	62 +3.3V
GND	63	□ □	64 G3	GND	63	□ □	64 K21

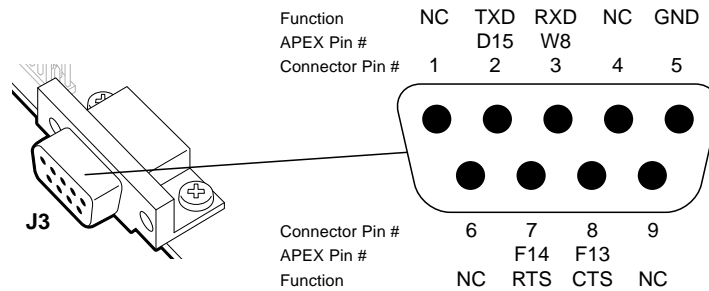


## Serial Port Connector

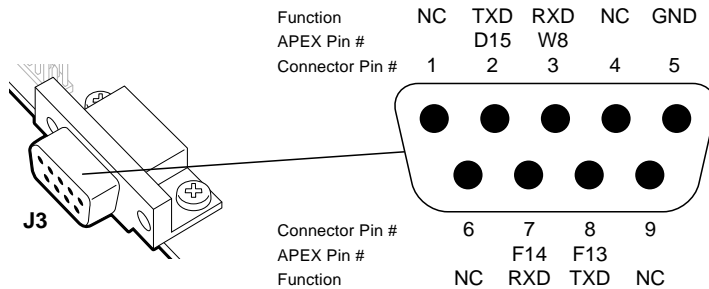
J3 is a standard DB-9 serial connector. This connector is typically used for host communication with a desktop workstation. Using a standard 9-pin serial cable connected to (for example) a COM-port. The transmit (TXD) from Nios, receive (RXD) by Nios, clear to send (CTS) and ready to send (RTS) signals use standard high-voltage RS-232 logic levels. U13 is a level-shifting buffer that presents or accepts 3.3-V versions of these signals to and from the APEX device.

The Nios 2.1 development kit includes a serial Y cable to support an on-chip debug peripheral. Figure 10 shows the pinout information on a design using a single UART with hardware handshaking and Figure 11 shows the pinout information on a design using both a communication UART and a separate debug UART.

**Figure 10. Serial Port Connector - UART with Hardware Handshaking**



**Figure 11. Serial Port Connector - 2 UARTs with no Hardware Handshaking**



## JTAG Connector

JP3 is a 10-pin JTAG interface connector compatible with Altera ByteBlaster II and MasterBlaster download cables. The JTAG connection can be used for any of three purposes:

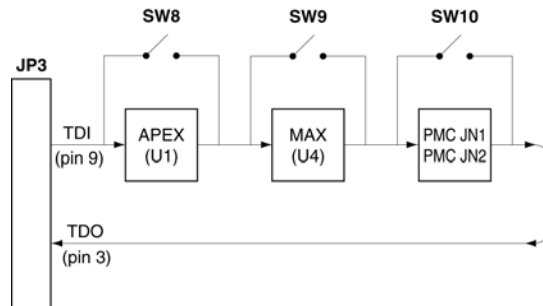
1. Quartus II software can configure the APEX device (U1) with a new bitstream (such as .sof) file via a MasterBlaster or ByteBlaster II download cable.
2. Quartus II or MAX+PLUS® II software can re-program the EPM7064 device (U4) with a new .pof file via a MasterBlaster or ByteBlaster II download cable.
3. User-provided host software can conduct JTAG serial communication with a card plugged into the PMC connectors (PMCJN1 and PMCJN2) if the card makes use of the JTAG signals that are part of the IEEE-1386 standard.

The JTAG chain on the Nios development board can include all, some, or none of the following devices, in order:

1. (SW8) The APEX device (U1)
2. (SW9) The EPM7064 configuration controller (U4)
3. (SW10) A card plugged into the PMC connectors PMCJN1 and PMCJN2, if present.

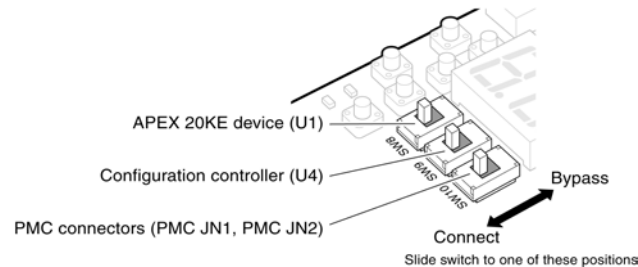
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**Figure 12. JTAG Chain**




See [Figure 1 on page 3](#) for precise and complete connections information.

For each device the indicated two-position connect/bypass switch determines whether the device is included in the JTAG chain (connect) or excluded (bypass).

**Figure 13. Two-Position Switches**

The JTAG connection is most commonly used to download user configuration (such as .sof) files to the APEX device chip during logic development and debugging. In this case, it is usually most convenient to leave SW8 in the connect position, and both SW9 and SW10 in the bypass position.

The EPM7064 device (U4) comes factory-programmed as a configuration controller. See [“Factory and User Configurations” on page 16](#). MAX+PLUS II projects that include the design, implementation, and programming files for the configuration-controller logic are included with the Nios embedded processor software. Most users will never need to re-program the configuration controller (U4).

 Re-programming U4 may result in an inoperable development board. Altera recommends that users leave SW9 and SW10 set to bypass.

## Configuration Controller

The configuration controller (U4), is an Altera EPM7064 PLD. It comes factory-programmed with logic that configures the APEX device (U1) from data stored in flash (U3) on power-up. At power-up (or when the reset switch SW2 is pressed), the configuration controller begins reading data out of the flash memory. The flash memory, APEX device, and configuration controller are connected so that data from the flash configures the APEX device in passive-parallel mode. See [“SW2: Reset” on page 18](#).

### Configuration Data

The Quartus II software can (optionally) produce hexout configuration files that are directly suitable for download and storage in the flash memory as configuration data. A hexout configuration file for the APEX20K200E device (U1) is a little less than 256 Kbytes, and thus occupies about 1/4 of the flash memory (U3).

New hexout files can be stored in the flash memory (U3) by software running on a Nios processor. The preloaded 32-bit Nios reference design includes the GERMS monitor program, which supports downloading hexout files from a host (such as desktop workstation) into flash memory.



See the *Nios Embedded Processor Software Development Reference Manual* for a detailed description of the GERMS monitor program.

## Factory and User Configurations

The configuration controller can manage two separate APEX device configurations stored in flash memory. These two configurations (hexout-files) are conventionally referred to as the *user configuration* and the *factory configuration*. Upon reset (or when the reset switch (SW2) is pressed) the configuration controller will attempt to load the APEX device with user configuration data. If this process fails (either because the user-configuration is invalid or not present) the configuration controller will then load the APEX device with factory configuration data.

The configuration controller expects user-configuration and factory-configuration files to be stored at fixed locations (offsets) in flash memory. [Table 2](#) shows how the configuration controller expects flash memory contents to be arranged.

0x100000 – 0x17FFFF	512 Kbytes	Nios instruction and nonvolatile data space.
0x180000 – 0x1BFFFF	256 Kbytes	User-defined APEX device configuration data.
0x1C0000 – 0x1FFFFFF	256 Kbytes	Factory-default APEX device configuration. See <a href="#">“Configuration Controller” on page 15.</a>

The 32-bit Nios reference design is pre-loaded into the factory-configuration region of the flash memory. Altera recommends that users avoid overwriting the factory configuration data.

The jumper (JP2) changes the behavior of the configuration controller. If a shorting block is present on JP2, the configuration controller will ignore the user-configuration and always configure the APEX device from the factory configuration. By shorting JP2, you can “escape” from the situation where a valid-but-nonfunctional user configuration is present in flash memory.



In the pre-loaded Nios reference design, the 1 Mbyte flash memory is mapped at base-address 0x100000. Thus, user hexout-files should be downloaded to address 0x180000 (= flash-base-address + user-configuration offset).

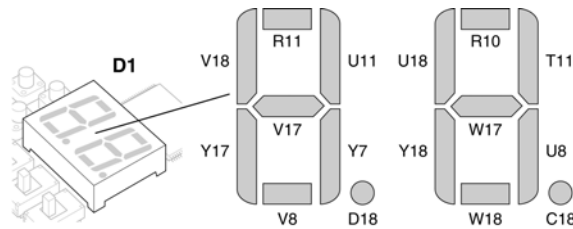


See the *Nios Embedded Processor Software Development Reference Manual* for detailed information about downloading and relocating files using the GERMS monitor.

## Two-Digit 7-segment display (D1)

D1 is connected to the APEX device so that each segment is individually controlled by a general-purpose I/O pin.

**Figure 14. Dual-Digit Display**

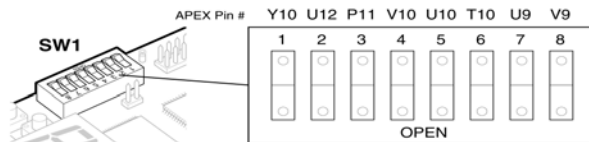


The pre-loaded Nios reference design includes parallel input/output (PIO) registers and logic for driving this display.

## Switches, Buttons, and LEDs

SW1 is an 8-DIP-switch block with each switch connected to an APEX general-purpose I/O and a pull-up resistor. The APEX device will see a logic-1 when each switch is open, and a logic-0 when each switch is closed.

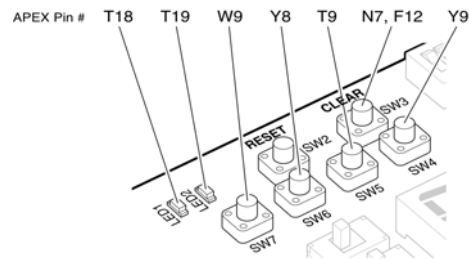
**Figure 15. Eight Dip Switch Block**



SW4, SW5, SW6, and SW7 are momentary-contact push-button switches, each connected to an APEX device general-purpose I/O and a pull-up resistor. The APEX device will see a logic-0 when each switch is pressed. Discrete LEDs LED1 and LED2 are each controlled by an APEX device general-purpose I/O. Each LED will light-up when the APEX device drives a logic-1 on its controlling output.

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**Figure 16. Switches and LEDs**



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The Nios development board uses dedicated switches SW2 and SW3 for the following fixed functions:

### **SW2: Reset**

When SW2 is pressed, a logic-0 value is driven to U7, the power-on reset controller. Pressing SW2 is equivalent to a power-on reset. When SW2 is pressed (or when the board is power-cycled), the configuration controller will load the APEX device from flash memory. See [“Configuration Controller” on page 15](#) for more information.

When the development board is delivered from the factory, the APEX device will be configured with the 32-bit reference design at power-up (or when SW2 is pressed). The reference design will then begin executing the GERMS monitor, a serial debug/download utility.

### **SW3: Clear**

When SW3 is pressed, a logic-0 is driven onto the APEX devices' DEV\_CLRn pin (and user I/O F12). The result of pressing SW3 depends on how the APEX device is currently configured.

The pre-loaded Nios reference design treats SW3 as a CPU-reset pin: The reference Nios CPU will reset and start executing code from its boot-address (0) when SW3 is pressed.

## Power-supply circuitry

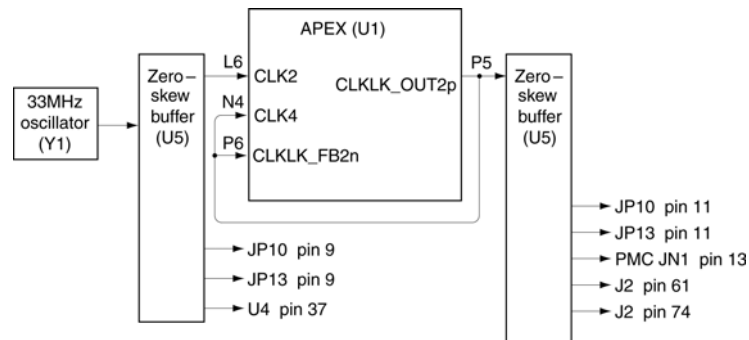
The Nios development board runs from a 9-V, unregulated, center-negative input. On-board circuitry generates 5-V, 3.3-V, and 1.8-V regulated power levels.

- The 1.8-V supply is used only for the APEX device core power source and it is not available on any connector or header.
- The 3.3-V supply is used as the power source for all APEX device I/O pins. The 3.3-V supply is also available to daughter cards or other devices plugged into any of the expansion connectors, including the PMC connectors and the SDRAM SODIMM socket. The total load from all externally-connected 3.3-V devices may not exceed 500 mA.
- The 5-V supply is presented on pin 2 of JP12 for use by any devices plugged into the 5-V-tolerant expansion connectors. The total load may not exceed 50 mA.

## Clock Circuitry

The Nios development board includes a 33.333 MHz free-running oscillator and a zero-skew, point-to-point clock distribution network that drives both the APEX device and pins on the expansion connectors, PMC connectors, and SODIMM connector. The zero-skew buffer distributes both the free-running 33 MHz clock and the clock-output from one of the APEX's device internal PLLs (CLKLK\_OUT1).

**Figure 17. Clock Circuitry**



## Board Component List

D1	Dual-digit 7-segment LED
J1	Power supply connector
J2	SDRAM SODIMM socket
J3	Serial port connector
PMCJN1	PMC connector
PMCJN2	PMC connector
JP2	Jumper header for configuration controller
JP3	JTAG header
JP8	40-pin header for 3.3 volt daughter card
JP9	14-pin header for 3.3 volt daughter card
JP10	20-pin header for 3.3 volt daughter card
JP11	40-pin header for 5 volt daughter card
JP12	14-pin header for 5 volt daughter card
JP13	20-pin header for 5 volt daughter card
JP14	6-pin header for serial debug
JP3	JTAG header
LED1	User-controllable LED
LED2	User-controllable LED
LED3	Flash-byte LED
LED7	Power indication LED
SW1	8-bit DIP switch block
SW2	Resets the board—clears the APEX device and reloads from the configuration controller
SW3	Clears the CPU
SW4	User-defined push-button
SW5	User-defined push-button
SW6	User-defined push-button
SW7	User-defined push-button
SW8	APEX device JTAG chain switch
SW9	Configuration controller JTAG chain switch
SW10	PMC JTAG chain switch
TP1	Ground point providing a ground plane reference
TP2	Ground point providing a ground plane reference
TP3	Ground point providing a ground plane reference

**Table 3. Nios Development Board Components (Part 2 of 2)**

TP4	Ground point providing a ground plane reference
U1	APEX EP20K200E device
U3	Flash memory device
U4	APEX device configuration controller
U5	Clock distribution chip
U7	Monitor reset
U13	RS-232 level-shifter
U14	SRAM
U15	SRAM
Y1	Programmable high-frequency oscillator

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