SBAS267 – MARCH 2003

Precision Analog-to-Digital Converter (ADC) and Digital-to-Analog Converters (DACs) with 8051 Microcontroller and Flash Memory

FEATURES

ANALOG FEATURES

- 24-BITS NO MISSING CODES
- 22-BITS EFFECTIVE RESOLUTION AT 10Hz
  Low Noise: 75nV
- PGA FROM 1 TO 128
- PRECISION ON-CHIP VOLTAGE REFERENCE:
  Accuracy: 0.2%
  Drift: 5ppm/°C
- 8 DIFFERENTIAL/SINGLE-ENDED CHANNELS
- ON-CHIP OFFSET/GAIN CALIBRATION
- OFFSET DRIFT: 0.02PPM/°C
- GAIN DRIFT: 0.5PPM/°C
- ON-CHIP TEMPERATURE SENSOR
- SELECTABLE BUFFER INPUT
- BURNOUT DETECT
- QUAD 16-BIT MONOTONIC VOLTAGE DACs:
  2 VDACs Can Be Programmed as IDACs
  8μs Settling Time

DIGITAL FEATURES

Microcontroller Core

- 8051 COMPATIBLE
- HIGH SPEED CORE:
  4 Clocks per Instruction Cycle
- DC TO 30MHz
- SINGLE INSTRUCTION 133ns
- DUAL DATA POINTER

Memory

- UP TO 32kB FLASH DATA MEMORY
- FLASH MEMORY PARTITIONING
- ENDURANCE 1M ERASE/WRITE CYCLES,
  100 YEAR DATA RETENTION
- IN-SYSTEM SERIALLY PROGRAMMABLE
- EXTERNAL PROGRAM/DATA MEMORY (64kB)
- 1280 BYTES DATA SRAM
- FLASH MEMORY SECURITY
- 2kB BOOT ROM
- PROGRAMMABLE WAIT STATE CONTROL

Peripheral Features

- 34 I/O PINS
- ADDITIONAL 32-BIT ACCUMULATOR
- THREE 16-BIT TIMER/COUNTERS
- SYSTEM TIMERS
- PROGRAMMABLE WATCHDOG TIMER
- FULL DUPLEX DUAL UART
- MASTER/SLAVE SPI™ WITH DMA
- MULTI-MASTER I²C™
- 16-BIT PWM
- POWER MANAGEMENT CONTROL
- INTERNAL CLOCK DIVIDER
- IDLE MODE CURRENT < 200μA
- STOP MODE CURRENT < 100nA
- PROGRAMMABLE BROWNOUT RESET
- PROGRAMMABLE LOW VOLTAGE DETECT
- 21 INTERRUPT SOURCES
- TWO HARDWARE BREAKPOINTS

GENERAL FEATURES

- PIN COMPATIBLE WITH MSC1210 FAMILY
- PACKAGE: TQFP-64
- LOW POWER: 4mW
- INDUSTRIAL TEMPERATURE RANGE:
  –40°C to +85°C
- POWER SUPPLY: 2.7V to 5.25V

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS
- INTELLIGENT SENSORS
- PORTABLE APPLICATIONS
- DAS SYSTEMS

PACKAGE/ORDERING INFORMATION

PRODUCT	FLASH MEMORY	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
MSC1211Y2	4k	TQFP-64	PAG	–40°C to +85°C	MSC1211Y2	MSC1211Y2PAGT	Tape and Reel, 250
MSC1211Y2	4k	"	"	"	"	MSC1211Y2PAGR	Tape and Reel, 2000
MSC1211Y3	8k	TQFP-64	PAG	–40°C to +85°C	MSC1211Y3	MSC1211Y3PAGT	Tape and Reel, 250
MSC1211Y3	8k	"	"	"	"	MSC1211Y3PAGR	Tape and Reel, 2000
MSC1211Y4	16k	TQFP-64	PAG	–40°C to +85°C	MSC1211Y4	MSC1211Y4PAGT	Tape and Reel, 250
MSC1211Y4	16k	"	"	"	"	MSC1211Y4PAGR	Tape and Reel, 2000
MSC1211Y5	32k	TQFP-64	PAG	–40°C to +85°C	MSC1211Y5	MSC1211Y5PAGT	Tape and Reel, 250
MSC1211Y5	32k	"	"	"	"	MSC1211Y5PAGR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com/msc.

ABSOLUTE MAXIMUM RATINGS(1)

Analog Inputs
- Input Current ..... 100mA, Momentary
- Input Current ..... 10mA, Continuous
- Input Voltage ..... AGND – 0.5V to AV_{DD} + 0.5V

Power Supply
- DV_{DD} to DGND ..... –0.3V to 6V
- AV_{DD} to AGND ..... –0.3V to 6V
- AGND to DGND ..... –0.3V to +0.3V
- V_{REF} to AGND ..... –0.3V to AV_{DD} + 0.3V
- Digital Input Voltage to DGND ..... –0.3V to DV_{DD} + 0.3V
- Digital Output Voltage to DGND ..... –0.3V to DV_{DD} + 0.3V
- Maximum Junction Temperature ..... +150°C
- Operating Temperature Range ..... –40°C to +85°C
- Storage Temperature Range ..... –65°C to +150°C
- Lead Temperature (soldering, 10s) ..... +300°C
- Package Power Dissipation 900mW
- Output Current All Pins 200mA
- Output Pin Short Circuit 10s
- Thermal Resistance, Junction-to-Ambient (θ_{JA}) ..... 66.6°C/W
- Thermal Resistance, Junction-to-Case (θ_{JC}) ..... 4.3°C/W

Digital Outputs
- Output Current ..... 100mA, Continuous
- I/O Source/Sink Current 100mA
- Power Pin Maximum 300mA

NOTE: (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MSC1211YX FAMILY FEATURES

FEATURES(1)	MSC1211Y2(2)	MSC1211Y3(2)	MSC1211Y4(2)	MSC1211Y5(2)
Flash Program Memory (Bytes)	Up to 4k	Up to 8k	Up to 16k	Up to 32k
Flash Data Memory (Bytes)	Up to 4k	Up to 8k	Up to 16k	Up to 32k
Internal Scratchpad RAM (Bytes)	256	256	256	256
Internal MOVX SRAM (Bytes)	1024	1024	1024	1024
Externally Accessible Memory (Bytes)	64k Program, 64k Data	64k Program, 64k Data	64k Program, 64k Data	64k Program, 64k Data

NOTES: (1) All peripheral features are the same on all devices; the flash memory size is the only difference. (2) The last digit of the part number (N) represents the onboard flash size = (2^N)kBytes.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise noted. For V_{DAC}, $V_{REF} = AV_{DD}$, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER	CONDITION	MSC1211Yx MIN	MSC1211Yx TYP	MSC1211Yx MAX	UNITS
ANALOG INPUT (AIN0-AIN7, AINCOM)					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 50mV		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Figure 4			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance	Buffer ON		4		pF
Input Leakage Current	Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources	Sensor Input Open Circuit		±2		µA
ADC OFFSET DAC					
Offset DAC Range			$\pm V_{REF}/(2 \cdot PGA)$		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.5		% of Range
Offset DAC Gain Error Drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
ENOB			22		Bits
Output Noise			See Typical Characteristics		
No Missing Codes	$Sinc^3$ Filter	24			Bits
Integral Nonlinearity	End Point Fit, Differential Input			±0.0015	%FSR
Offset Error	After Calibration		7.5		ppm of FS
Offset Drift(1)	Before Calibration		0.02		ppm of FS/°C
Gain Error(2)	After Calibration		0.005		%
Gain Error Drift(1)	Before Calibration		0.5		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		–50		50	% of FS
Common-Mode Rejection	At DC	100	115		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = $-20\log(\Delta V_{OUT}/\Delta V_{DD})$(3)		88		dB
VOLTAGE REFERENCE INPUTS					
Reference Input Range	REF IN+, REF IN–	0.0		AV_{DD}(2)	V
ADC V_{REF}	$V_{REF} \equiv$ (REF IN+) – (REF IN–)	0.3	2.5	AV_{DD}	V
Common-Mode Rejection	At DC		110		dB
Input Current(4)	V_{REF} = 2.5V, ADC Only		10		µA
DAC Reference Current	For Each DAC, 5V Reference		25		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	VREFH = 1 at +25°C, PGA = 1, 2, 4, 8	2.495	2.5	2.505	V
	VREFH = 0		1.25		V
Power-Supply Rejection Ratio			65		dB
Short-Circuit Current Source			8		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Output Impedance	Sourcing 100µA		3		Ω
Startup Time from Power ON	C_{REFOUT} = 0.1µF		8		ms
Temperature Sensor					
Temperature Sensor Voltage	T = +25°C		115		mV
Temperature Sensor Coefficient			375		µV/°C
VOLTAGE DAC STATIC PERFORMANCE(5)					
Resolution		16			Bits
Relative Accuracy			±0.05	±0.146	%
Differential Nonlinearity				±1	LSB
Zero Code Error	All 0s Loaded to DAC Register		+13	+35	mV
Full-Scale Error	All 1s Loaded to DAC Register	–1.25	0		% of FSR
Gain Error		–1.25	0	+1.25	% of FSR
Zero Code Error Drift			±20		µV/°C
Gain Temperature Coefficient			±5		ppm of FSR/°C

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V (Cont.)

All specifications from T_{MIN} to T_{MAX}, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER		CONDITION	MSC1211Yx MIN	MSC1211Yx TYP	MSC1211Yx MAX	UNITS
VOLTAGE DAC OUTPUT CHARACTERISTICS[6]						
Output Voltage Range			AGND		AV_{DD}	V
Output Voltage Settling Time		To ±0.003% FSR, 0200_H to $FD00_H$		8		µs
Slew Rate				1		V/µs
DC Output Impedance				7		Ω
Short-Circuit Current		All 1s Loaded to DAC Register		20		mA
IDAC OUTPUT CHARACTERISTICS						
Full-Scale Output Current		Maximum V_{REF} = 2.5V		25		mA
Maximum Short-Circuit Current Duration				Indefinite		
Compliance Voltage				AV_{DD} – 1.5		V
Relative Accuracy		Over Full Range		0.185		% of FSR
Zero Code Error				0.5		% of FSR
Full-Scale Error				–0.4		% of FSR
Gain Error				–0.6		% of FSR
ANALOG POWER-SUPPLY REQUIREMENTS						
Power-Supply Voltage		AV_{DD}	4.75		5.25	V
Analog Current	I_{ADC} + I_{VREF}	Analog OFF, PDAD = 1		< 1		nA
ADC Current	I_{ADC}	PGA = 1, Buffer OFF		200		µA
		PGA = 128, Buffer OFF		500		µA
		PGA = 1, Buffer ON		240		µA
		PGA = 128, Buffer ON		850		µA
VDAC Current	I_{VDAC}	Excluding Load Current External Reference		250		µA
V_{REF} Supply Current	I_{VREF}	ADC ON, V_{DAC} OFF		250		µA

NOTES: (1) Calibration can minimize these errors. (2) The gain calibration cannot have a REF IN+ of more than AV_{DD} – 1.5V with buffer ON. To calibrate gain, turn buffer off. (3) DV_{OUT} is change in digital result. (4) 12pF switched capacitor at f_{SAMP} clock frequency (see Figure 6). (5) Linearity calculated using a reduced code range of 512 to 65024; output unloaded. (6) Ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications from T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, Bipolar, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +1.25V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER	CONDITION	MSC1211Yx MIN	MSC1211Yx TYP	MSC1211Yx MAX	UNITS
ANALOG INPUT (AIN0-AIN7, AINCOM)					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 50mV		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Figure 4			$\pm V_{REF}$/PGA	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
Fast Settling Filter	–3dB		0.469 • f_{DATA}		
$Sinc^2$ Filter	–3dB		0.318 • f_{DATA}		
$Sinc^3$ Filter	–3dB		0.262 • f_{DATA}		
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance	Buffer On		4		pF
Input Leakage Current	Multiplexer Channel Off, T = +25°C		0.5		pA
Burnout Current Sources	Sensor Input Open Circuit		±2		µA
ADC OFFSET DAC					
Offset DAC Range			$\pm V_{REF}/(2 \cdot PGA)$		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±1.5		% of Range
Offset DAC Gain Error Drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
ENOB			22		Bits
Output Noise			See Typical Characteristics		
No Missing Codes	$Sinc^3$ Filter	24			Bits
Integral Nonlinearity	End Point Fit, Differential Input			±0.0015	%FSR
Offset Error	After Calibration		7.5		ppm of FS
Offset Drift[1]	Before Calibration		0.02		ppm of FS/°C
Gain Error[2]	After Calibration		0.005		%
Gain Error Drift[1]	Before Calibration		1.0		ppm/°C
System Gain Calibration Range		80		120	% of FS
System Offset Calibration Range		–50		50	% of FS

ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V (Cont.)

All specifications from T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 15.625kHz, PGA = 1, Buffer ON, f_{DATA} = 10Hz, and Bipolar, $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +1.25V, unless otherwise noted. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

PARAMETER	CONDITION	MSC1211Yx MIN	MSC1211Yx TYP	MSC1211Yx MAX	UNITS
SYSTEM PERFORMANCE (Cont.)					
Common-Mode Rejection	At DC	100	115		dB
	f_{CM} = 60Hz, f_{DATA} = 10Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 50Hz		120		dB
	f_{CM} = 60Hz, f_{DATA} = 60Hz		120		dB
Normal Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 50Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 60Hz		100		dB
Power-Supply Rejection	At DC, dB = –20log(DV_{OUT}/DV_{DD})(3)		85		dB
VOLTAGE REFERENCE INPUTS					
Reference Input Range	REF IN+, REF IN–	0.0		AV_{DD}(2)	V
ADC V_{REF}	$V_{REF} \equiv$ (REF IN+) – (REF IN–)	0.3	1.25	AV_{DD}	V
Common-Mode Rejection	At DC		110		dB
Input Current(4)	V_{REF} = 1.25V, ADC Only		10		µA
DAC Reference Current	For each DAC, 3V Reference		25		µA
ON-CHIP VOLTAGE REFERENCE					
Output Voltage	VREFH = 0 at +25°C, PGA = 1, 2, 4, 8	1.245	1.25	1.255	V
Power-Supply Rejection Ratio			65		dB
Short-Circuit Current Source			2.6		mA
Short-Circuit Current Sink			50		µA
Short-Circuit Duration	Sink or Source		Indefinite		
Drift			5		ppm/°C
Output Impedance	Sourcing 100µA		3		Ω
Startup Time from Power ON	C_{REFOUT} = 0.1µF		8		ms
Temperature Sensor					
Temperature Sensor Voltage	T = +25°C		115		mV
Temperature Sensor Coefficient			375		µV/°C
VOLTAGE DAC STATIC PERFORMANCE(5)					
Resolution		16			Bits
Relative Accuracy			±0.05	±0.146	% of FSR
Differential Nonlinearity	Ensured Monotonic by Design			±1	LSB
Zero Code Error	All 0s Loaded to DAC Register		+13	+35	mV
Full-Scale Error	All 1s Loaded to DAC Register	–1.25	0		% of FSR
Gain Error		–1.25	0	±1.25	% of FSR
Zero Code Error Drift			±20		µV/°C
Gain Temperature Coefficient			±5		ppm of FSR/°C
VOLTAGE DAC OUTPUT CHARACTERISTICS(6)					
Output Voltage Range		AGND		AV_{DD}	V
Output Voltage Settling Time	To ±0.003% FSR, 0200_H to $FD00_H$		8		µs
Slew Rate			1		V/µs
DC Output Impedance			7		Ω
Short-Circuit Current	All 1s Loaded to DAC Register		16		mA
IDAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current	Maximum V_{REF} = 2.5V		25		mA
Maximum Short-Circuit Current Duration			Indefinite		
Compliance Voltage			AV_{DD} – 1.5		
Relative Accuracy	Over Full Range		0.185		% of FSR
Zero Code Error			0.5		% of FSR
Full-Scale Error			–0.4		% of FSR
Gain Error			–0.6		% of FSR
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	2.7		3.6	V
Analog Current $I_{ADC} + I_{VREF}$	Analog OFF, PDAD = 1		< 1		nA
ADC Current I_{ADC}	PGA = 1, Buffer OFF		200		µA
	PGA = 128, Buffer OFF		500		µA
	PGA = 1, Buffer ON		240		µA
	PGA = 128, Buffer ON		850		µA
VDAC Current I_{VDAC}	Excluding Load Current External Reference		250		µA
V_{REF} Current I_{VREF}			250		µA

NOTES: (1) Calibration can minimize these errors. (2) The gain calibration cannot have a REF IN+ of more than AV_{DD} – 1.5V with buffer ON. To calibrate gain, turn buffer off. (3) DV_{OUT} is change in digital result. (4) 12pF switched capacitor at f_{SAMP} clock frequency (see Figure 6). (5) Linearity calculated using a reduced code range of 512 to 65024; output unloaded. (6) Ensured by design and characterization, not production tested.

DIGITAL CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

All specifications from T_{MIN} to T_{MAX}, unless otherwise specified.

PARAMETER	CONDITION	MSC1211Yx MIN	MSC1211Yx TYP	MSC1211Yx MAX	UNITS
POWER-SUPPLY REQUIREMENTS					
	DV_{DD}	2.7		3.6	V
	Normal Mode, f_{OSC} = 1MHz		1.3		mA
	Normal Mode, f_{OSC} = 8MHz		6		mA
	Stop Mode		100		nA
	DV_{DD}	4.75		5.25	V
	Normal Mode, f_{OSC} = 1MHz		2.2		mA
	Normal Mode, f_{OSC} = 8MHz		14		mA
	Stop Mode		100		nA
DIGITAL INPUT/OUTPUT (CMOS)					
Logic Level: V_{IH} (except XIN pin)		0.6 • DV_{DD}		DV_{DD}	V
V_{IL} (except XIN pin)		DGND		0.2 • DV_{DD}	V
Ports 0-3, Input Leakage Current, Input Mode	V_{IH} = DV_{DD} or V_{IH} = 0V	–10	0	+10	µA
Pins $\overline{EA}$, XIN Input Leakage Current			0		µA
V_{OL}, ALE, $\overline{PSEN}$, Ports 0-3, All Output Modes	I_{OL} = 1mA	DGND		0.4	V
V_{OL}, ALE, $\overline{PSEN}$, Ports 0-3, All Output Modes	I_{OL} = 30mA, 3V (20mA)		1.5		V
V_{OH}, ALE, $\overline{PSEN}$, Ports 0-3, Strong Drive Output	I_{OH} = 1mA	DV_{DD} – 0.4	DV_{DD} – 0.1	DV_{DD}	V
V_{OH}, ALE, $\overline{PSEN}$, Ports 0-3, Strong Drive Output	I_{OH} = 30mA, 3V (20mA)		DV_{DD} – 1.5		V
Ports 0-3 Pull-Up Resistors			9		kΩ
Pins ALE, $\overline{PSEN}$, Pull-Up Resistors	Flash Programming Mode Only		9		kΩ
Pin RST, Pull-Down Resistor			200		kΩ

FLASH MEMORY CHARACTERISTICS: DV_{DD} = 2.7V to 5.25V

t_{USEC} = 1µs, t_{MSEC} = 1ms

PARAMETER	CONDITION	MSC1211Yx MIN	MSC1211Yx TYP	MSC1211Yx MAX	UNITS
Flash Memory Endurance		100,000	1,000,000		cycles
Flash Memory Data Retention		100			Years
Mass and Page Erase Time	Set with FER Value in FTCON	10			ms
Flash Memory Data Retention	Set with FWR Value in FTCON	30		40	µs

AC ELECTRICAL CHARACTERISTICS[1][2]: DV_{DD} = 2.7V to 5.25V

SYMBOL	FIGURE	PARAMETER	2.7V to 3.6V MIN	2.7V to 3.6V MAX	4.75V to 5.25V MIN	4.75V to 5.25V MAX	UNITS
System Clock							
f_{OSC}[3]	D	External Crystal Frequency (f_{OSC})	1	16	1	30	MHz
$1/t_{OSC}$[3]	D	External Clock Frequency (f_{OSC})	0	16	1	30	MHz
f_{OSC}[3]	D	External Ceramic Resonator Frequency (f_{OSC})	1	12	1	12	MHz
Program Memory							
t_{LHLL}	A	ALE Pulse Width	$1.5t_{CLK} - 5$		$1.5t_{CLK} - 5$		ns
t_{AVLL}	A	Address Valid to ALE LOW	$0.5t_{CLK} - 10$		$0.5t_{CLK} - 7$		ns
t_{LLAX}	A	Address Hold After ALE LOW	$0.5t_{CLK}$		$0.5t_{CLK}$		ns
t_{LLIV}	A	ALE LOW to Valid Instruction In		$2.5t_{CLK} - 35$		$2.5t_{CLK} - 25$	ns
t_{LLPL}	A	ALE LOW to $\overline{PSEN}$ LOW	$0.5t_{CLK}$		$0.5t_{CLK}$		ns
t_{PLPH}	A	$\overline{PSEN}$ Pulse Width	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
t_{PLIV}	A	$\overline{PSEN}$ LOW to Valid Instruction In		$2t_{CLK} - 40$		$2t_{CLK} - 30$	ns
t_{PXIX}	A	Input Instruction Hold After $\overline{PSEN}$	5		–5		ns
t_{PXIZ}	A	Input Instruction Float After $\overline{PSEN}$		$t_{CLK} - 5$		t_{CLK}	ns
t_{AVIV}	A	Address to Valid Instruction In		$3t_{CLK} - 40$		$3t_{CLK} - 25$	ns
t_{PLAZ}	A	$\overline{PSEN}$ LOW to Address Float		0		0	ns
Data Memory							
t_{RLRH}	B	$\overline{RD}$ Pulse Width ($t_{MCS} = 0$)[4]	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
	B	$\overline{RD}$ Pulse Width ($t_{MCS} > 0$)[4]	$t_{MCS} - 5$		$t_{MCS} - 5$		ns
t_{WLWH}	C	$\overline{WR}$ Pulse Width ($t_{MCS} = 0$)[4]	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
	C	Pulse Width ($t_{MCS} > 0$)[4]	$t_{MCS} - 5$		$t_{MCS} - 5$		ns
t_{RLDV}	B	$\overline{RD}$ LOW to Valid Data In ($t_{MCS} = 0$)[4]		$2t_{CLK} - 40$		$2t_{CLK} - 30$	ns
	B	$\overline{RD}$ LOW to Valid Data In ($t_{MCS} > 0$)[4]		$t_{MCS} - 40$		$t_{MCS} - 30$	ns
t_{RHDX}	B	Data Hold After Read	–5		–5		ns
t_{RHDZ}	B	Data Float After Read ($t_{MCS} = 0$)[4]		t_{CLK}		t_{CLK}	ns
	B	Data Float After Read ($t_{MCS} > 0$)[4]		$2t_{CLK}$		$2t_{CLK}$	ns
t_{LLDV}	B	ALE LOW to Valid Data In ($t_{MCS} = 0$)[4]		$2.5t_{CLK} - 40$		$2.5t_{CLK} - 25$	ns
	B	ALE LOW to Valid Data In ($t_{MCS} > 0$)[4]		$t_{CLK} + t_{MCS} - 40$		$t_{CLK} + t_{MCS} - 25$	ns
t_{AVDV}	B	Address to Valid Data In ($t_{MCS} = 0$)[4]		$3t_{CLK} - 40$		$3t_{CLK} - 25$	ns
	B	Address to Valid Data In ($t_{MCS} > 0$)[4]		$1.5t_{CLK} + t_{MCS} - 40$		$1.5t_{CLK} + t_{MCS} - 25$	ns
t_{LLWL}	B, C	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW ($t_{MCS} = 0$)[4]	$0.5t_{CLK} - 5$	$0.5t_{CLK} + 5$	$0.5t_{CLK} - 5$	$0.5t_{CLK} + 5$	ns
	B, C	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW ($t_{MCS} > 0$)[4]	$t_{CLK} - 5$	$t_{CLK} + 5$	$t_{CLK} - 5$	$t_{CLK} + 5$	ns
t_{AVWL}	B, C	Address to $\overline{RD}$ or $\overline{WR}$ LOW ($t_{MCS} = 0$)[4]	$t_{CLK} - 5$		$t_{CLK} - 5$		ns
	B, C	Address to $\overline{RD}$ or $\overline{WR}$ LOW ($t_{MCS} > 0$)[4]	$2t_{CLK} - 5$		$2t_{CLK} - 5$		ns
t_{QVWX}	C	Data Valid to $\overline{WR}$ Transition	–8		–5		ns
t_{WHQX}	C	Data Hold After $\overline{WR}$	$t_{CLK} - 8$		$t_{CLK} - 5$		ns
t_{RLAZ}	B	$\overline{RD}$ LOW to Address Float		$-0.5t_{CLK} - 5$		$-0.5t_{CLK} - 5$	ns
t_{WHLH}	B, C	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH ($t_{MCS} = 0$)[4]	–5	5	–5	5	ns
	B, C	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH ($t_{MCS} > 0$)[4]	$t_{CLK} - 5$	$t_{CLK} + 5$	$t_{CLK} - 5$	$t_{CLK} + 5$	ns
External Clock							
t_{HIGH}	D	HIGH Time[5]	15		10		ns
t_{LOW}	D	LOW Time[5]	15		10		ns
t_R	D	Rise Time[5]		5		5	ns
t_F	D	Fall Time[5]		5		5	ns

NOTES: (1) Parameters are valid over operating temperature range, unless otherwise specified. (2) Load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF. (3) $t_{CLK} = 1/f_{OSC}$ = one oscillator clock period for clock divider = 1. (4) t_{MCS} is a time period related to the Stretch MOVX selection. The following table shows the value of t_{MCS} for each stretch selection. (5) These values are characterized but not 100% production tested.

MD2	MD1	MD0	MOVX DURATION	t_{MCS}
0	0	0	2 Machine Cycles	0
0	0	1	3 Machine Cycles (default)	$4t_{CLK}$
0	1	0	4 Machine Cycles	$8t_{CLK}$
0	1	1	5 Machine Cycles	$12t_{CLK}$
1	0	0	6 Machine Cycles	$16t_{CLK}$
1	0	1	7 Machine Cycles	$20t_{CLK}$
1	1	0	8 Machine Cycles	$24t_{CLK}$
1	1	1	9 Machine Cycles	$28t_{CLK}$

EXPLANATION OF THE AC SYMBOLS

Each Timing Symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designators are:

A—Address
C—Clock
D—Input Data
H—Logic Level HIGH
I—Instruction (program memory contents)
L—Logic Level LOW, or ALE
P—$\overline{\text{PSEN}}$
Q—Output Data
R—$\overline{\text{RD}}$ Signal
t—Time
V—Valid
W—$\overline{\text{WR}}$ Signal
X—No Longer a Valid Logic Level
Z—Float

Examples: (1) t_{AVLL} = Time for address valid to ALE LOW. (2) t_{LLPL} = Time for ALE LOW to $\overline{\text{PSEN}}$ LOW.

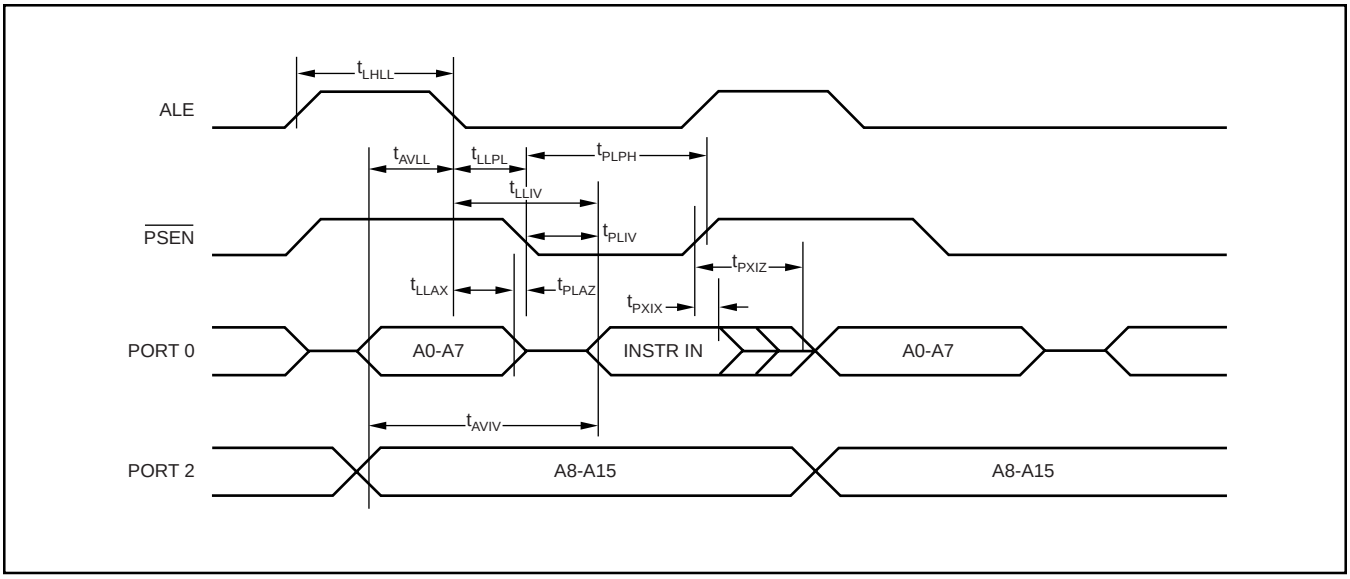


FIGURE A. External Program Memory Read Cycle.

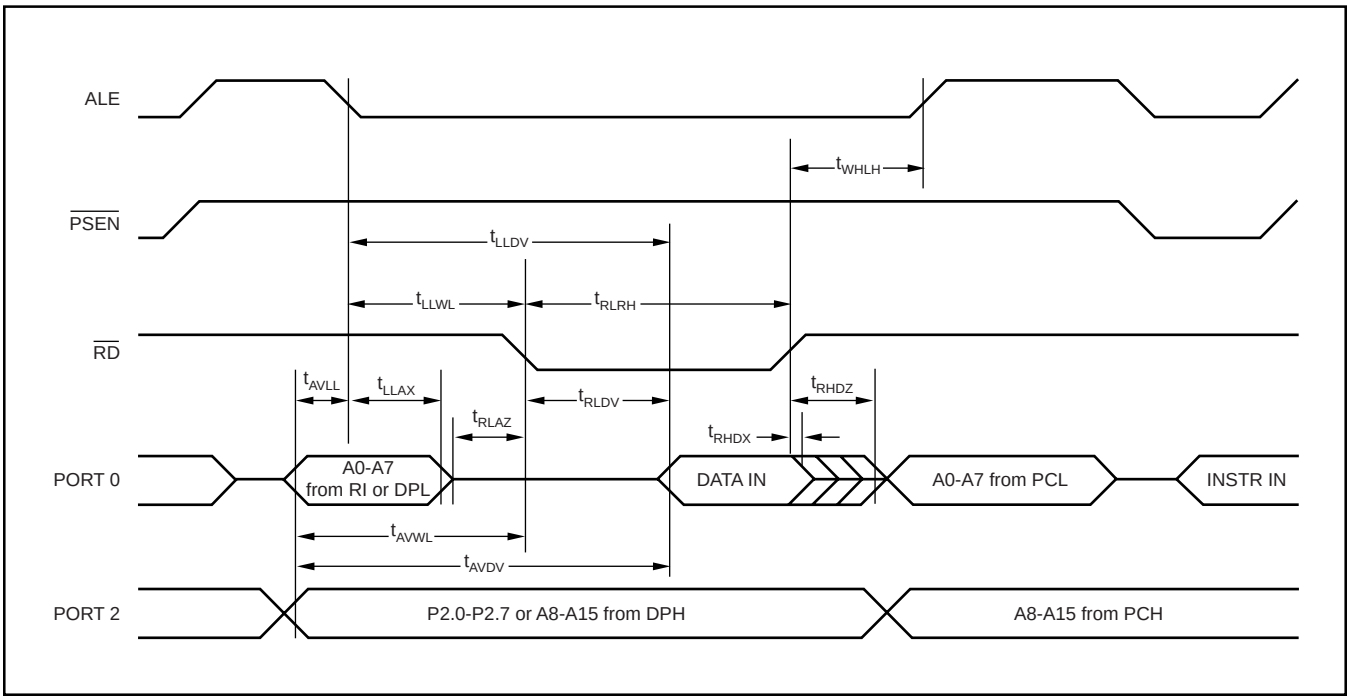


FIGURE B. External Data Memory Read Cycle.

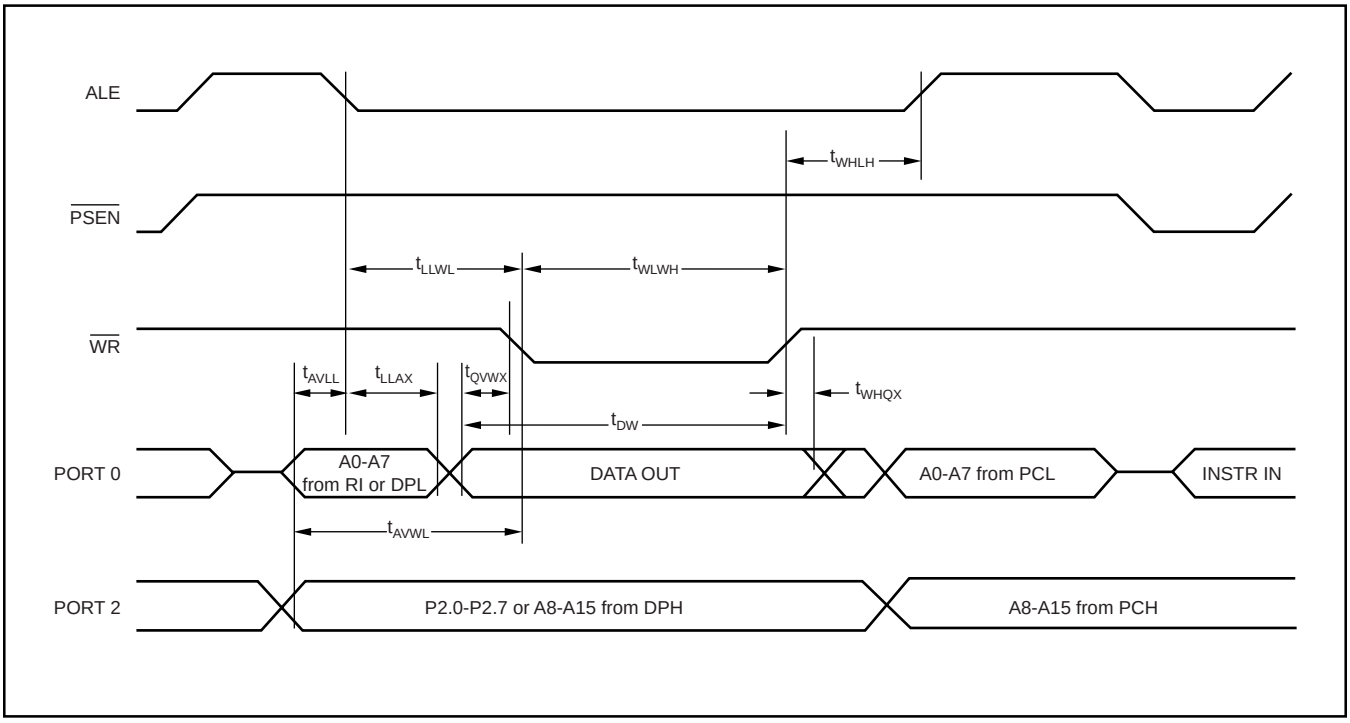


FIGURE C. External Data Memory Write Cycle.

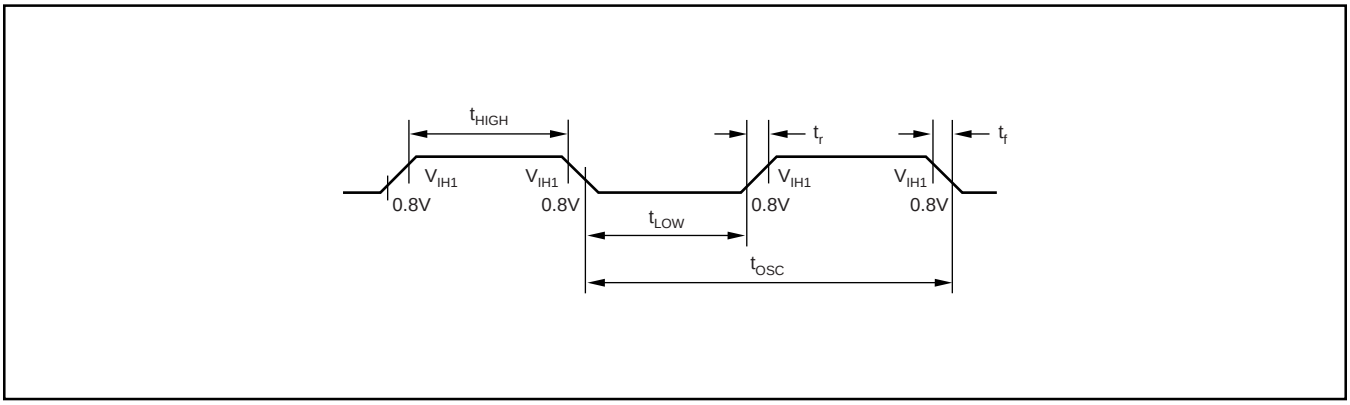


FIGURE D. External Clock Drive CLK.

RESET AND POWER-ON TIMING

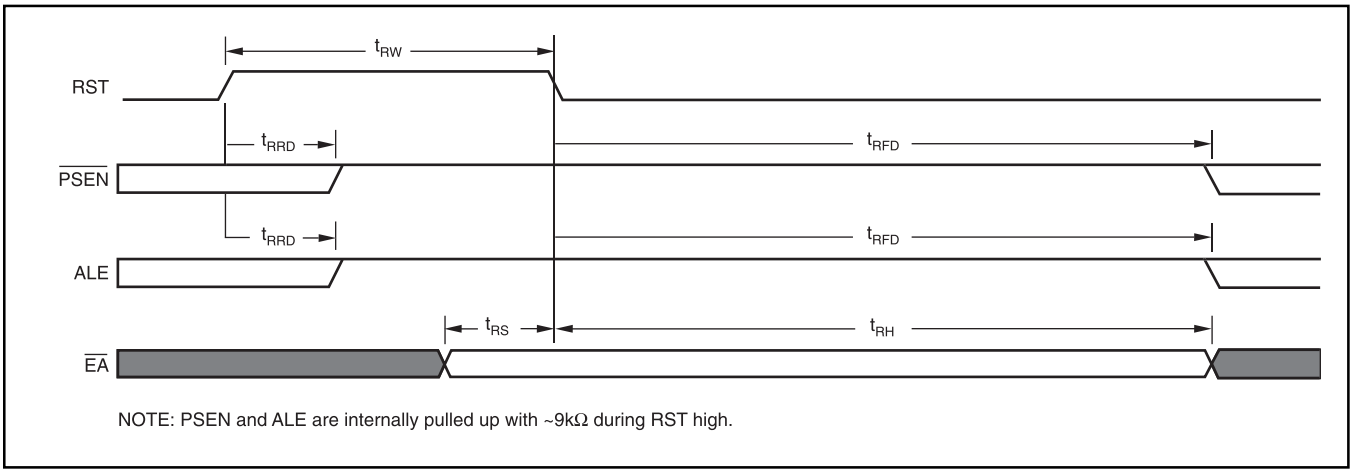


FIGURE E. Reset Timing.

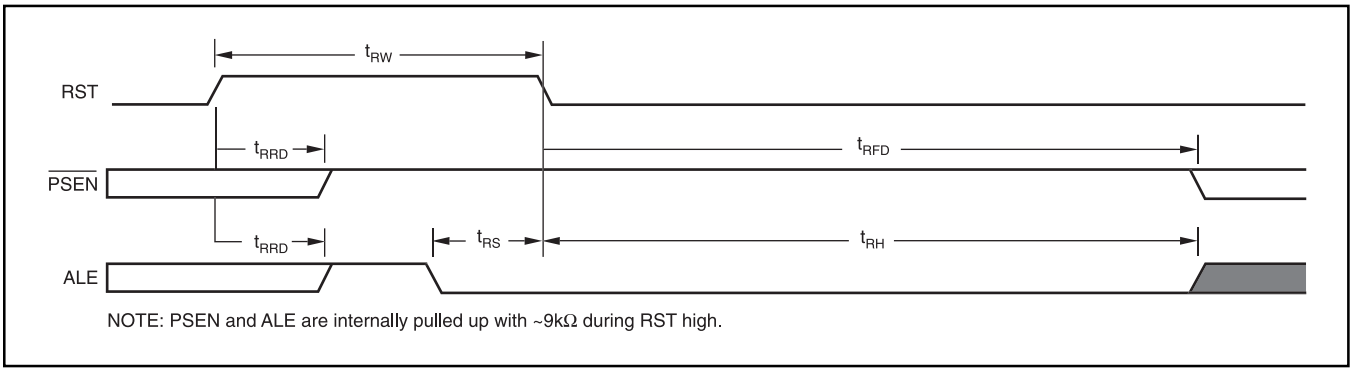


FIGURE F. Parallel Flash Programming Power-On Timing ($\overline{EA}$ is ignored).

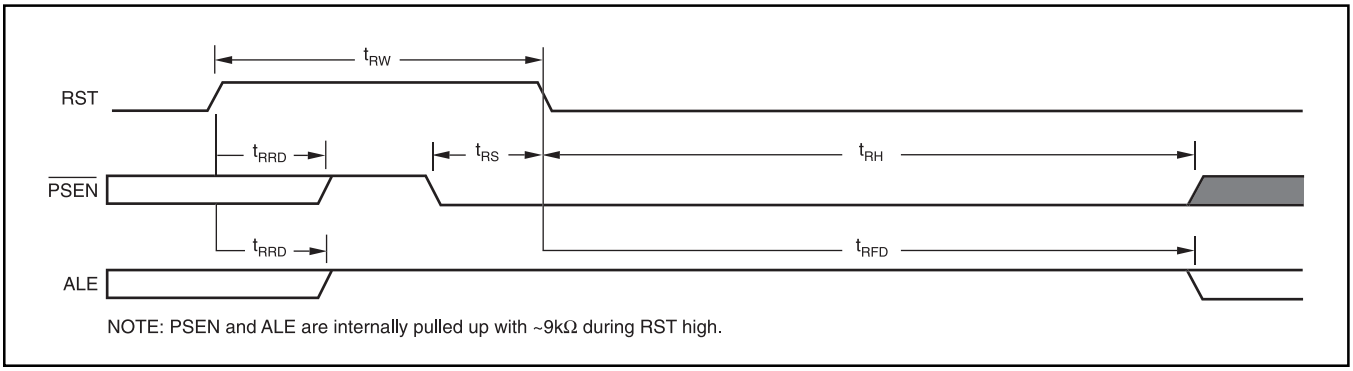
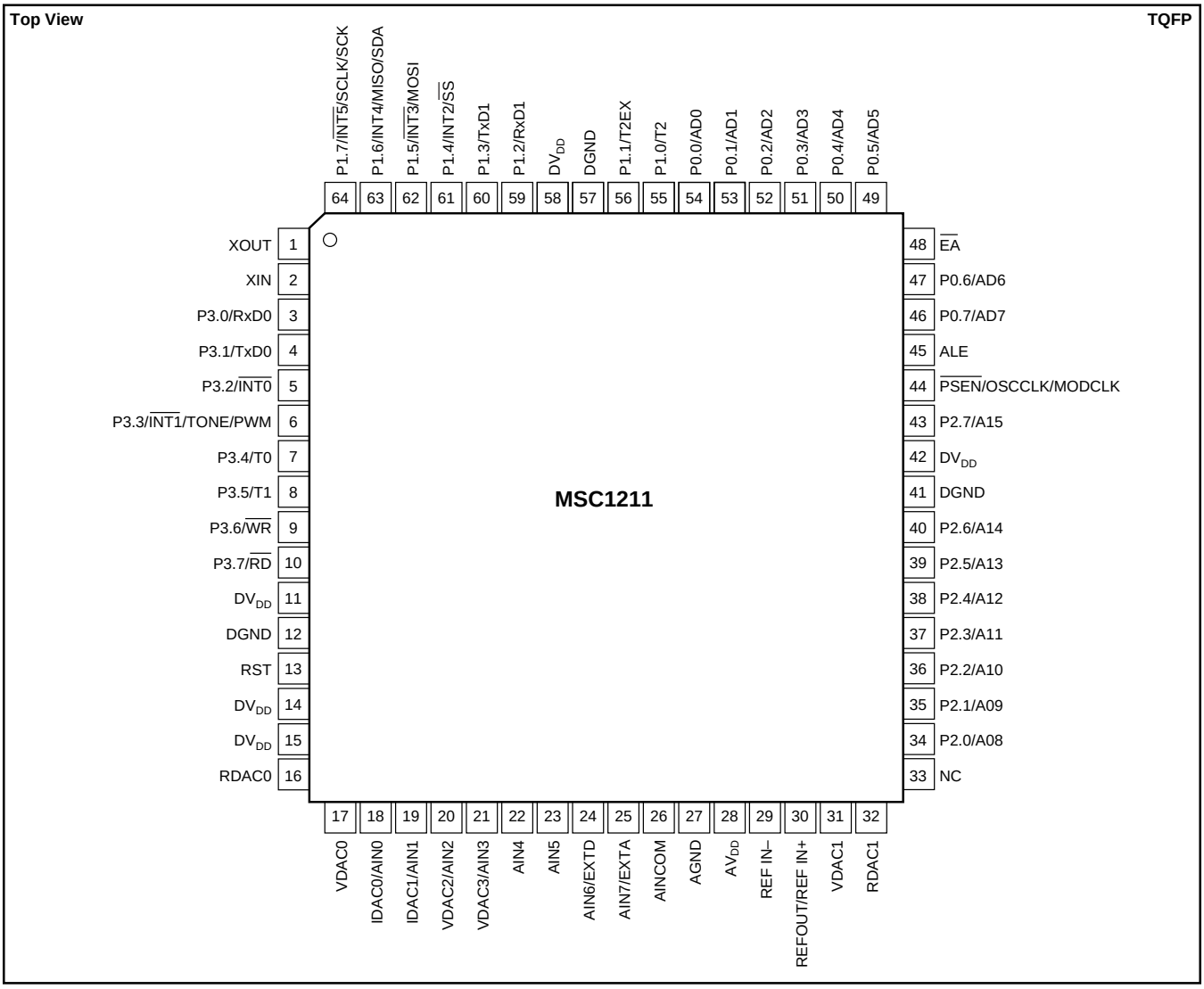


FIGURE G. Serial Flash Programming Power-On Timing ($\overline{EA}$ is ignored).

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RW}	RST width	2 t_{OSC}	—	ns
t_{RRD}	RST rise to $\overline{PSEN}$ ALE internal pull high	—	5	µs
t_{RFD}	RST falling to $\overline{PSEN}$ and ALE start	—	$(2^{17} + 512)$ t_{OSC}	ns
t_{RS}	Input signal to RST falling setup time	t_{OSC}	—	ns
t_{RH}	RST falling to input signal hold time	$(2^{17} + 512)$ t_{OSC}	—	ns

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	XOUT	The crystal oscillator pin XOUT supports parallel resonant AT cut crystals and ceramic resonators. XOUT serves as the output of the crystal amplifier.
2	XIN	The crystal oscillator pin XIN supports parallel resonant AT cut crystals and ceramic resonators. XIN can also be an input if there is an external clock source instead of a crystal.
3-10	P3.0-P3.7	Port 3 is a bidirectional I/O port. The alternate functions for Port 3 are listed below. Port 3—Alternate Functions:

PORT	ALTERNATE	MODE
P3.0	RxD0	Serial Port 0 Input
P3.1	TxD0	Serial Port 0 Output
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$/TONE/PWM	External Interrupt 1/TONE/PWM Output
P3.4	T0	Timer 0 External Input
P3.5	T1	Timer 1 External Input
P3.6	$\overline{WR}$	External Data Memory Write Strobe
P3.7	$\overline{RD}$	External Data Memory Read Strobe

11, 14, 15, 42, 58	DV_{DD}	Digital Power Supply
12, 41, 57	DGND	Digital Ground
13	RST	A HIGH on the reset input for two t_{OSC} periods will reset the device.
16	RDAC0	RDAC0 Output
17	VDAC0	VDAC0 Output
27	AGND	Analog Ground
18	IDAC0/AIN0	IDAC0 Output/Analog Input Channel 0
19	IDAC1/AIN1	IDAC1 Output/Analog Input Channel 1

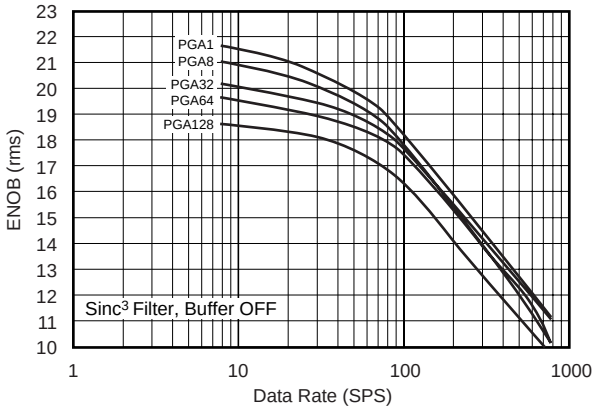
PIN DESCRIPTIONS (Cont.)

<table>
<tr><th>PIN #</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>20</td><td>VDAC2/AIN2</td><td>VDAC2 Output/Analog Input Channel 2</td></tr>
<tr><td>21</td><td>VDAC3/AIN3</td><td>VDAC3 Output/Analog Input Channel 3</td></tr>
<tr><td>22</td><td>AIN4</td><td>Analog Input Channel 4</td></tr>
<tr><td>23</td><td>AIN5</td><td>Analog Input Channel 5</td></tr>
<tr><td>24</td><td>AIN6, EXTD</td><td>Analog Input Channel 6, Low Voltage Detect Input Generates DLVD Interrupt</td></tr>
<tr><td>25</td><td>AIN7, EXTA</td><td>Analog Input Channel 7, Low Voltage Detect Input Generates ALVD Interrupt</td></tr>
<tr><td>26</td><td>AINCOM</td><td>Analog Common for Single-Ended Inputs</td></tr>
<tr><td>28</td><td>AV_{DD}</td><td>Analog Power Supply</td></tr>
<tr><td>29</td><td>REF IN–</td><td>Voltage Reference Negative Input</td></tr>
<tr><td>30</td><td>REFOUT/REF IN+</td><td>Voltage Reference Output/ Voltage Reference Positive Input</td></tr>
<tr><td>31</td><td>VDAC1</td><td>VDAC1 Output</td></tr>
<tr><td>32</td><td>RDAC1</td><td>RDAC1 Output</td></tr>
<tr><td>33</td><td>NC</td><td>No Connection</td></tr>
<tr><td>34-40, 43</td><td>P2.0-P2.7</td><td>Port 2 is a bidirectional I/O port. The alternate functions for Port 2 are listed below.
Port 2—Alternate Functions:
<table>
<tr><th>PORT</th><th>ALTERNATE</th><th>MODE</th></tr>
<tr><td>P2.0</td><td>A8</td><td>Address Bit 8</td></tr>
<tr><td>P2.1</td><td>A9</td><td>Address Bit 9</td></tr>
<tr><td>P2.2</td><td>A10</td><td>Address Bit 10</td></tr>
<tr><td>P2.3</td><td>A11</td><td>Address Bit 11</td></tr>
<tr><td>P2.4</td><td>A12</td><td>Address Bit 12</td></tr>
<tr><td>P2.5</td><td>A13</td><td>Address Bit 13</td></tr>
<tr><td>P2.6</td><td>A14</td><td>Address Bit 14</td></tr>
<tr><td>P2.7</td><td>A15</td><td>Address Bit 15</td></tr>
</table></td></tr>
<tr><td>44</td><td>$\overline{PSEN}$
OSCCLK
MODCLK</td><td>Program Store Enable: Connected to optional external memory as a chip enable. $\overline{PSEN}$ will provide an active low pulse. In programming mode, $\overline{PSEN}$ is used as an input along with ALE to define serial or parallel programming mode. $\overline{PSEN}$ is held HIGH for parallel programming and tied LOW for serial programming. This pin can also be selected (when not using external memory) to output the Oscillator clock, Modulator clock, HIGH, or LOW for light loads.
<table>
<tr><th>ALE</th><th>$\overline{PSEN}$</th><th>PROGRAM MODE SELECTION DURING RESET</th></tr>
<tr><td>NC</td><td>NC</td><td>Normal Operation (user application mode)</td></tr>
<tr><td>0</td><td>NC</td><td>Parallel Programming</td></tr>
<tr><td>NC</td><td>0</td><td>Serial Programming</td></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>45</td><td>ALE</td><td>Address Latch Enable: Used for latching the low byte of the address during an access to external memory. ALE is emitted at a constant rate of 1/2 the oscillator frequency, and can be used for external timing or clocking. One ALE pulse is skipped during each access to external data memory. In programming mode, ALE is used as an input along with $\overline{PSEN}$ to define serial or parallel programming mode. ALE is held HIGH for serial programming and tied LOW for parallel programming. This pin can also be selected (when not using external memory) to output HIGH or LOW for light loads.</td></tr>
<tr><td>48</td><td>$\overline{EA}$</td><td>External Access Enable: $\overline{EA}$ must be externally held LOW to enable the device to fetch code from external program memory locations starting with 0000_H.</td></tr>
<tr><td>46, 47, 49-54</td><td>P0.0-P0.7</td><td>Port 0 is a bidirectional I/O port. The alternate functions for Port 0 are listed below.
Port 0—Alternate Functions:
<table>
<tr><th>PORT</th><th>ALTERNATE</th><th>MODE</th></tr>
<tr><td>P0.0</td><td>AD0</td><td>Address/Data Bit 0</td></tr>
<tr><td>P0.1</td><td>AD1</td><td>Address/Data Bit 1</td></tr>
<tr><td>P0.2</td><td>AD2</td><td>Address/Data Bit 2</td></tr>
<tr><td>P0.3</td><td>AD3</td><td>Address/Data Bit 3</td></tr>
<tr><td>P0.4</td><td>AD4</td><td>Address/Data Bit 4</td></tr>
<tr><td>P0.5</td><td>AD5</td><td>Address/Data Bit 5</td></tr>
<tr><td>P0.6</td><td>AD6</td><td>Address/Data Bit 6</td></tr>
<tr><td>P0.7</td><td>AD7</td><td>Address/Data Bit 7</td></tr>
</table></td></tr>
<tr><td>55, 56, 59-64</td><td>P1.0-P1.7</td><td>Port 1 is a bidirectional I/O port. The alternate functions for Port 1 are listed below.
Port 1—Alternate Functions:
<table>
<tr><th>PORT</th><th>ALTERNATE</th><th>MODE</th></tr>
<tr><td>P1.0</td><td>T2</td><td>T2 Input</td></tr>
<tr><td>P1.1</td><td>T2EX</td><td>T2 External Input</td></tr>
<tr><td>P1.2</td><td>RxD1</td><td>Serial Port Input</td></tr>
<tr><td>P1.3</td><td>TxD1</td><td>Serial Port Output</td></tr>
<tr><td>P1.4</td><td>$\overline{INT2}/\overline{SS}$</td><td>External Interrupt/Slave Select</td></tr>
<tr><td>P1.5</td><td>$\overline{INT3}$/MOSI</td><td>External Interrupt/Master Out-Slave In</td></tr>
<tr><td>P1.6</td><td>$\overline{INT4}$/MISO</td><td>External Interrupt/Master In-Slave Out/SDA</td></tr>
<tr><td>P1.7</td><td>$\overline{INT5}$/SCK</td><td>External Interrupt/Serial Clock/SCK</td></tr>
</table></td></tr>
</table>

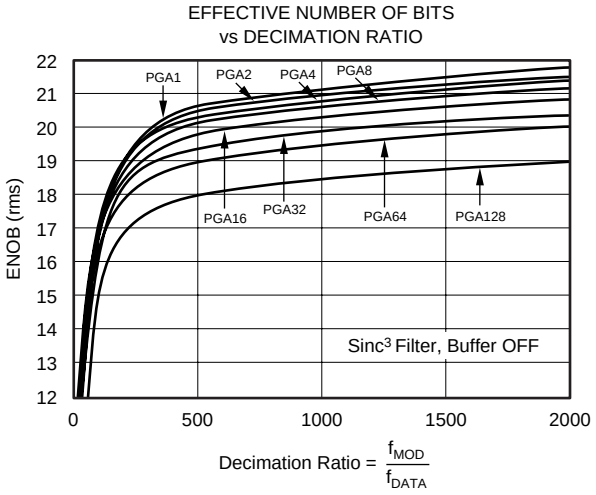
TYPICAL CHARACTERISTICS

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer On, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

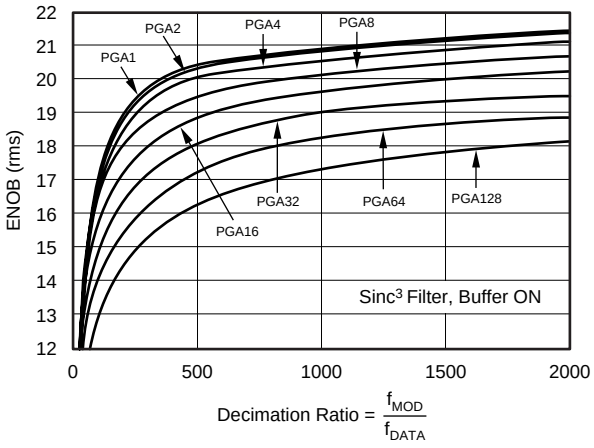
EFFECTIVE NUMBER OF BITS vs DATA RATE



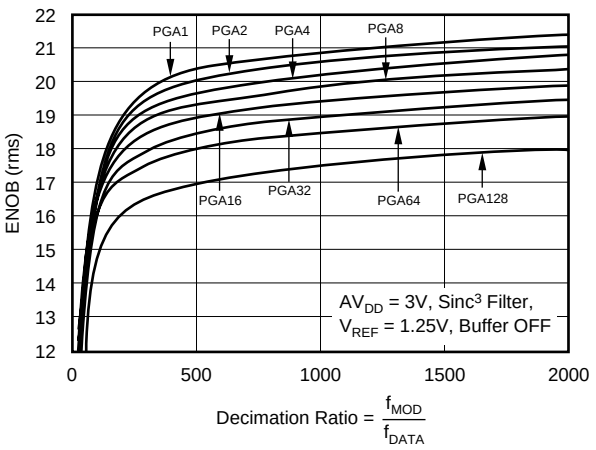
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



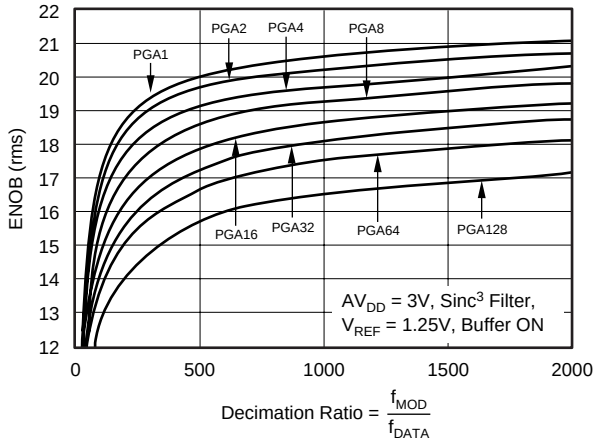
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



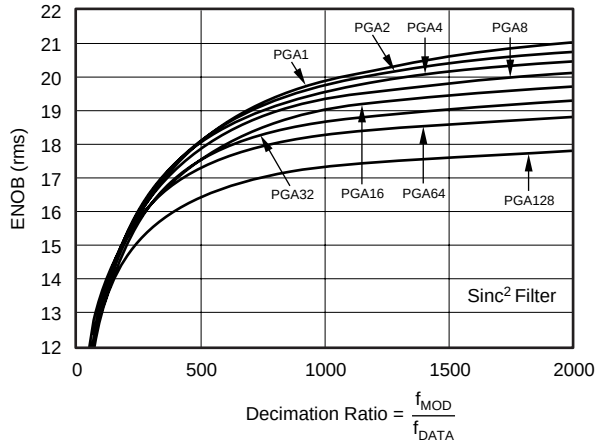
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



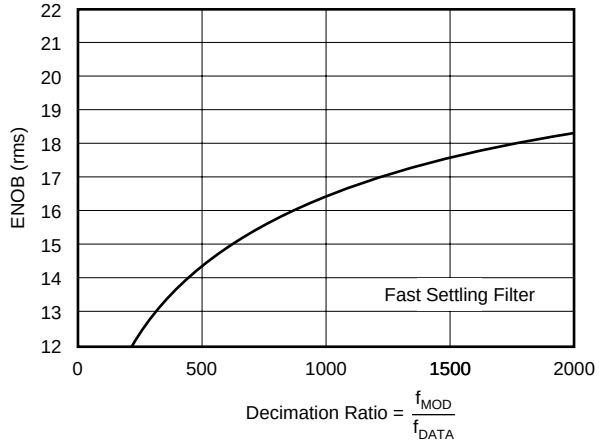
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



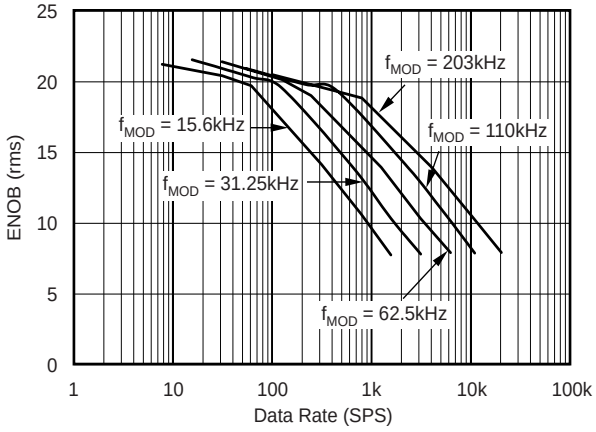
TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer On, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified. For V_{DAC}, $V_{REF} = AV_{DD}$, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

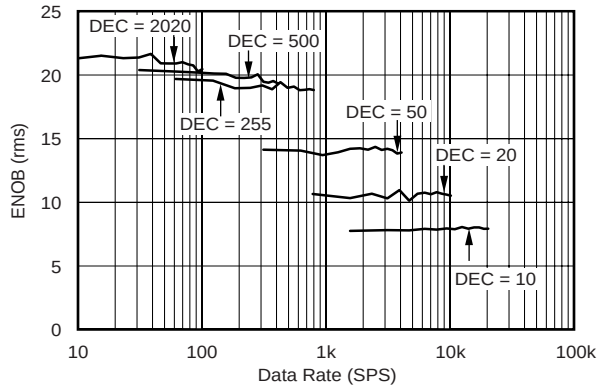
FAST SETTLING FILTER
EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



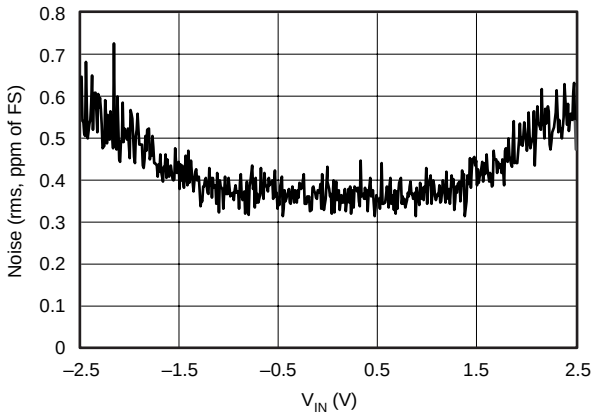
EFFECTIVE NUMBER OF BITS vs f_{MOD}
(set with ACLK)



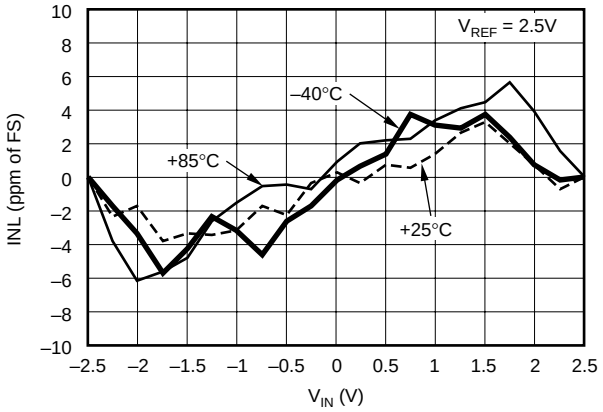
EFFECTIVE NUMBER OF BITS vs f_{MOD} (set with ACLK)
WITH FIXED DECIMATION



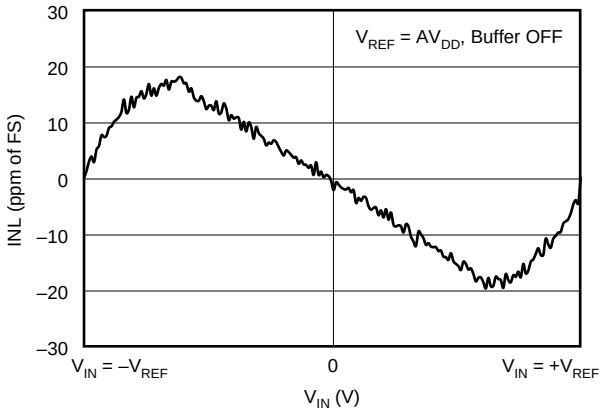
NOISE vs INPUT SIGNAL



INTEGRAL NON-LINEARITY vs INPUT SIGNAL



INTEGRAL NON-LINEARITY vs INPUT SIGNAL



TYPICAL CHARACTERISTICS (Cont.)

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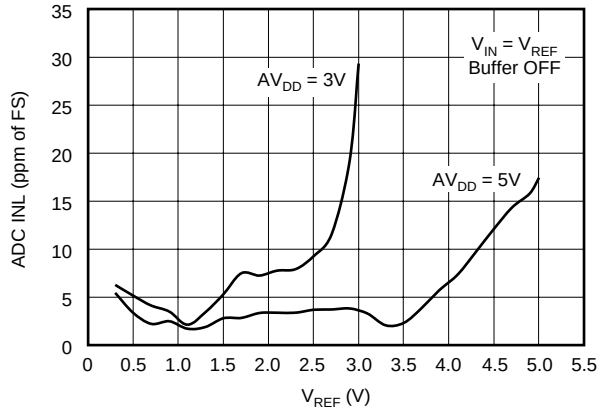
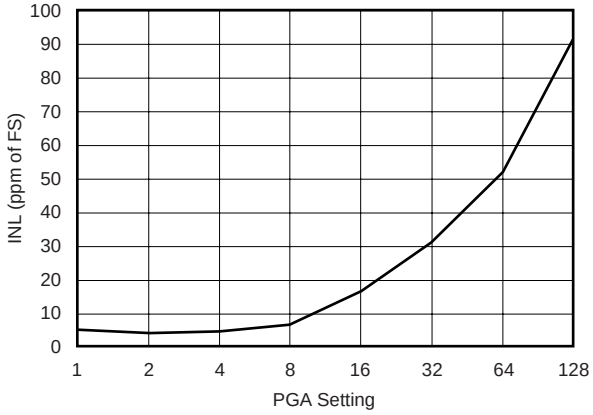
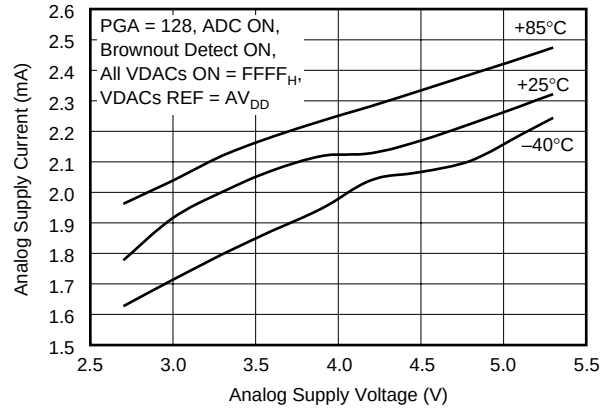
ADC INTEGRAL NONLINEARITY vs V_{REF}



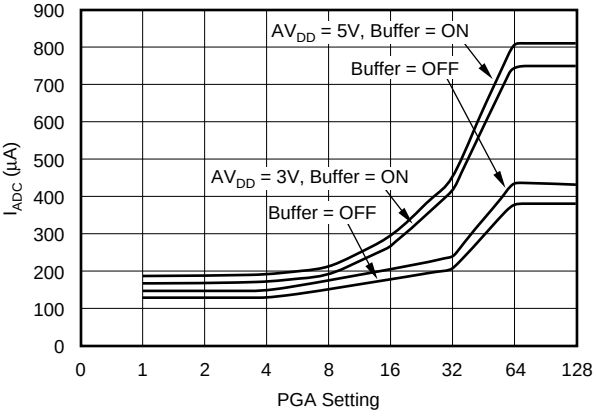
INL ERROR vs PGA



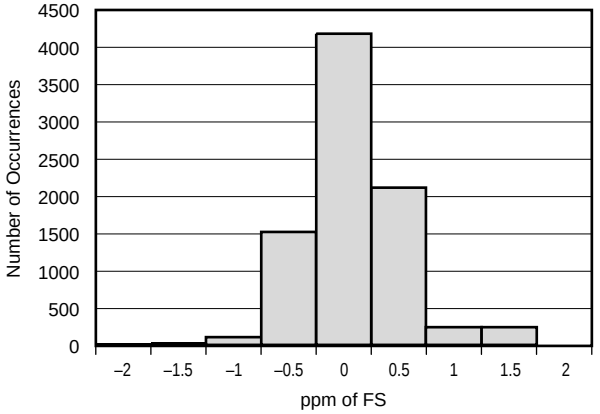
MAXIMUM ANALOG SUPPLY CURRENT



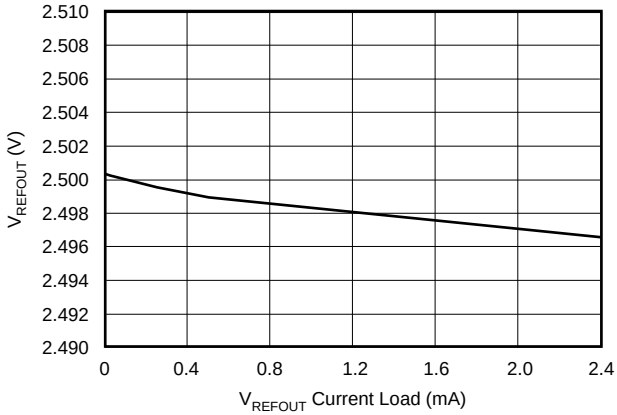
ADC CURRENT vs PGA



HISTOGRAM OF OUTPUT DATA



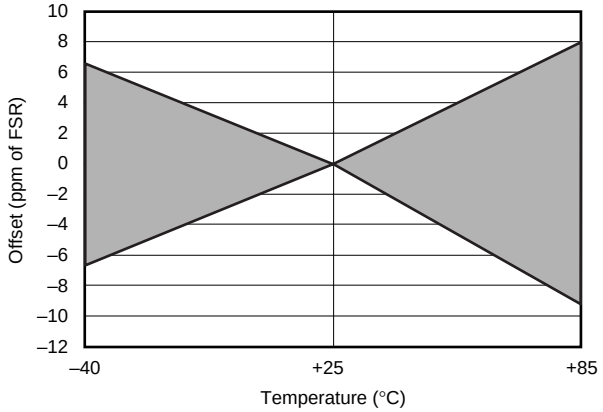
V_{REFOUT} vs LOAD CURRENT



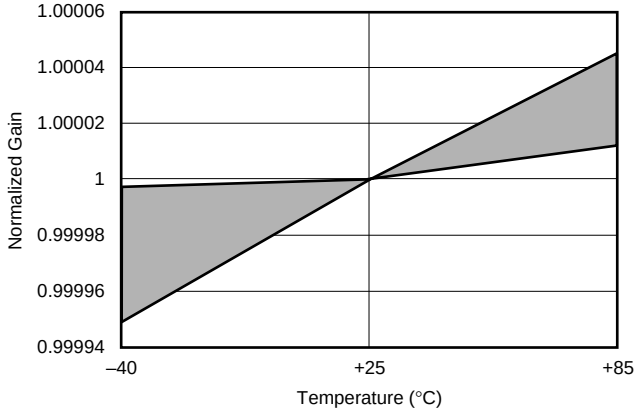
TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer On, and $V_{REF} \equiv$ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified. For V_{DAC}, $V_{REF} = AV_{DD}$, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

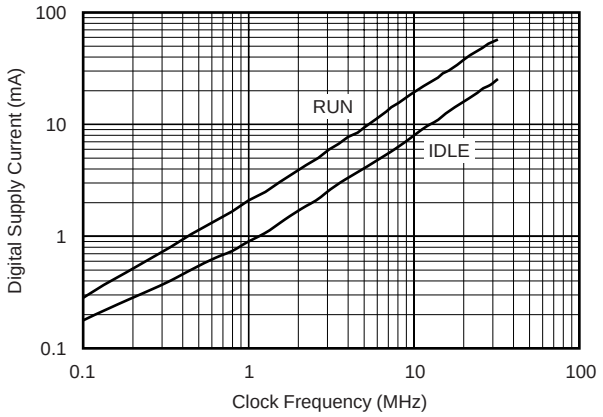
OFFSET DAC: OFFSET vs TEMPERATURE



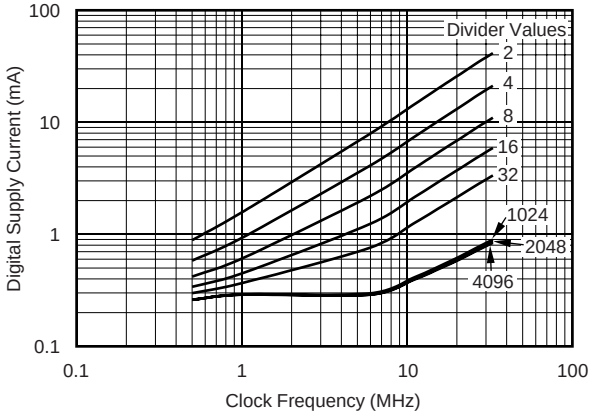
OFFSET DAC: GAIN vs TEMPERATURE



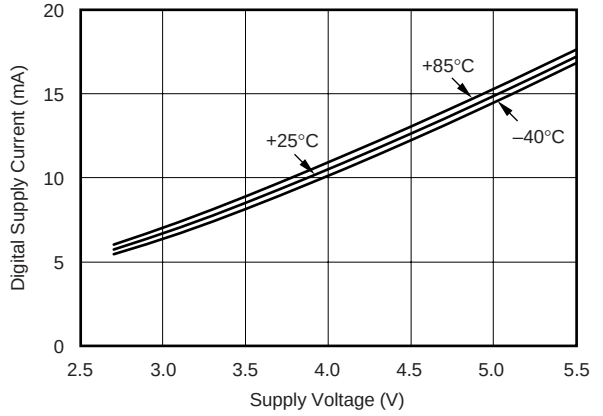
DIGITAL SUPPLY CURRENT vs FREQUENCY



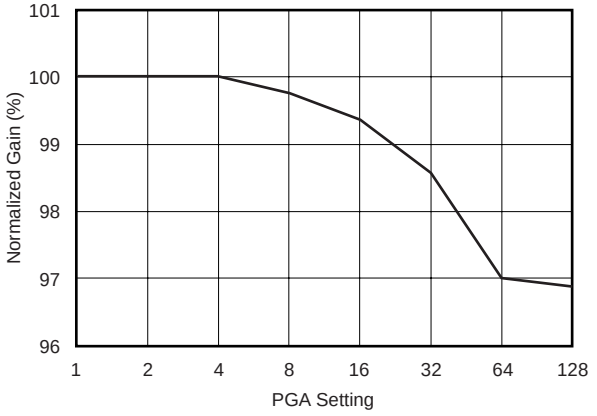
DIGITAL SUPPLY CURRENT vs CLOCK DIVIDER



DIGITAL SUPPLY CURRENT vs SUPPLY VOLTAGE



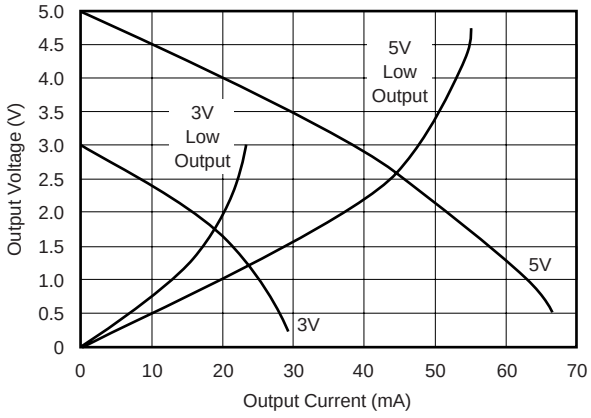
NORMALIZED GAIN vs PGA



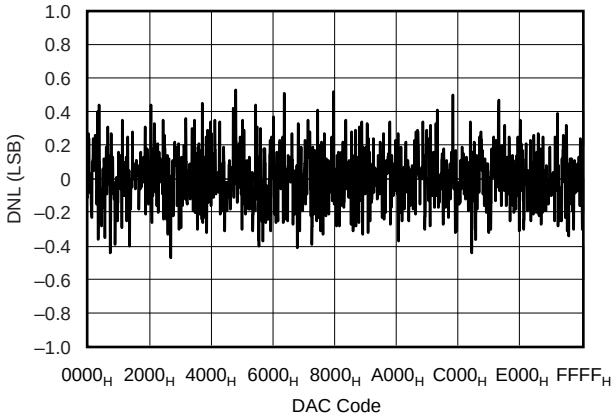
TYPICAL CHARACTERISTICS (Cont.)

AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer On, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified. For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

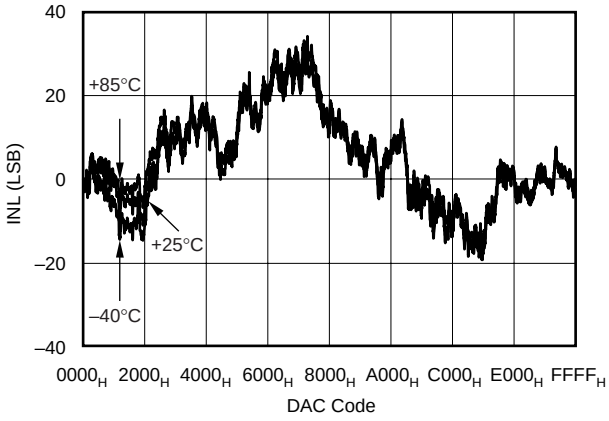
CMOS DIGITAL OUTPUT



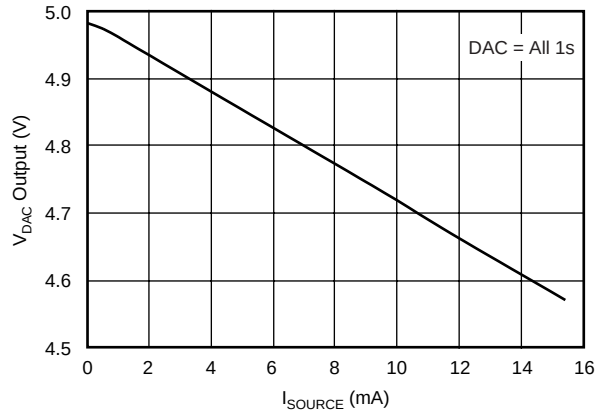
VDAC DIFFERENTIAL NONLINEARITY vs CODE



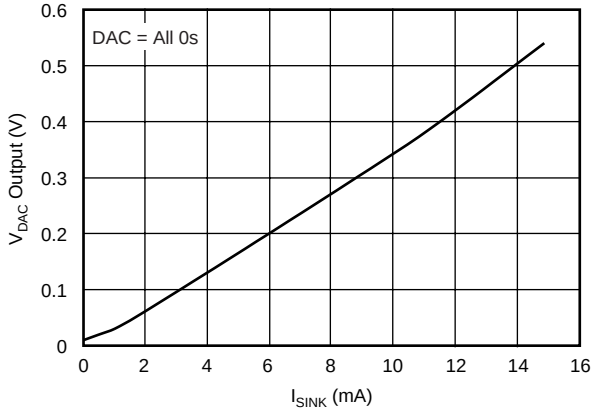
VDAC INTEGRAL NONLINEARITY vs CODE



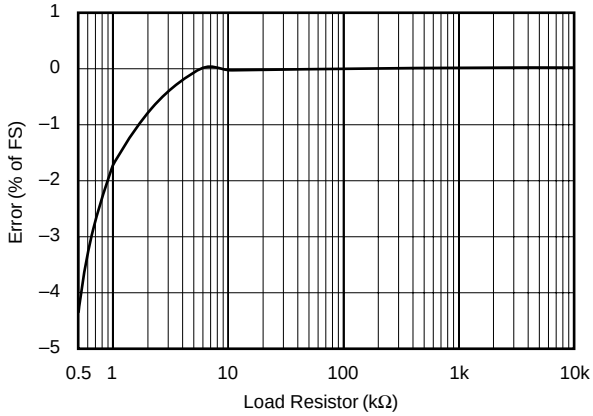
VDAC SOURCE CURRENT CAPABILITY



VDAC SINK CURRENT CAPABILITY



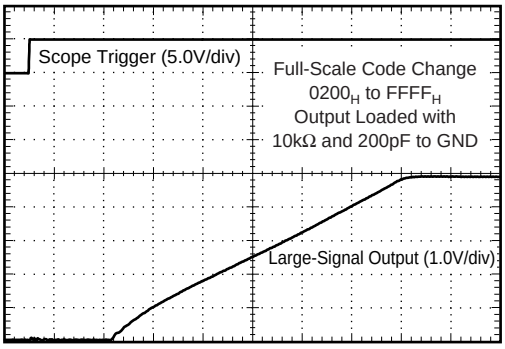
VDAC FULL-SCALE ERROR vs LOAD RESISTOR



TYPICAL CHARACTERISTICS (Cont.)

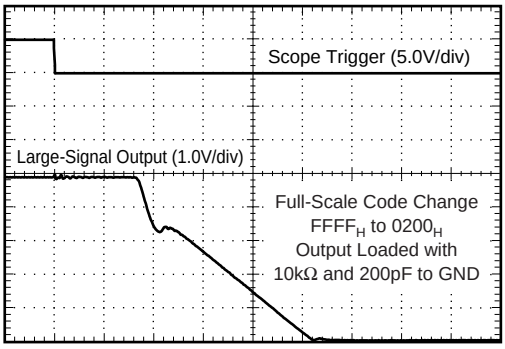
AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 8MHz, PGA = 1, f_{MOD} = 15.625kHz, Bipolar, Buffer On, and V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.
For V_{DAC}, V_{REF} = AV_{DD}, R_{LOAD} = 10kΩ, and C_{LOAD} = 200pF, unless otherwise noted.

FULL-SCALE SETTLING TIME



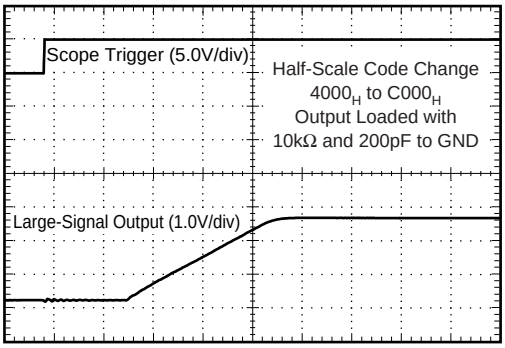
Time (1µs/div)

FULL-SCALE SETTLING TIME



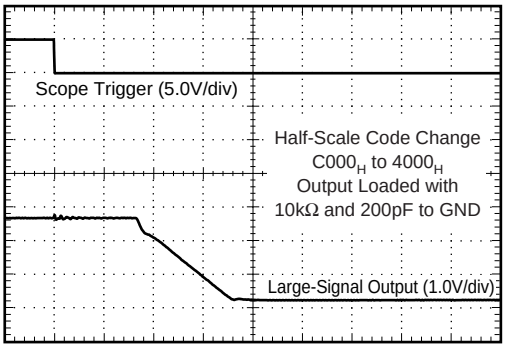
Time (1µs/div)

HALF-SCALE SETTLING TIME



Time (1µs/div)

HALF-SCALE SETTLING TIME



Time (1µs/div)

DESCRIPTION

The MSC1211Yx is a completely integrated family of mixed-signal devices incorporating a high-resolution delta-sigma ADC, quad 16-bit DACs, 8-channel multiplexer, burnout detect current sources, selectable buffered input, offset DAC (Digital-to-Analog Converter), Programmable Gain Amplifier (PGA), temperature sensor, voltage reference, 8-bit microcontroller, Flash Program Memory, Flash Data Memory, and Data SRAM, as shown in Figure 1.

On-chip peripherals include an additional 32-bit accumulator, an SPI compatible serial port with FIFO, I^2C, dual UARTs, multiple digital input/output ports, watchdog timer, low-voltage detect, on-chip power-on reset, 16-bit PWM, breakpoints, brownout reset, three timer/counters, and a system clock divider.

The device accepts low-level differential or single-ended signals directly from a transducer. The ADC provides 24 bits of resolution and 24 bits of no-missing-code performance using a $sinc^3$ filter with a programmable sample rate. The ADC also has a selectable filter that allows for high-resolution single-cycle conversion.

The microcontroller core is 8051 instruction set compatible. The microcontroller core is an optimized 8051 core which executes up to three times faster than the standard 8051 core, given the same clock source. That makes it possible to run the device at a lower external clock frequency and achieve the same performance at lower power than the standard 8051 core.

The MSC1211Yx allows the user to uniquely configure the Flash and SRAM memory maps to meet the needs of their application. The Flash is programmable down to 2.7V using both serial and parallel programming methods. The Flash endurance is 100k Erase/Write cycles. In addition, 1280 bytes of RAM are incorporated on-chip.

The part has separate analog and digital supplies, which can be independently powered from 2.7V to +5.5V. At +3V operation, the power dissipation for the part is typically less than 4mW. The MSC1211Yx is packaged in a TQFP-64 package.

The MSC1211Yx is designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation.

ENHANCED 8051 CORE

All instructions in the MSC1211 family perform exactly the same functions as they would in a standard 8051. The effect on bits, flags, and registers is the same. However, the timing is different. The MSC1211 family utilizes an efficient 8051 core which results in an improved instruction execution speed of between 1.5 and 3 times faster than the original core for the same external clock speed (4 clock cycles per instruction versus 12 clock cycles per instruction, as shown in Figure 2). This translates into an effective throughput improvement of more than 2.5 times, using the same code and same external clock speed. Therefore, a device frequency of 30MHz for the MSC1211Yx actually performs at an

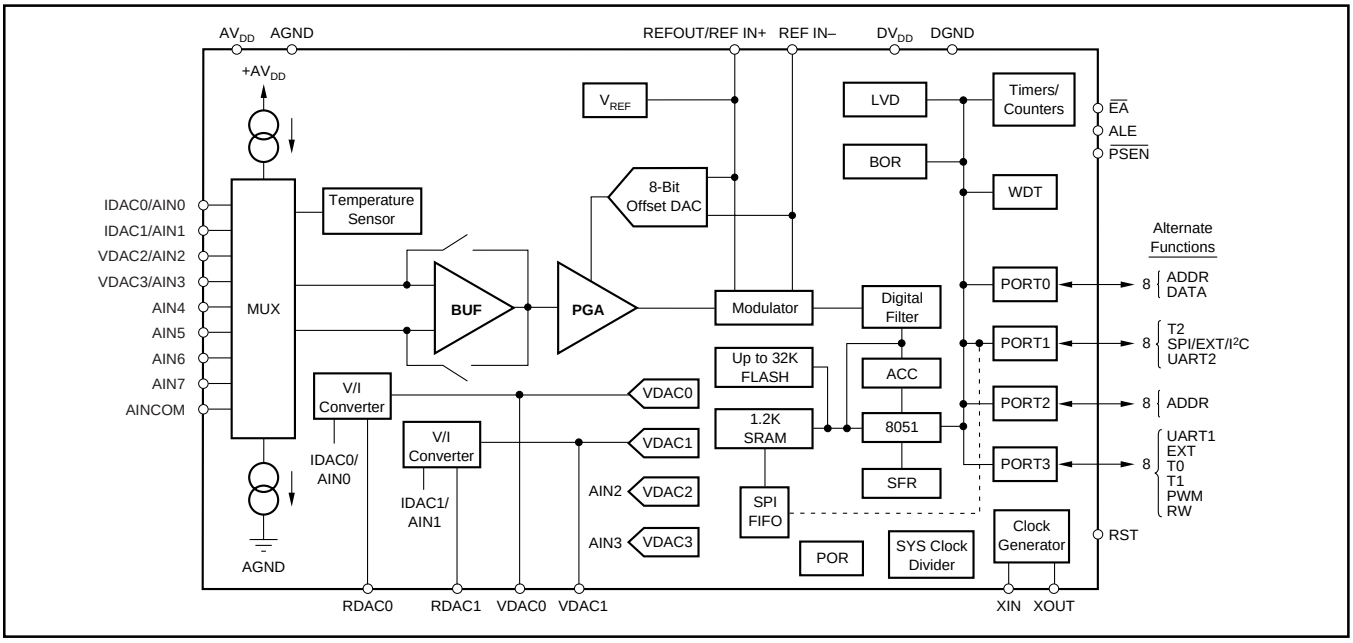


FIGURE 1. Block Diagram.

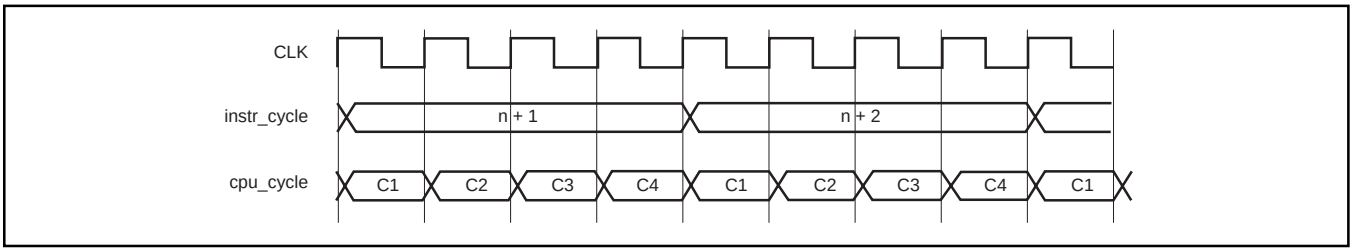


FIGURE 2. Instruction Cycle Timing.

equivalent execution speed of 75MHz compared to the standard 8051 core. This allows the user to run the device at slower external clock speeds which reduces system noise and power consumption, but provides greater throughput. This performance difference can be seen in Figure 3. The timing of software loops will be faster with the MSC1211. However, the timer/counter operation of the MSC1211 may be maintained at 12 clocks per increment or optionally run at 4 clocks per increment.

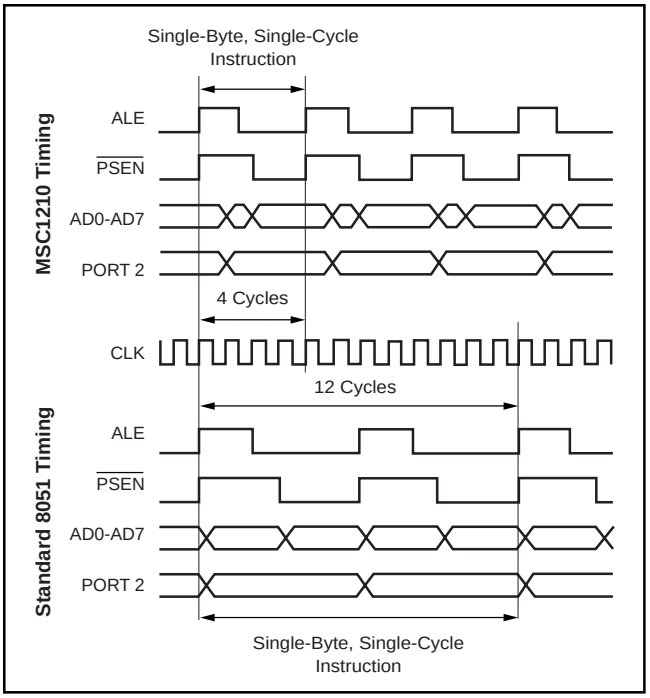


FIGURE 3. Comparison of MSC1211 Timing to Standard 8051 Timing.

The MSC1211 also provides dual data pointers (DPTRs) to speed block Data Memory moves.

Additionally, it can stretch the number of memory cycles to access external Data Memory from between two and nine instruction cycles in order to accommodate different speeds of memory or devices, as shown in Table I. The MSC1211 provides an external memory interface with a 16-bit address bus (P0 and P2). The 16-bit address bus makes it necessary to multiplex the low address byte through the P0 port. To enhance P0 and P2 for high-speed memory access, hardware configuration control is provided to configure the ports for external memory/peripheral interface or general-purpose I/O.

CKCON ($8E_H$) MD2:MD0	INSTRUCTION CYCLES (for MOVX)	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (SYS CLKs)	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (µs) AT 12MHz
000	2	2	0.167
001	3 (default)	4	0.333
010	4	8	0.667
011	5	12	1.000
100	6	16	1.333
101	7	20	1.667
110	8	24	2.000
111	9	28	2.333

TABLE I. Memory Cycle Stretching. Stretching of MOVX timing as defined by MD2, MD1, and MD0 bits in CKCON register (address $8E_H$).

Furthermore, improvements were made to peripheral features that offload processing from the core, and the user, to further improve efficiency. For instance, the SPI interface uses a FIFO, which allows the SPI interface to transmit and receive data with minimum overhead needed from the core. Also, a 32-bit accumulator was added to significantly reduce the processing overhead for the multiple byte data from the ADC or other sources. This allows for 24-bit addition and shifting to be accomplished in a few instruction cycles, compared to hundreds of instruction cycles through software implementation.

Family Device Compatibility

The hardware functionality and pin configuration across the MSC1211 family is fully compatible. To the user the only difference between family members is the memory configuration. This makes migration between family members simple. Code written for the MSC1211Y2 can be executed directly on an MSC1211Y3, MSC1211Y4, or MSC1211Y5. This gives the user the ability to add or subtract software functions and to freely migrate between family members. Thus, the MSC1211 can become a standard device used across several application platforms.

Family Development Tools

The MSC1211 is fully compatible with the standard 8051 instruction set. This means that the user can develop software for the MSC1211 with their existing 8051 development tools. Additionally, a complete, integrated development environment is provided with each demo board, and third-party developers also provide support.

Power Down Modes

The MSC1211 can power several of the peripherals and put the CPU into IDLE. This is accomplished by shutting off the clocks to those sections, as shown in Figure 4.

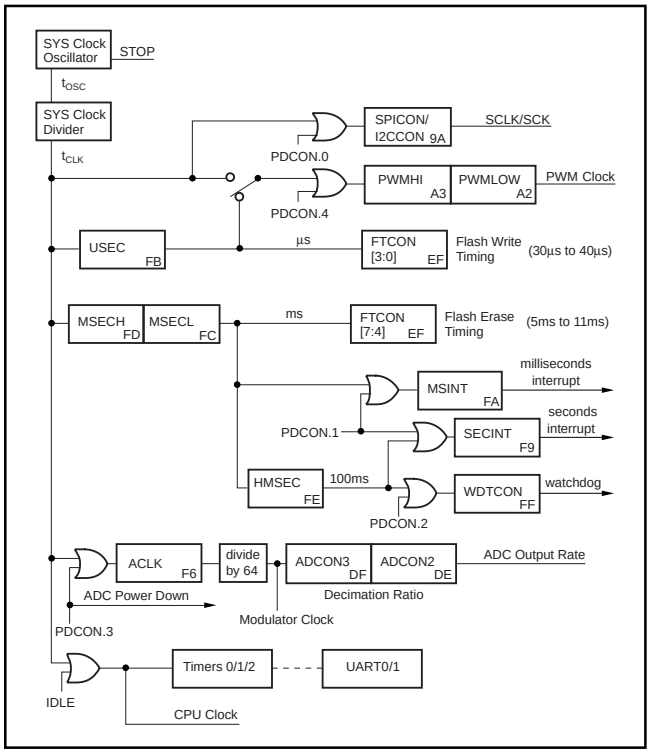


FIGURE 4. MSC1211 Timing Chain and Clock Control.

OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected as the input channel, as shown in Figure 5. If AIN0 is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. With this method, it is possible to have up to eight fully differential input channels. It is also possible to switch the polarity of the differential input pair to negate any offset voltages.

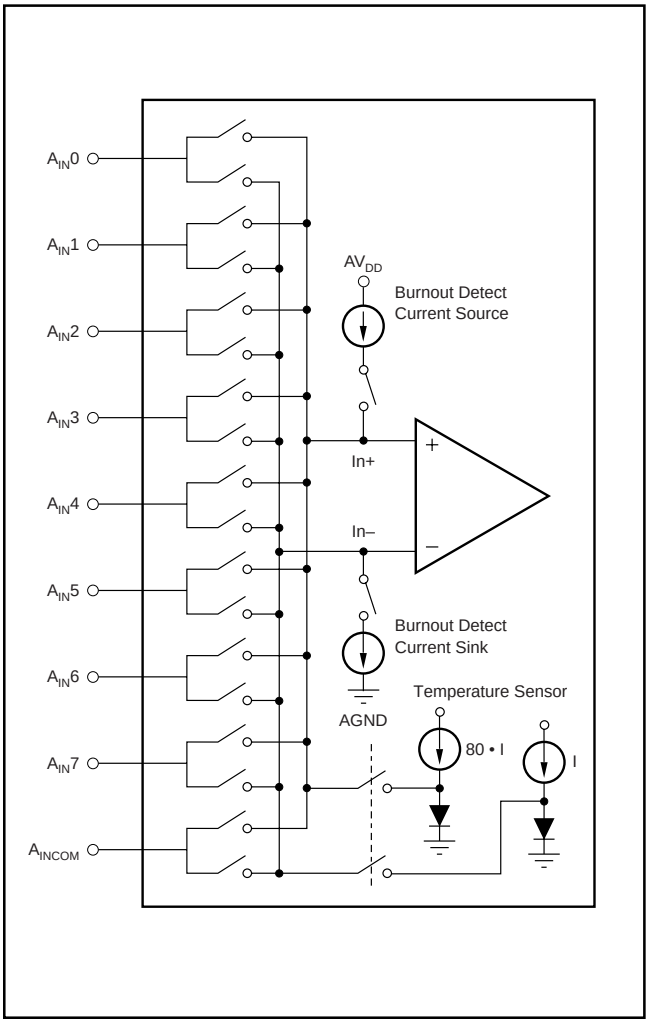


FIGURE 5. Input Multiplexer Configuration.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the pins.

TEMPERATURE SENSOR

On-chip diodes provide temperature sensing capability. When the configuration register for the input MUX is set to all 1s, the diodes are connected to the input of the ADC. All other channels are open.

BURNOUT DETECT

When the Burnout Detect (BOD) bit is set in the ADC control configuration register (ADCON0 DC_H), two current sources are enabled. The current source on the positive input channel sources approximately 2µA of current. The current source on the negative input channel sinks approximately 2µA. This allows for the detection of an open circuit (full-scale reading) or short circuit (small differential reading) on the selected input differential pair.

INPUT BUFFER

The analog input impedance is always high, regardless of PGA setting (when the buffer is enabled). With the buffer enabled, the input voltage range is reduced and the analog power-supply current is higher. If the limitation of input voltage range is acceptable, then the buffer is always preferred.

The input impedance of the MSC1211 without the buffer is 5MΩ/PGA. The buffer is controlled by the state of the BUF bit in the ADC control register (ADCON0 DC_H).

ANALOG INPUT

When the buffer is not selected, the input impedance of the analog input changes with ACLK clock frequency (ACLK $F6_H$) and gain (PGA). The relationship is:

$$A_{IN}\ \text{Impedance}\ (\Omega) = \left(\frac{1\text{MHz}}{\text{ACLK Frequency}}\right) \bullet \left(\frac{5\text{M}\Omega}{\text{PGA}}\right)$$

where ACLK frequency = f_{CLK}/(ACLK +1).

Figure 6 shows the basic input structure of the MSC1211. The sampling frequency varies according to the PGA settings, as shown in Table II.

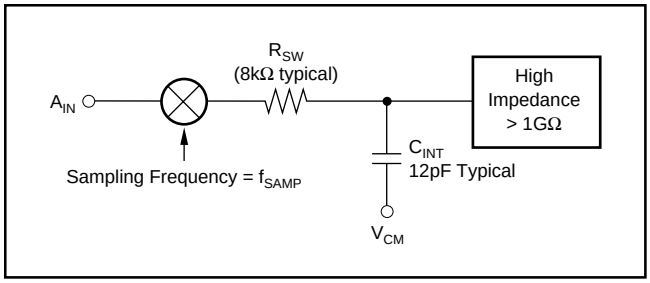


FIGURE 6. Analog Input Structure.

PGA	FULL-SCALE RANGE	SAMPLING FREQUENCY
1	$\pm V_{REF}$	f_{SAMP}
2	$\pm V_{REF}/2$	f_{SAMP}
4	$\pm V_{REF}/4$	f_{SAMP}
8	$\pm V_{REF}/8$	$f_{SAMP} \bullet 2$
16	$\pm V_{REF}/16$	$f_{SAMP} \bullet 4$
32	$\pm V_{REF}/32$	$f_{SAMP} \bullet 8$
64	$\pm V_{REF}/64$	$f_{SAMP} \bullet 16$
128	$\pm V_{REF}/128$	$f_{SAMP} \bullet 16$
NOTE: f_{SAMP} = ACLK frequency/64.		

TABLE II. Sampling Frequency Versus PGA Setting.

PGA

The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the ADC. For instance, with a PGA of 1 on a ±2.5V full-scale range, the ADC can resolve to 1.5µV. With a PGA of 128 on a ±19mV full-scale range, the ADC can resolve to 75nV. With a PGA of 1 on a ±2.5V full-scale range, it would require a 26-bit ADC to resolve 75nV, as shown in Table III.

PGA SETTING	FULL-SCALE RANGE (V)	ENOB AT 10Hz	RMS MEASUREMENT RESOLUTION (nV)	EQUIVALENT ENOB AT PGA = 1 (5V RANGE)
1	±2.5V	21.7	1468	21.7
2	±1.25	21.5	843	22.5
4	±0.625	21.4	452	23.4
8	±0.313	21.2	259	24.2
16	±0.156	20.8	171	24.8
32	±0.0781	20.4	113	25.4
64	±0.039	20	74.5	26
128	±0.019	19	74.5	26

TABLE III. ENOB Versus PGA.

OFFSET DAC

The analog input to the PGA can be offset by up to half the full-scale input range of the PGA by using the ODAC register (SFR $E6_H$). The ODAC (Offset DAC) register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Since the ODAC introduces an analog (instead of digital) offset to the PGA, using the ODAC does not reduce the performance of the ADC.

MODULATOR

The modulator is a single-loop 2nd-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the CLK using the value in the Analog Clock register (ACLK). The data output rate is:

$$\text{Data Rate} = f_{MOD}/\text{Decimation Ratio}$$

where $f_{MOD} = f_{CLK}/(ACLK + 1)/64$

CALIBRATION

The offset and gain errors in the MSC1211, or the complete system, can be reduced with calibration. Calibration is controlled through the ADCON1 register (SFR DD_H), bits CAL2:CAL0. Each calibration process takes seven t_{DATA} periods (data conversion time) to complete. Therefore, it takes 14 t_{DATA} periods to complete both an offset and gain calibration.

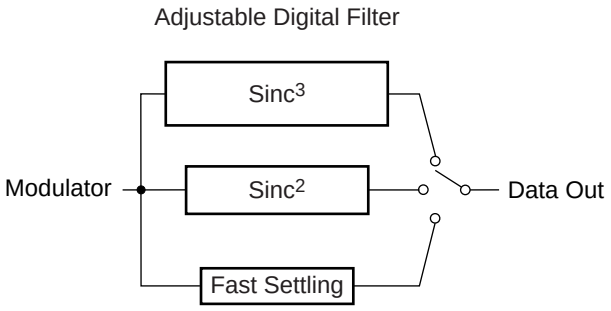
For system calibration, the appropriate signal must be applied to the inputs. The system offset command requires a “zero” differential input signal. It then computes an offset that will nullify offset in the system. The system gain command requires a positive “full-scale” differential input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take seven t_{DATA} periods to complete.

Calibration should be performed after power on, a change in temperature, decimation ratio, buffer, or a change of the PGA. Calibration will remove the effects of the Offset DAC, therefore, changes to the Offset DAC register must be done after calibration.

At the completion of calibration, the ADC Interrupt bit goes HIGH which indicates the calibration is finished and valid data is available.

DIGITAL FILTER

The Digital Filter can use either the Fast Settling, $sinc^2$, or $sinc^3$ filter, as shown in Figure 7. In addition, the Auto mode changes the sinc filter after the input channel or PGA is changed. When switching to a new channel, it will use the Fast Settling filter, for the next two conversions the first of which should be discarded. It will then use the $sinc^2$ followed by the $sinc^3$ filter to improve noise performance. This combines the low-noise advantage of the $sinc^3$ filter with the quick response of the Fast Settling Time filter. The frequency response of each filter is shown in Figure 8.



FILTER SETTLING TIME

FILTER	SETTLING TIME (Conversion Cycles)
$Sinc^3$	3(1)
$Sinc^2$	2(1)
Fast	1(1)

NOTE: (1) With Synchronized Channel Changes.

AUTO MODE FILTER SELECTION

CONVERSION CYCLE			
1	2	3	4+
Discard	Fast	$Sinc^2$	$Sinc^3$

FIGURE 7. Filter Step Responses.

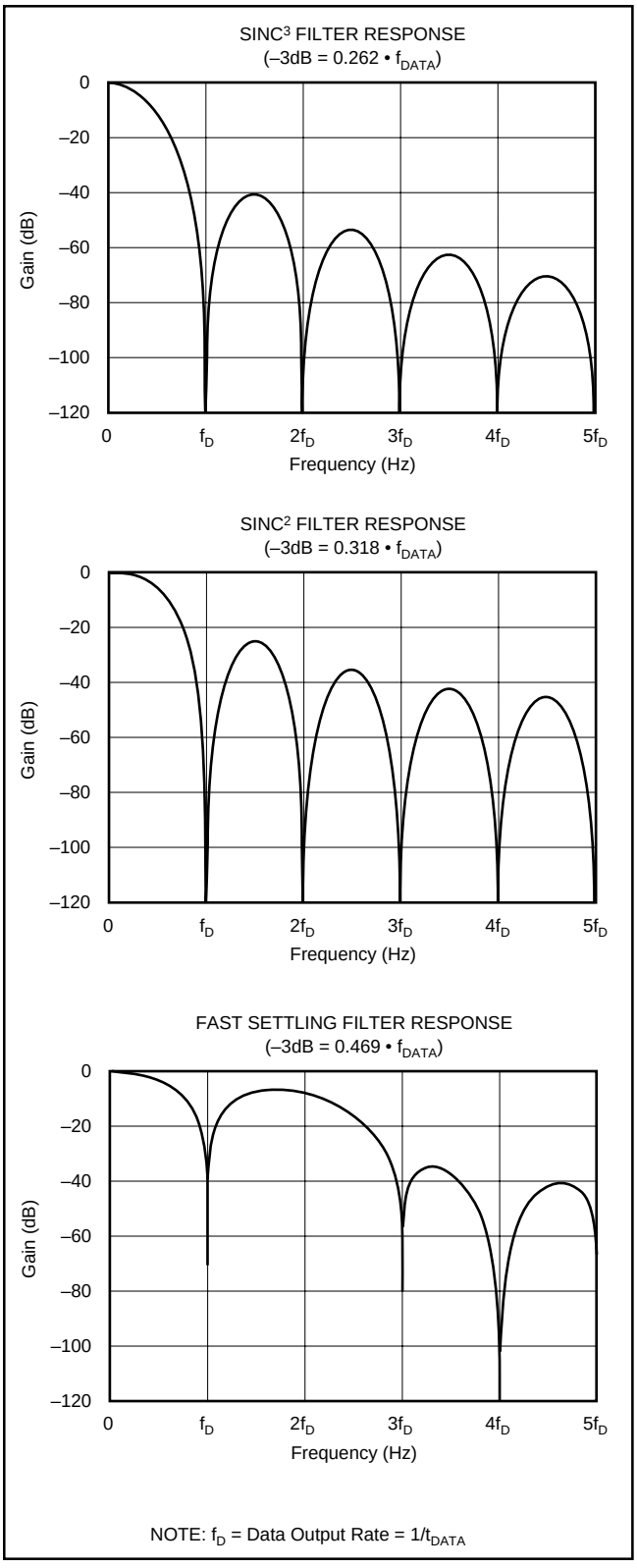


FIGURE 8. Filter Frequency Responses.

VOLTAGE REFERENCE

The voltage reference used for the MSC1211 can either be internal or external. The power-up configuration for the voltage reference is 2.5V internal. The selection for the voltage reference is made through the ADCON0 register (SFR DC_H).

The internal voltage reference is selectable as either 1.25V (AV_{DD} = 2.7V to 5.25V) or 2.5V (AV_{DD} = 4.5V to 5.25V). If the internal V_{REF} is not used, it should be turned off to reduce noise and power consumption. The V_{REFOUT} pin should have a 0.1µF capacitor to AGND.

The external voltage reference is differential and is represented by the voltage difference between the pins: REF IN+ and REF IN–. The absolute voltage on either pin (REF IN+ and REF IN–) can range from AGND to AV_{DD}, however, the differential voltage must not exceed 2.6V. The differential voltage reference provides easy means of performing ratiometric measurement.

DAC

The architecture consists of a string DAC followed by an output buffer amplifier. Figure 9 shows a block diagram of the DAC architecture.

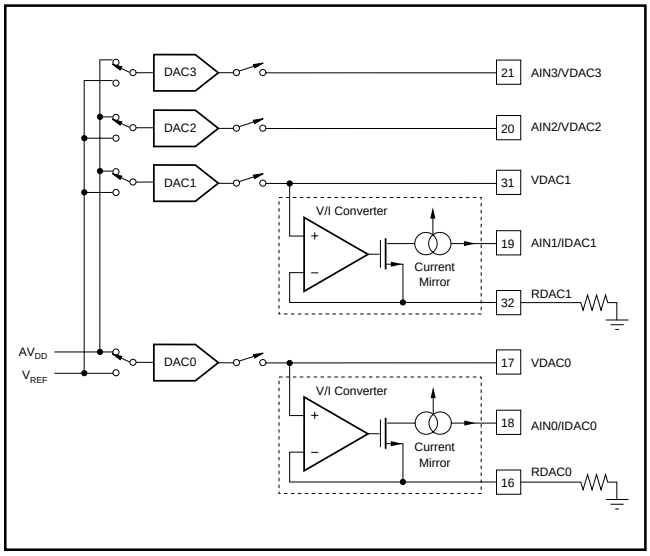


FIGURE 9. DAC Architecture.

The input coding to the DAC is straight binary, so the ideal output voltage is given by:

$$VDAC = V_{REF} \bullet \frac{D}{65536}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The DAC selects the voltage from a string of resistors from the reference to AGND. It is essentially a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is ensured monotonic because it is a string of resistors.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of AGND to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1V/µs with a full-scale settling time of 8µs with the output unloaded.

DAC REFERENCE

Each DAC can be selected to use the internal REFOUT/REF IN+ voltage or the supply voltage AV_{DD} as the reference for the DAC. The full range of the voltage DAC is limited according to Table IV. The full range of the current DAC is limited according to Table V.

DAC REFERENCE	AV_{DD} = 5V	AV_{DD} = 3V	AV_{DD} < 3.0V
DACREF = AV_{DD}	Full Range	Full Range	Not Recommended
DACREF = 2.5V	Full Range	Not Recommended	Not Recommended
DACREF = 1.25V	Full Range	Full Range	Not Recommended

TABLE IV. Voltage DAC Code Range.

DAC REFERENCE	AV_{DD} = 5V	AV_{DD} = 3V	AV_{DD} < 3.0V
DACREF = AV_{DD}	0000-7FFF$_H$	0000-3FFF$_H$	Not Recommended
DACREF = 2.5V	Full Range	Not Recommended	Not Recommended
DACREF = 1.25V	Full Range	Full Range	Not Recommended

TABLE V. Current DAC Code Range.

DAC LOADING

The DAC can be selected to be turned off with a 1kΩ, 100kΩ, or open circuit on the DAC outputs.

BIPOLAR OPERATION USING THE DAC

The DAC can be used for a bipolar output range, as shown in Figure 10. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

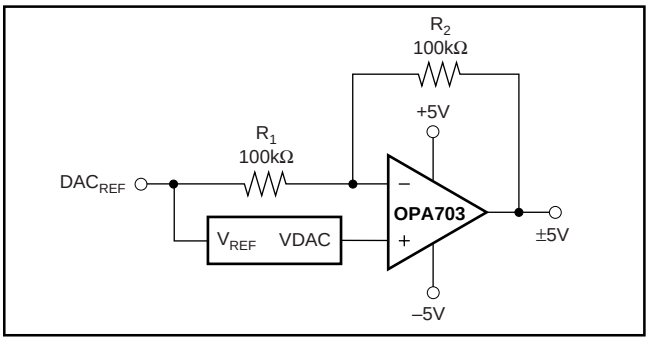


FIGURE 10. Bipolar Operation with the DAC.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[DAC_{REF} \bullet \left(\frac{D}{65536} \right) \bullet \left(\frac{R_1 + R_2}{R_1} \right) - DAC_{REF} \bullet \left(\frac{R_2}{R_1} \right) \right]$$

where D represents the input code in decimal (0–65535).

With DAC_{REF} = 5V, $R_1 = R_2$ = 10kΩ:

$$V_O = \left(\frac{10 \bullet D}{65536} \right) - 5V$$

This is an output voltage range of ±5V with 0000_H corresponding to a –5V output and $FFFF_H$ corresponding to a +5V output. Similarly, using V_{REF} = 2.5V, a ±2.5V output voltage can be achieved.

IDAC

The compliance specification of the IDAC output defines the maximum output voltage to achieve the expected current. Refer to Figure 9 for the IDAC structure and to Table V for the DAC reference selection and code range.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The built-in (on-chip) power-on reset circuitry was designed to accommodate analog or digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically at the specified rate. If BOR is enabled, the ramp rate can be slower.

MEMORY MAP

The MSC1211 contains on-chip SFR, Flash Memory, Scratchpad RAM Memory, Boot ROM, and SRAM. The SFR registers are primarily used for control and status. The standard 8051 features and additional peripheral features of the MSC1211 are controlled through the SFR. Reading from undefined SFR will return zero and writing to undefined SFR registers is not recommended and will have indeterminate effects.

Flash Memory is used for both Program Memory and Data Memory. The user has the ability to select the partition size of Program and Data Memories. The partition size is set through hardware configuration bits, which are programmed through either the parallel or serial programming methods. Both Program and Data Flash Memories are erasable and writable (programmable) in user application mode. However, only program execution can occur from Program Memory. As an added precaution, a lock feature can be activated through the hardware configuration bits, which disables erase and writes to 4kB of Program Flash Memory or the entire Program Flash Memory in user application mode.

The MSC1211 includes 1kB of SRAM on-chip. SRAM starts at address 0 and is accessed through the MOVX instruction. This SRAM can also be located to start at 8400_H and can be accessed as both Program and Data Memory.

FLASH MEMORY

The MSC1211 uses a memory addressing scheme that separates Program Memory (FLASH/ROM) from Data Memory (FLASH/RAM). Each area is 64kB beginning at address 0000_H and ending at $FFFF_H$, as shown in Figure 11. The program and data segments can overlap since they are accessed in different ways. Program Memory is fetched by the microcontroller automatically. There is one instruction (MOVC) that is used to explicitly read the program area. This is commonly used to read lookup tables. The Data Memory area is accessed explicitly using the MOVX instruction. This instruction provides multiple ways of specifying the target address. It is used to access the 64kB of Data Memory. The address and data range of devices with on-chip Program and Data Memory overlap the 64kB memory space. When on-chip memory is enabled, accessing memory in the on-chip range will cause the device to access internal memory. Memory accesses beyond the internal range will be addressed externally via Ports 0 and 2.

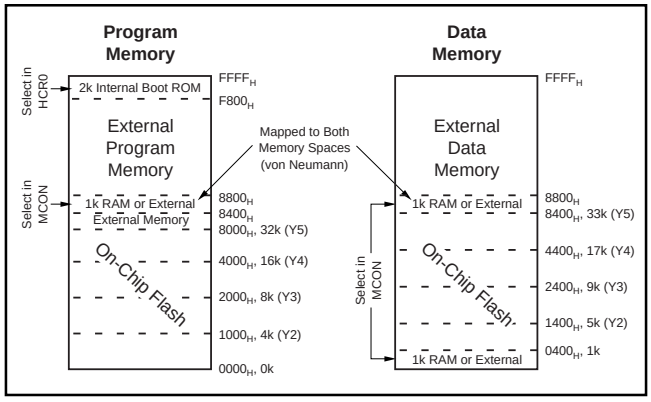


FIGURE 11. Memory Map.

The MSC1211 has two Hardware Configuration registers (HCR0 and HCR1) that are programmable only during Flash Memory Programming mode.

The MSC1211 allows the user to partition the Flash Memory between Program Memory and Data Memory. For instance, the MSC1211Y5 contains 32kB of Flash Memory on-chip. Through the HW configuration registers, the user can define the partition between Program Memory (PM) and Data Memory (DM), as shown in Tables VI and VII. The MSC1211 family offers four memory configurations.

HCR0	MSC1211Y2		MSC1211Y3		MSC1211Y4		MSC1211Y5	
DFSEL	PM	DM	PM	DM	PM	DM	PM	DM
000	0kB	4kB	0kB	8kB	0kB	16kB	0kB	32kB
001	0kB	4kB	0kB	8kB	0kB	16kB	0kB	32kB
010	0kB	4kB	0kB	8kB	0kB	16kB	16kB	16kB
011	0kB	4kB	0kB	8kB	8kB	8kB	24kB	8kB
100	0kB	4kB	4kB	4kB	12kB	4kB	28kB	4kB
101	2kB	2kB	6kB	2kB	14kB	2kB	30kB	2kB
110	3kB	1kB	7kB	1kB	15kB	1kB	31kB	1kB
111 (default)	4kB	0kB	8kB	0kB	16kB	0kB	32kB	0kB

NOTE: When a 0kB program memory configuration is selected program execution is external.

TABLE VI. MSC1211Y Flash Partitioning.

HCR0	MSC1211Y2		MSC1211Y3		MSC1211Y4		MSC1211Y5	
DFSEL	PM	DM	PM	DM	PM	DM	PM	DM
000	0000	0400-13FF	0000	0400-23FF	0000	0400-43FF	0000	0400-83FF
001	0000	0400-13FF	0000	0400-23FF	0000	0400-43FF	0000	0400-83FF
010	0000	0400 13FF	0000	0400 23FF	0000	0400 43FF	0000-3FFF	0400-43FF
011	0000	0400-13FF	0000	0400-23FF	0000-1FFF	0400-23FF	0000-5FFF	0400-23FF
100	0000	0400-13FF	0000-0FFF	0400-13FF	0000-2FFF	0400-13FF	0000-6FFF	0400-13FF
101	0000-07FF	0400-0BFF	0000-17FF	0400-0BFF	0000-37FF	0400-0BFF	0000-77FF	0400-0BFF
110	0000-0BFF	0400-07FF	0000-1BFF	0400-07FF	0000-3BFF	0400-07FF	0000-7BFF	0400-07FF
111 (default)	0000-0FFF	0000	0000-1FFF	0000	0000-3FFF	0000	0000-7FFF	0000

NOTE: Program memory accesses above the highest listed address will access external program memory.

TABLE VII. Flash Memory Partitioning.

It is important to note that the Flash Memory is readable and writable (depending on the MXWS bit in the MWS SFR) by the user through the MOVX instruction when configured as either Program or Data Memory. This means that the user may partition the device for maximum Flash Program Memory size (no Flash Data Memory) and use Flash Program Memory as Flash Data Memory. This may lead to undesirable behavior if the PC points to an area of Flash Program Memory that is being used for data storage. Therefore, it is recommended to use Flash partitioning when Flash Memory is used for data storage. Flash partitioning prohibits execution of code from Data Flash Memory. Additionally, the Program Memory erase/write can be disabled through hardware configuration bits (HCR0), while still providing access (read/write/erase) to Data Flash Memory.

The effect of memory mapping on Program and Data Memory is straightforward. The Program Memory is decreased in size from the top of internal Program Memory. Therefore, if the MSC1211Y5 is partitioned with 31kB of Flash Program Memory and 1kB of Flash Data Memory, external Program Memory execution will begin at $7C00_H$ (versus 8000_H for 32kB). The Flash Data Memory is added on top of the SRAM memory. Therefore, access to Data Memory (through MOVX) will access SRAM for addresses 0000_H-$03FF_H$ and access Flash Memory for addresses 0400_H-$07FF_H$.

Data Memory

The MSC1211 can address 64kB of Data Memory. Scratchpad Memory provides 256 bytes in addition to the 64kB of Data Memory. The MOVX instruction is used to access the Data SRAM Memory. This includes 1024 bytes of on-chip Data SRAM Memory. The data bus values do not appear on Port 0 (during data bus timing) for internal memory access.

The MSC1211 also has on-chip Flash Data Memory which is readable and writable (depending on Memory Write Select register) during normal operation (full V_{DD} range). This memory is mapped into the external Data Memory space directly above the SRAM.

REGISTER MAP

The Register Map is illustrated in Figure 12. It is entirely separate from the Program and Data Memory areas mentioned before. A separate class of instructions is used to access the registers. There are 256 potential register locations. In practice, the MSC1211 has 256 bytes of Scratchpad RAM and up to 128 SFRs. This is possible, since the upper 128 Scratchpad RAM locations can only be accessed indirectly. That is, the contents of a Working Register (described below) will designate the RAM location. Thus, a direct reference to one of the upper 128 locations must be an SFR access. Direct RAM is reached at locations 0 to $7F_H$ (0 to 127).

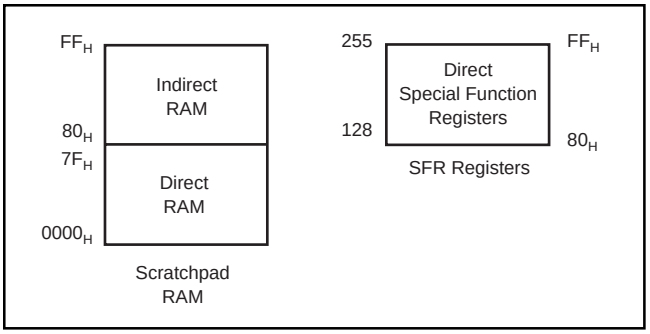


FIGURE 12. Register Map.

SFRs are accessed directly between 80_H and FF_H (128 to 255). The RAM locations between 128 and 255 can be reached through an indirect reference to those locations. Scratchpad RAM is available for general-purpose data storage. It is commonly used in place of off-chip RAM when the total data contents are small. When off-chip RAM is needed, the Scratchpad area will still provide the fastest general-purpose access. Within the 256 bytes of RAM, there are several special-purpose areas.

Bit Addressable Locations

In addition to direct register access, some individual bits are also accessible. These are individually addressable bits in both the RAM and SFR area. In the Scratchpad RAM area, registers 20_H to $2F_H$ are bit addressable. This provides 128 (16 • 8) individual bits available to software. A bit access is distinguished from a full-register access by the type of instruction. In the SFR area, any register location ending in a 0 or 8 is bit addressable. Figure 13 shows details of the on-chip RAM addressing including the locations of individual RAM bits.

Working Registers

As part of the lower 128 bytes of RAM, there are four banks of Working Registers, as shown in Figure 13. The Working Registers are general-purpose RAM locations that can be addressed in a special way. They are designated R0 through R7. Since there are four banks, the currently selected bank will be used by any instruction using R0-R7. This allows software to change context by simply switching banks. This is controlled via the Program Status Word register (PSW; $0D0_H$) in the SFR area described below. Registers R0 and R1 also allow their contents to be used for indirect addressing of the upper 128 bytes of RAM. Thus, an instruction can designate the value

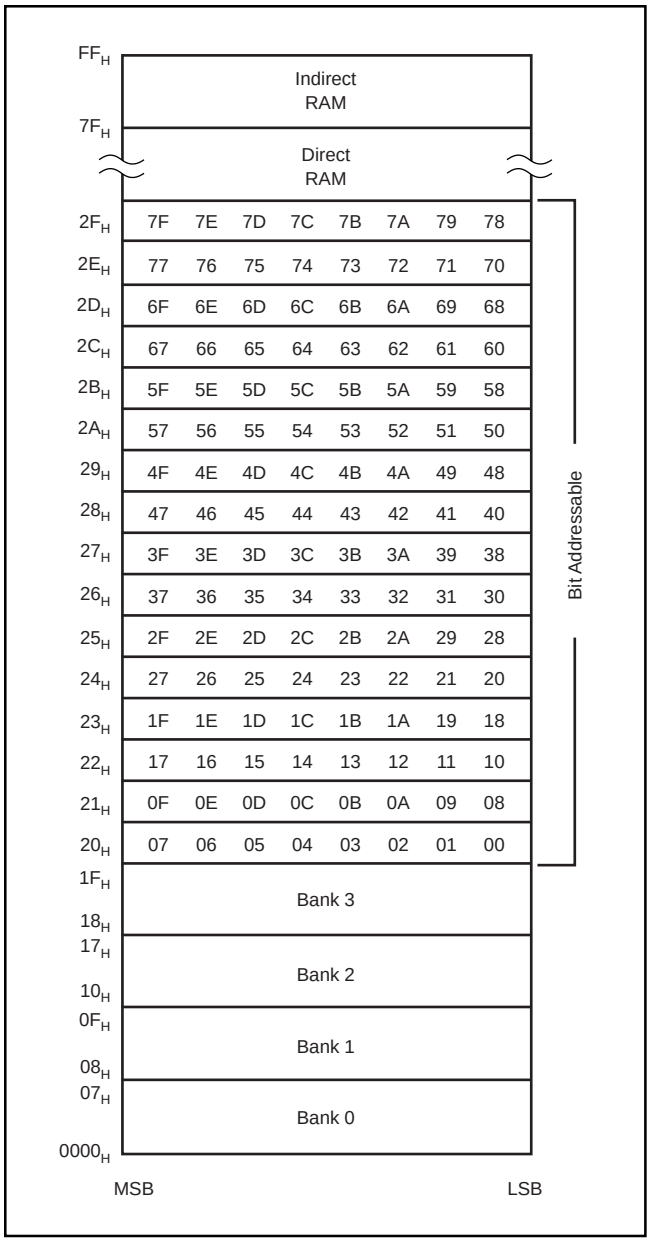


FIGURE 13. Scratchpad Register Addressing.

stored in R0 (for example) to address the upper RAM. The 16 bytes immediately above the these registers are bit addressable. So any of the 128 bits in this area can be directly accessed using bit addressable instructions.

Stack

Another use of the Scratchpad area is for the programmer's stack. This area is selected using the Stack Pointer (SP; 81_H) SFR. Whenever a call or interrupt is invoked, the return address is placed on the Stack. It also is available to the programmer for variables, etc., since the Stack can be moved and there is no fixed location within the RAM designated as Stack. The Stack Pointer will default to 07_H on reset. The user can then move it as needed. A convenient location would be the upper RAM area (> $7F_H$) since this is only available indirectly. The SP will point to the last used value. Therefore, the next value placed on the Stack is put at SP + 1. Each PUSH or CALL will increment the SP by the appropriate value. Each POP or RET will decrement as well.

Program Memory

After reset, the CPU begins execution from Program Memory location 0000_H. The selection of where Program Memory execution begins is made by tying the $\overline{EA}$ pin to V_{DD} for internal access, or DGND for external access. When $\overline{EA}$ is tied to V_{DD}, any PC fetches outside the internal Program Memory address occur from external memory. If $\overline{EA}$ is tied to DGND, then all PC fetches address external memory. The standard internal Program Memory size for MSC1211 family members is shown in Table VIII. Refer to the Accessing External Memory section for details on using external Program Memory. If enabled the Boot ROM will appear from address $F800_H$ to $FFFF_H$.

MODEL NUMBER	STANDARD INTERNAL PROGRAM MEMORY SIZE (BYTES)
MSC1211Y5	32k
MSC1211Y4	16k
MSC1211Y3	8k
MSC1211Y2	4k

TABLE VIII. MSC1211 Maximum Internal Program Memory Sizes.

ACCESSING EXTERNAL MEMORY

If external memory is used, P0 and P2 can be configured as address and data lines. If external memory is not used, P0 and P2 can be configured as general-purpose I/O lines through the Hardware Configuration Register.

To enable access to external memory bits 0 and 1 of the HCR1 register must be set to 0. When these bits are enabled all memory accesses for both internal and external memory will appear on ports 0 and 2. During the data portion of the cycle for internal memory, Port 0 will be zero for security purposes.

Accesses to external memory are of two types: accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory.

External Program Memory and external Data Memory may be combined if desired by applying the $\overline{RD}$ and $\overline{PSEN}$ signals to the inputs of an AND gate and using the output of the gate as the read strobe to the external Program/Data Memory.

A program fetch from external Program Memory uses a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @DPTR) or an 8-bit address (MOVX @R_I).

If Port 2 is selected for external memory use (HCR1, bit 0), it can not be used as a general-purpose I/O. This bit (or Bit 1 of HCR1) also forces bits P3.6 and P3.7 to be used for $\overline{WR}$ and $\overline{RD}$ instead of I/O. Port 2, P3.6, and P3.7 should all be written to '1'.

If an 8-bit address is being used (MOVX @R_I), the contents of the MPAGE (92_H) SFR remain at the Port 2 pins throughout the external memory cycle. This will facilitate paging.

In any case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDR/DATA signals use CMOS drivers in the Port 0, Port 2, $\overline{WR}$, and $\overline{RD}$ output buffers. Thus, in this application the Port 0 pins are not open-drain outputs, and do not require external pull-ups for high-speed access. Signal ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated.

The function of Port 0 and Port 2 is selected in Hardware Configuration Register 1. This can only be changed during the Flash Program mode. There is no conflict in the use of these registers; they will either be used as general-purpose I/O or for external memory access. The default state is for Port 0 and Port 2 to be used as general-purpose I/O. If an external memory access is attempted when they are configured as general-purpose I/O, the values of Port 0 and Port 2 will not be affected.

External Program Memory is accessed under two conditions:

1) Whenever signal $\overline{EA}$ is LOW during reset, then all future accesses are external, or

2) Whenever the Program Counter (PC) contains a number that is outside of the internal Program Memory address range, if the ports are enabled.

If Port 0 and Port 2 is selected for external memory, all 8 bits of Port 0 and Port 2, as well as P3.6 and P3.7, are dedicated to an output function and may not be used for general-purpose I/O. During external program fetches, Port 2 outputs the high byte of the PC.

Programming Flash Memory

There are four sections of Flash Memory for programming.

1. 128 configuration bytes.
2. Reset sector (4kB) (not to be confused with the 2kB Boot ROM).
3. Program Memory.
4. Data Memory.

Boot Rom

There is a 2kB Boot ROM that controls operation during serial or parallel programming. Additionally, the Boot ROM routines can be accessed during the user mode if it is enabled. When enabled, the Boot ROM routines will be located at memory addresses $F800_H$-$FFFF_H$ during user mode. In program mode the Boot ROM is located in the first 2kB of Program Memory.

Flash Programming Mode

There are two programming modes: parallel and serial. The programming mode is selected by the state of the ALE and $\overline{PSEN}$ signals during power-on reset. Serial programming mode is selected with $\overline{PSEN}$ = 0 and ALE = 1. Parallel programming mode is selected with $\overline{PSEN}$ = 1 and ALE = 0 (see Figure 14). If they are both HIGH, the MSC1211 will operate in normal user mode. Both signals LOW is a reserved mode and is not defined. Programming mode is exited with a power-on reset signal and the normal mode selected.

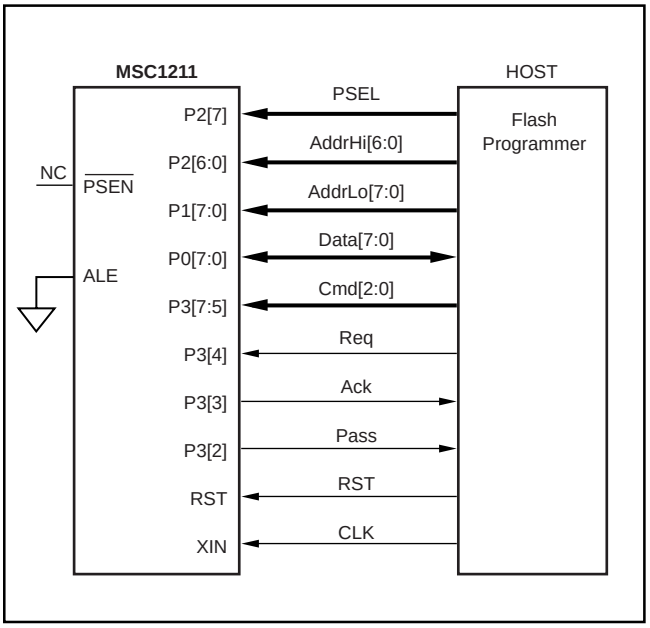


FIGURE 14. Parallel Programming Configuration.

The MSC1211 is shipped with Flash Memory erased (all 1's). Parallel programming methods typically involve a third-party programmer. Serial programming methods typically involve in-system programming. User Application mode allows Flash Program and Data Memory programming. The actual code for Flash programming can not execute from Flash. That code must execute from the Boot ROM or internal (von Neumann) RAM.

INTERRUPTS

The MSC1211 uses a three-priority interrupt system. As shown in Table IX, each interrupt source has an independent priority bit, flag, interrupt vector, and enable (except that nine interrupts share the Auxilliary Interrupt (AI) at the highest priority). In addition, interrupts can be globally enabled or disabled. The interrupt structure is compatible with the original 8051 family. All of the standard interrupts are available.

HARDWARE CONFIGURATION MEMORY

The 128 configuration bytes can only be written during the program mode. The bytes are accessed through SFR registers CADDR (SFR 93_H) and CDATA (SFR 94_H). Two of the configuration bytes control Flash partitioning and system control. If the security bit is set, these bits can not be changed except with a Mass Erase command that erases all of the Flash Memory including the 128 configuration bytes.

INTERRUPT/EVENT	INTERRUPT ADDR	INTERRUPT NUM	PRIORITY	FLAG	PRIORITY ENABLE	CONTROL
DV_{DD} Low Voltage/HW Breakpoint	33_H	6	HIGH 0	EDLVB (AIE.0)(1) EBP (BPCON.0)(1)	EDLVV (AIE.0)(1) EBP (BPCON.0)(1)	N/A
AV_{DD} Low Voltage	33_H	6	0	EALV (AIE.1)(1)	EALV (AIE.1)(1)	N/A
SPI Receive / I^2C	33_H	6	0	ESPIR (AIE.2)(1)	ESPIR (AIE.2)(1)	N/A
SPI Transmit	33_H	6	0	ESPIT (AIE.3)(1)	ESPIT (AIE.3)(1)	N/A
Milliseconds Timer	33_H	6	0	EMSEC (AIE.4)(1)	EMSEC (AIE.4)(1)	N/A
ADC	33_H	6	0	EADC (AIE.5)(1)	EADC (AIE .5)(1)	N/A
Summation Register	33_H	6	0	ESUM (AIE.6)(1)	ESUM (AIE.6)(1)	N/A
Seconds Timer	33_H	6	0	ESEC (AIE.7)(1)	ESEC (AIE.7)(1)	N/A
External Interrupt 0	03_H	0	1	IE0 (TCON.1)(2)	EX0 (IE.0)(4)	PX0 (IP.0)
Timer 0 Overflow	$0B_H$	1	2	TF0 (TCON.5)(3)	ET0 (IE.1)(4)	PT0 (IP.1)
External Interrupt 1	13_H	2	3	IE1 (TCON.3)(2)	EX1 (IE.2)(4)	PX1 (IP.2)
Timer 1 Overflow	$1B_H$	3	4	TF1 (TCON.7)(3)	ET1 (IE.3)(4)	PT1 (IP.3)
Serial Port 0	23_H	4	5	RI_0 (SCON0.0) TI_0 (SCON0.1)	ES0 (IE.4)(4)	PS0 (IP.4)
Timer 2 Overflow	$2B_H$	5	6	TF2 (T2CON.7)	ET2 (IE.5)(4)	PT2 (IP.5)
Serial Port 1	$3B_H$	7	7	RI_1 (SCON1.0) TI_1 (SCON1.1)	ES1 (IE.6)(4)	PS1 (IP.6)
External Interrupt 2	43_H	8	8	IE2 (EXIF.4)	EX2 (EIE.0)(4)	PX2 (IP.0)
External Interrupt 3	$4B_H$	9	9	IE3 (EXIF.5)	EX3 (EIE.1)(4)	PX3 (IP.1)
External Interrupt 4	53_H	10	10	IE4 (EXIF.6)	EX4 (EIE.2)(4)	PX4 (IP.2)
External Interrupt 5	$5B_H$	11	11	IE5 (EXIF.7)	EX5 (EIE.3)(4)	PX5 (IP.3)
Watchdog	63_H	12	12 LOW	WDTI (EICON.3)	EWDI (EIE.4)(4)	PWDI (IP.4)

NOTES: (1) These interrupts set the AI flag (EICON.4) and are enabled by EAI (EICON.5). (2) If edge triggered, cleared automatically by hardware when the service routine is vectored to. If level triggered, the flag follows the state of the pin. (3) Cleared automatically by hardware when interrupt vector occurs. (4) Globally enabled by $\overline{EA}$ (IE.7).

TABLE IX. Interrupt Summary.

Hardware Configuration Register 0 (HCR0)—Accessed Using SFR Registers CADDR and CDATA.

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CADDR $7F_H$	EPMA	PML	RSL	EBR	EWDR	DFSEL2	DFSEL1	DFSEL0

For access to this register during normal operation, refer to the register descriptions for CADDR and CDATA.

EPMA Enable Programming Memory Access (Security Bit).

bit 7 0: After reset in programming modes, Flash Memory can only be accessed in UAM mode until a mass erase is done.

1: Fully Accessible (default)

PML Program Memory Lock. (PML has Priority Over RSL)

bit 6 0: Enable all Flash Programming Modes in program mode, can be written in UAM.

1: Enable read only for program mode, can't be written in UAM (default).

RSL Reset Sector Lock.

bit 5 0: Enable Reset Sector Writing

1: Enable Read Only Mode for Reset Sector (4kB) (default)

EBR Enable Boot Rom. Boot Rom is 2kB of code located in ROM, not to be confused with the 4kB Boot Sector located in Flash Memory.

bit 4 0: Disable Internal Boot Rom

1: Enable Internal Boot Rom (default)

EWDR Enable Watchdog Reset.

bit 3 0: Disable Watchdog Reset

1: Enable Watchdog Reset (default)

DFSEL Data Flash Memory Size. (see Table III)

bits 2-0 000: Reserved

001: 32kB, 16kB, 8kB, or 4kB Data Flash Memory

010: 16kB, 8kB, or 4kB Data Flash Memory

011: 8kB or 4kB Data Flash Memory

100: 4kB Data Flash Memory

101: 2kB Data Flash Memory

110: 1kB Data Flash Memory

111: No Data Flash Memory (default)

The reset sector can be used to provide another method of Flash Memory programming. This will allow Program Memory updates without changing the jumpers for in-circuit code updates or program development. The code in this boot sector would then provide the monitor and programming routines with the ability to jump into the main Flash code when programming is finished.

Hardware Configuration Register 1 (HCR1)

	7	6	5	4	3	2	1	0
CADDR $7E_H$	DBLSEL1	DBLSEL0	ABLSEL1	ABLSEL0	DAB	DDB	EGP0	EGP23

For access to this register during normal operation, refer to the register descriptions for CADDR and CDATA.

DBLSEL Digital Brownout Level Select

bits 7-6 00: 4.5V

01: 4.2V

10: 2.7V

11: 2.5V (default)

ABLSEL Analog Brownout Level Select

bits 5-4 00: 4.5V

01: 4.2V

10: 2.7V

11: 2.5V (default)

DAB Disable Analog Power-Supply Brownout Detection

bit 3 0: Enable Analog Brownout Detection

1: Disable Analog Brownout Detection (default).

DDB Disable Digital Power-Supply Brownout Detection

bit 2 0: Enable Digital Brownout Detection

1: Disable Digital Brownout Detection (default)

EGP0 Enable General-Purpose I/O for Port 0

bit 1 0: Port 0 is Used for External Memory, P3.6 and P3.7 Used for $\overline{WR}$ and $\overline{RD}$.

1: Port 0 is Used as General-Purpose I/O (default)

EGP23 Enable General-Purpose I/O for Ports 2 and 3

bit 0 0: Port 2 is Used for External Memory, P3.6 and P3.7 Used for $\overline{WR}$ and $\overline{RD}$.

1: Port 2 and Port3 are Used as General-Purpose I/O (default)

Configuration Memory Programming

Certain key functions such as Brownout Reset and Watchdog Timer are controlled by the hardware configuration bits. These bits are nonvolatile and can only be changed through serial and parallel programming. Other peripheral control and status functions, such as ADC configuration timer setup, and Flash control are controlled through the SFRs.

SFR Definitions (Boldface is unique to the MSC1211)

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUES
80_H	P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FF_H
81_H	SP									07_H
82_H	DPL0									00_H
83_H	DPH0									00_H
84_H	**DPL1**									**00_H**
85_H	**DPH1**									**00_H**
86_H	**DPS**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	**00_H**
87_H	**PCON**	**SMOD**	**0**	**1**	**1**	**GF1**	**GF0**	**STOP**	**IDLE**	**30_H**
88_H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00_H
89_H	TMOD	|----------Timer 1 ----------|				|----------Timer 0 ----------|				00_H
		GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	
$8A_H$	TL0									00_H
$8B_H$	TL1									00_H
$8C_H$	TH0									00_H
$8D_H$	TH1									00_H
$8E_H$	**CKCON**	**0**	**0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	**01_H**
$8F_H$	**MWS**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**MXWS**	**00_H**
90_H	P1	P1.7 $\overline{INT5}$/SCLK/SCK	P1.6 INT4/MISO/SDA	P1.5 $\overline{INT3}$/MOSI	P1.4 INT2/$\overline{SS}$	P1.3 TXD1	P1.2 RXD1	P1.1 T2EX	P1.0 T2	FF_H
91_H	EXIF	IE5	IE4	IE3	IE2	1	0	0	0	08_H
92_H	**MPAGE**									**00_H**
93_H	**CADDR**									**00_H**
94_H	**CDATA**									**00_H**
95_H	**MCON**	**BPSEL**	**0**	**0**					**RAMMAP**	**00_H**
96_H										
97_H										
98_H	SCON0	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00_H
99_H	SBUF0									00_H
$9A_H$	**SPICON** **I2CCON**	**SCLK2** **START**	**SCLK1** **STOP**	**SCLK0** **ACK**	**FIFO** **0**	**ORDER** **FAST**	**MSTR** **MSTR**	**CPHA** **SCLS**	**CPOL** **FILEN**	**00_H**
$9B_H$	**SPIDATA** **I2CDATA**									**00_H**
$9C_H$	**SPIRCON** **I2CSTAT**	**RXCNT7** **RXFLUSH** **GCMEN**	**RXCNT6**	**RXCNT5**	**RXCNT4**	**RXCNT3**	**RXCNT2** **RXIRQ2**	**RXCNT1** **RXIRQ1**	**RXCNT0** **RXIRQ0**	**00_H**
$9D_H$	**SPITCON** **I2CGM**	**TXCNT7** **TXFLUSH** **STAT7** **SCKD7/SAE**	**TXCNT6** **STAT6** **SCKD6/SA6**	**TXCNT5** **CLK_EN** **STAT5** **SCKD5/SA5**	**TXCNT4** **DRV_DLY** **STAT4** **SCKD4/SA4**	**TXCNT3** **DRV_EN** **STAT3** **SCKD3/SA3**	**TXCNT2** **TXIRQ2** **0** **SCKD2/SA2**	**TXCNT1** **TXIRQ1** **0** **SCKD1/SA1**	**TXCNT0** **TXIRQ0** **0** **SCKD0/SA0**	**00_H**
$9E_H$	**SPISTART**	**1**								**80_H**
$9F_H$	**SPIEND**	**1**								**80_H**
$A0_H$	P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FF_H
$A1_H$	**PWMCON**			**PPOL**	**PWMSEL**	**SPDSEL**	**TPCNTL2**	**TPCNTL1**	**TPCNTL0**	**00_H**
$A2_H$	**PWMLOW** **TONELOW**	**PWM7** **TDIV7**	**PWM6** **TDIV6**	**PWM5** **TDIV5**	**PWM4** **TDIV4**	**PWM3** **TDIV3**	**PWM2** **TDIV2**	**PWM1** **TDIV1**	**PWM0** **TDIV0**	**00_H**
$A3_H$	**PWMHI** **TONEHI**	**PWM15** **TDIV15**	**PWM14** **TDIV14**	**PWM13** **TDIV13**	**PWM12** **TDIV12**	**PWM11** **TDIV11**	**PWM10** **TDIV10**	**PWM9** **TDIV9**	**PWM8** **TDIV8**	**00_H**
$A4_H$										
$A5_H$	**PAI**	**0**	**0**	**0**	**0**	**PAI3**	**PAI2**	**PAI1**	**PAI0**	**00_H**
$A6_H$	**AIE**	**ESEC**	**ESUM**	**EADC**	**EMSEC**	**ESPIT**	**ESPIR/EI2C**	**EALV**	**EDLVB**	**00_H**
$A7_H$	**AISTAT**	**SEC**	**SUM**	**ADC**	**MSEC**	**SPIT**	**SPIR/I2CSI**	**ALVD**	**DLVD**	**00_H**
$A8_H$	IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00_H
$A9_H$	**BPCON**	**BP**	**0**	**0**	**0**	**0**	**0**	**PMSEL**	**EBP**	**00_H**
AA_H	**BPL**									
AB_H	**BPH**									
AC_H	**P0DDRL**	**P03H**	**P03L**	**P02H**	**P02L**	**P01H**	**P01L**	**P00H**	**P00L**	**00_H**
AD_H	**P0DDRH**	**P07H**	**P07L**	**P06H**	**P06L**	**P05H**	**P05L**	**P04H**	**P04L**	**00_H**
AE_H	**P1DDRL**	**P13H**	**P13L**	**P12H**	**P12L**	**P11H**	**P11L**	**P10H**	**P10L**	**00_H**
AF_H	**P1DDRH**	**P17H**	**P17L**	**P16H**	**P16L**	**P15H**	**P15L**	**P14H**	**P14L**	**00_H**
$B0_H$	P3	P3.7 $\overline{RD}$	P3.6 $\overline{WR}$	P3.5 T1	P3.4 T0	P3.3 $\overline{INT1}$	P3.2 $\overline{INT0}$	P3.1 TXD0	P3.0 RXD0	FF_H
$B1_H$	**P2DDRL**	**P23H**	**P23L**	**P22H**	**P22L**	**P21H**	**P21L**	**P20H**	**P20L**	**00_H**
$B2_H$	**P2DDRH**	**P27H**	**P27L**	**P26H**	**P26L**	**P25H**	**P25L**	**P24H**	**P24L**	**00_H**
$B3_H$	**P3DDRL**	**P33H**	**P33L**	**P32H**	**P32L**	**P31H**	**P31L**	**P30H**	**P30L**	**00_H**
$B4_H$	**P3DDRH**	**P37H**	**P37L**	**P36H**	**P36L**	**P35H**	**P35L**	**P34H**	**P34L**	**00_H**
$B5_H$	**DACL**									
$B6_H$	**DACH**									
$B7_H$	**DACCON**	**DSEL7**	**DSEL6**	**DSEL5**	**DSEL4**	**DSEL3**	**DSEL2**	**DSEL1**	**DSEL0**	**00_H**
$B8_H$	IP	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	80_H

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET VALUES
$B9_H$										
BA_H										
BB_H										
BC_H										
BD_H										
BE_H										
BF_H										
$C0_H$	SCON1	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00_H
$C1_H$	SBUF1									00_H
$C2_H$										
$C3_H$										
$C4_H$										
$C5_H$										
$C6_H$	**EWU**						**EWUWDT**	**EWUEX1**	**EWUEX0**	**00_H**
$C7_H$	**SYSCLK**	**0**	**0**	**DIVMOD1**	**DIVMOD0**	**0**	**DIV2**	**DIV1**	**DIV0**	**00_H**
$C8_H$	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00_H
$C9_H$										
CA_H	RCAP2L									00_H
CB_H	RCAP2H									00_H
CC_H	TL2									00_H
CD_H	TH2									00_H
CE_H										
CF_H										
$D0_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P	00_H
$D1_H$	**OCL**								**LSB**	**00_H**
$D2_H$	**OCM**									**00_H**
$D3_H$	**OCH**	**MSB**								**00_H**
$D4_H$	**GCL**								**LSB**	**24_H**
$D5_H$	**GCM**									**90_H**
$D6_H$	**GCH**	**MSB**								**67_H**
$D7_H$	**ADMUX**	**INP3**	**INP2**	**INP1**	**INP0**	**INN3**	**INN2**	**INN1**	**INN0**	**01_H**
$D8_H$	EICON	SMOD1	1	EAI	AI	WDTI	0	0	0	40_H
$D9_H$	**ADRESL**								**LSB**	**00_H**
DA_H	**ADRESM**									**00_H**
DB_H	**ADRESH**	**MSB**								**00_H**
DC_H	**ADCON0**	**—**	**BOD**	**EVREF**	**VREFH**	**EBUF**	**PGA2**	**PGA1**	**PGA0**	**38_H**
DD_H	**ADCON1**	**—**	**POL**	**SM1**	**SM0**	**—**	**CAL2**	**CAL1**	**CAL0**	**$x000\_0000_B$**
DE_H	**ADCON2**	**DR7**	**DR6**	**DR5**	**DR4**	**DR3**	**DR2**	**DR1**	**DR0**	**$1B_H$**
DF_H	**ADCON3**	**0**	**0**	**0**	**0**	**0**	**DR10**	**DR9**	**DR8**	**06_H**
$E0_H$	ACC									00_H
$E1_H$	**SSCON**	**SSCON1**	**SSCON0**	**SCNT2**	**SCNT1**	**SCNT0**	**SHF2**	**SHF1**	**SHF0**	**00_H**
$E2_H$	**SUMR0**									**00_H**
$E3_H$	**SUMR1**									**00_H**
$E4_H$	**SUMR2**									**00_H**
$E5_H$	**SUMR3**									**00_H**
$E6_H$	**ODAC**									**00_H**
$E7_H$	**LVDCON**	**ALVDIS**	**ALVD2**	**ALVD1**	**ALVD0**	**DLVDIS**	**DLVD2**	**DLVD1**	**DLVD0**	**00_H**
$E8_H$	EIE	1	1	1	EWDI	EX5	EX4	EX3	EX2	$E0_H$
$E9_H$	**HWPC0**						**1**	**MEMORY SIZE**		**0000_01xx_B**
EA_H	**HWPC1**					**1**				**08_H**
EB_H	**HWVER**									
EC_H	**Reserved**									**00_H**
ED_H	**Reserved**									**00_H**
EE_H	**FMCON**	**0**	**PGERA**	**0**	**FRCM**	**0**	**BUSY**	**1**	**0**	**02_H**
EF_H	**FTCON**	**FER3**	**FER2**	**FER1**	**FER0**	**FWR3**	**FWR2**	**FWR1**	**FWR0**	**$A5_H$**
$F0_H$	B									00_H
$F1_H$	**PDCON**	**0**	**PDDAC**	**PDI2C**	**PDPWM**	**PDAD**	**PDWDT**	**PDST**	**PDSPI**	**$7F_H$**
$F2_H$	**PASEL**	**0**	**0**	**PSEN2**	**PSEN1**	**PSEN0**	**0**	**ALE1**	**ALE0**	**00_H**
$F3_H$										
$F4_H$										
$F5_H$										
$F6_H$	**ACLK**	**0**	**FREQ6**	**FREQ5**	**FREQ4**	**FREQ3**	**FREQ2**	**FREQ1**	**FREQ0**	**03_H**
$F7_H$	**SRST**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**RSTREQ**	**00_H**
$F8_H$	EIP	1	1	1	PWDI	PX5	PX4	PX3	PX2	$E0_H$
$F9_H$	**SECINT**	**WRT**	**SECINT6**	**SECINT5**	**SECINT4**	**SECINT3**	**SECINT2**	**SECINT1**	**SECINT0**	**$7F_H$**
FA_H	**MSINT**	**WRT**	**MSINT6**	**MSINT5**	**MSINT4**	**MSINT3**	**MSINT2**	**MSINT1**	**MSINT0**	**$7F_H$**
FB_H	**USEC**	**0**	**0**	**FREQ5**	**FREQ4**	**FREQ3**	**FREQ2**	**FREQ1**	**FREQ0**	**03_H**
FC_H	**MSECL**									**$9F_H$**
FD_H	**MSECH**									**$0F_H$**
FE_H	**HMSEC**									**63_H**
FF_H	**WDTCON**	**EWDT**	**DWDT**	**RWDT**	**WDCNT4**	**WDCNT3**	**WDCNT2**	**WDCNT1**	**WDCNT0**	**00_H**

Port 0 (P0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 80_H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FF_H

P0.7-0 bits 7-0 Port 0. This port functions as a multiplexed address/data bus during external memory access, and as a general-purpose I/O port when external memory access is not needed. During external memory cycles, this port will contain the LSB of the address when ALE is HIGH, and Data when ALE is LOW. When used as a general-purpose I/O, this port drive is selected by P0DDRL and P0DDRH (AC_H, AD_H). Whether Port 0 is used as general-purpose I/O or for external memory access is determined by the Flash Configuration Register (HCR1.1) (see SFR CADDR 93_H).

Stack Pointer (SP)

	7	6	5	4	3	2	1	0	Reset Value
SFR 81_H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	07_H

SP.7-0 bits 7-0 **Stack Pointer**. The stack pointer identifies the location where the stack will begin. The stack pointer is incremented before every PUSH or CALL operation and decremented after each POP or RET/RETI. This register defaults to 07_H after reset.

Data Pointer Low 0 (DPL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 82_H	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0	00_H

DPL0.7-0 bits 7-0 **Data Pointer Low 0**. This register is the low byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86_H).

Data Pointer High 0 (DPH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 83_H	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0	00_H

DPH0.7-0 bits 7-0 **Data Pointer High 0.** This register is the high byte of the standard 8051 16-bit data pointer. DPL0 and DPH0 are used to point to non-scratchpad data RAM. The current data pointer is selected by DPS (SFR 86_H).

Data Pointer Low 1 (DPL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 84_H	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0	00_H

DPL1.7-0 bits 7-0 **Data Pointer Low 1**. This register is the low byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86_H) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer High 1 (DPH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 85_H	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0	00_H

DPH1.7-0 bits 7-0 **Data Pointer High.** This register is the high byte of the auxiliary 16-bit data pointer. When the SEL bit (DPS.0) (SFR 86_H) is set, DPL1 and DPH1 are used in place of DPL0 and DPH0 during DPTR operations.

Data Pointer Select (DPS)

	7	6	5	4	3	2	1	0	Reset Value
SFR 86_H	0	0	0	0	0	0	0	SEL	00_H

SEL bit 0 **Data Pointer Select.** This bit selects the active data pointer.

0: Instructions that use the DPTR will use DPL0 and DPH0.

1: Instructions that use the DPTR will use DPL1 and DPH1.

Power Control (PCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 87_H	SMOD	0	1	1	GF1	GF0	STOP	IDLE	30_H

SMOD bit 7 — **Serial Port 0 Baud Rate Doubler Enable.** The serial baud rate doubling function for Serial Port 0.
0: Serial Port 0 baud rate will be a standard baud rate.
1: Serial Port 0 baud rate will be double that defined by baud rate generation equation.

GF1 bit 3 — **General-Purpose User Flag 1.** This is a general-purpose flag for software control.

GF0 bit 2 — **General-Purpose User Flag 0.** This is a general-purpose flag for software control.

STOP bit 1 — **Stop Mode Select.** Setting this bit will halt the oscillator and block external clocks. This bit will always read as a 0. Exit with RESET.

IDLE bit 0 — **Idle Mode Select.** Setting this bit will freeze the CPU, Timer 0, 1, and 2, and the UARTs; other peripherals remain active. This bit will always be read as a 0. Exit with AI ($A6_H$) and EWU ($C6_H$) interrupts.

Timer/Counter Control (TCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 88_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00_H

TF1 bit 7 — **Timer 1 Overflow Flag.** This bit indicates when Timer 1 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow has been detected.
1: Timer 1 has overflowed its maximum count.

TR1 — **Timer 1 Run Control.** This bit enables/disables the operation of Timer 1. Halting this timer will preserve the current bit 6 count in TH1, TL1.
0: Timer is halted.
1: Timer is enabled.

TF0 bit 5 — **Timer 0 Overflow Flag.** This bit indicates when Timer 0 overflows its maximum count as defined by the current mode. This bit can be cleared by software and is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow has been detected.
1: Timer 0 has overflowed its maximum count.

TR0 bit 4 — **Timer 0 Run Control.** This bit enables/disables the operation of Timer 0. Halting this timer will preserve the current count in TH0, TL0.
0: Timer is halted.
1: Timer is enabled.

IE1 bit 3 — **Interrupt 1 Edge Detect.** This bit is set when an edge/level of the type defined by IT1 is detected. If IT1 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 1 service routine. If IT1 = 0, this bit will inversely reflect the state of the $\overline{INT1}$ pin.

IT1 bit 2 — **Interrupt 1 Type Select.** This bit selects whether the $\overline{INT1}$ pin will detect edge or level triggered interrupts.
0: $\overline{INT1}$ is level triggered.
1: $\overline{INT1}$ is edge triggered.

IE0 bit 3 — **Interrupt 0 Edge Detect.** This bit is set when an edge/level of the type defined by IT0 is detected. If IT0 = 1, this bit will remain set until cleared in software or the start of the External Interrupt 0 service routine. If IT0 = 0, this bit will inversely reflect the state of the $\overline{INT0}$ pin.

IT0 bit 2 — **Interrupt 0 Type Select.** This bit selects whether the $\overline{INT0}$ pin will detect edge or level triggered interrupts.
0: $\overline{INT0}$ is level triggered.
1: $\overline{INT0}$ is edge triggered.

Timer Mode Control (TMOD)

	7	6	5	4	3	2	1	0	
	TIMER 1				TIMER 0				Reset Value
SFR 89_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00_H

GATE bit 7 **Timer 1 Gate Control.** This bit enables/disables the ability of Timer 1 to increment.
0: Timer 1 will clock when TR1 = 1, regardless of the state of pin $\overline{INT1}$.
1: Timer 1 will clock only when TR1 = 1 and pin $\overline{INT1}$ = 1.

C/$\overline{T}$ bit 6 **Timer 1 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on T1 pin when TR1 (TCON.6, SFR 88_H) is 1.

M1, M0 bits 5-4 **Timer 1 Mode Select.** These bits select the operating mode of Timer 1.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Timer 1 is halted, but holds its count.

GATE bit 3 **Timer 0 Gate Control.** This bit enables/disables the ability of Timer 0 to increment.
0: Timer 0 will clock when TR0 = 1, regardless of the state of pin $\overline{INT0}$ (software control).
1: Timer 0 will clock only when TR0 = 1 and pin $\overline{INT0}$ = 1 (hardware control).

C/$\overline{T}$ bit 2 **Timer 0 Counter/Timer Select.**
0: Timer is incremented by internal clocks.
1: Timer is incremented by pulses on pin T0 when TR0 (TCON.4, SFR 88_H) is 1.

M1, M0 bits 1-0 **Timer 0 Mode Select.** These bits select the operating mode of Timer 0.

M1	M0	MODE
0	0	Mode 0: 8-bit counter with 5-bit prescale.
0	1	Mode 1: 16 bits.
1	0	Mode 2: 8-bit counter with auto reload.
1	1	Mode 3: Timer 1 is halted, but holds its count.

Timer 0 LSB (TL0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8A_H$	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	00_H

TL0.7-0 bits 7-0 **Timer 0 LSB.** This register contains the least significant byte of Timer 0.

Timer 1 LSB (TL1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8B_H$	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	00_H

TL1.7-0 bits 7-0 **Timer 1 LSB.** This register contains the least significant byte of Timer 1.

Timer 0 MSB (TH0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8C_H$	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	00_H

TH0.7-0 bits 7-0 **Timer 0 MSB.** This register contains the most significant byte of Timer 0.

Timer 1 MSB (TH1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8D_H$	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	00_H

TH1.7-0 **Timer 1 MSB.** This register contains the most significant byte of Timer 1.
bits 7-0

Clock Control (CKCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8E_H$	0	0	T2M	T1M	T0M	MD2	MD1	MD0	01_H

T2M **Timer 2 Clock Select.** This bit controls the division of the system clock that drives Timer 2. This bit has no effect
bit 5 when the timer is in baud rate generator or clock output modes. Clearing this bit to 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 2 uses a divide by 12 of the crystal frequency.
1: Timer 2 uses a divide by 4 of the crystal frequency.

T1M **Timer 1 Clock Select.** This bit controls the division of the system clock that drives Timer 1. Clearing this bit to
bit 4 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 1 uses a divide by 12 of the crystal frequency.
1: Timer 1 uses a divide by 4 of the crystal frequency.

T0M **Timer 0 Clock Select.** This bit controls the division of the system clock that drives Timer 0. Clearing this bit to
bit 3 0 maintains 8051 compatibility. This bit has no effect on instruction cycle timing.
0: Timer 0 uses a divide by 12 of the crystal frequency.
1: Timer 0 uses a divide by 4 of the crystal frequency.

MD2, MD1, MD0 Stretch MOVX Select 2-0. These bits select the time by which external MOVX cycles are to be stretched.
bits 2-0 This allows slower memory or peripherals to be accessed without using ports or manual software intervention. The for $\overline{RD}$ or $\overline{WR}$ strobe will be stretched by the specified interval, which will be transparent to the software except for the increased time to execute the MOVX instruction. All internal MOVX instructions on devices containing MOVX SRAM are performed at the 2 instruction cycle rate.

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (SYS CLKs)	$\overline{RD}$ or $\overline{WR}$ STROBE WIDTH (µs) AT 12MHz
0	0	0	0	2 Instruction Cycles	2	0.167
0	0	1	1	3 Instruction Cycles (default)	4	0.333
0	1	0	2	4 Instruction Cycles	8	0.667
0	1	1	3	5 Instruction Cycles	12	1.000
1	0	0	4	6 Instruction Cycles	16	1.333
1	0	1	5	7 Instruction Cycles	20	1.667
1	1	0	6	8 Instruction Cycles	24	2.000
1	1	1	7	9 Instruction Cycles	28	2.333

Memory Write Select (MWS)

	7	6	5	4	3	2	1	0	Reset Value
SFR $8F_H$	0	0	0	0	0	0	0	MXWS	00_H

MXWS **MOVX Write Select.** This allows writing to the internal Flash program memory.
bit 0 0: No writes are allowed to the internal Flash program memory.
1: Writing is allowed to the internal Flash program memory, unless PML (HCR0) or RSL (HCR0) are on.

Port 1 (P1)

	7	6	5	4	3	2	1	0	Reset Value
SFR 90_H	P1.7 $\overline{INT5}$/SCLK/SCK	P1.6 INT4/MISO/SDA	P1.5 $\overline{INT3}$/MOSI	P1.4 INT2/$\overline{SS}$	P1.3 TXD1	P1.2 RXD1	P1.1 T2EX	P1.0 T2	FF_H

P1.7-0 bits 7-0 **General-Purpose I/O Port 1.** This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 1 latch bit must contain a logic '1' before the pin can be used in its alternate function capacity. To use the alternate function, set the appropriate mode in P1DDRL (SFR AE_H), P1DDRH (SFR AF_H).

$\overline{INT5}$/SCLK/SCK bit 7
External Interrupt 5. A falling edge on this pin will cause an external interrupt 5 if enabled.
SPI Clock. The master clock for SPI data transfers.
Serial Clock. The serial clock for I^2C data transfers.

INT4/MISO/SDA bit 6
External Interrupt 4. A rising edge on this pin will cause an external interrupt 4 if enabled.
Master In Slave Out. For SPI data transfers, this pin receives data for the master and transmits data from the slave.
ISDA. For I^2C data transfers, this pin is the data line.

$\overline{INT3}$/MOSI bit 5
External Interrupt 3. A falling edge on this pin will cause an external interrupt 3 if enabled.
Master Out Slave In. For SPI data transfers, this pin transmits master data and receives slave data.

INT2/$\overline{SS}$ bit 4
External Interrupt 2. A rising edge on this pin will cause an external interrupt 2 if enabled.
Slave Select. During SPI operation, this pin provides the select signal for the slave device.

TXD1 bit 3 **Serial Port 1 Transmit.** This pin transmits the serial Port 1 data in serial port modes 1, 2, 3, and emits the synchronizing clock in serial port mode 0.

RXD1 bit 2 **Serial Port 1 Receive.** This pin receives the serial Port 1 data in serial port modes 1, 2, 3, and is a bidirectional data transfer pin in serial port mode 0.

T2EX bit 1 **Timer 2 Capture/Reload Trigger.** A 1 to 0 transition on this pin will cause the value in the T2 registers to be transferred into the capture registers if enabled by EXEN2 (T2CON.3, SFR $C8_H$). When in auto-reload mode, a 1 to 0 transition on this pin will reload the Timer 2 registers with the value in RCAP2L and RCAP2H if enabled by EXEN2 (T2CON.3, SFR $C8_H$).

T2 bit 0 **Time 2 External Input.** A 1 to 0 transition on this pin will cause Timer 2 to increment or decrement depending on the timer configuration.

External Interrupt Flag (EXIF)

	7	6	5	4	3	2	1	0	Reset Value
SFR 91_H	IE5	IE4	IE3	IE2	1	0	0	0	08_H

IE5 bit 7 **External Interrupt 5 Flag.** This bit will be set when a falling edge is detected on $\overline{INT5}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE4 bit 6 **External Interrupt 4 Flag.** This bit will be set when a rising edge is detected on INT4. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE3 bit 5 **External Interrupt 3 Flag.** This bit will be set when a falling edge is detected on $\overline{INT3}$. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

IE2 bit 4 **External Interrupt 2 Flag.** This bit will be set when a rising edge is detected on INT2. This bit must be cleared manually by software. Setting this bit in software will cause an interrupt if enabled.

Memory Page (MPAGE)

	7	6	5	4	3	2	1	0	Reset Value
SFR 92_H									00_H

MPAGE bits 7-0 The 8051 uses Port 2 for the upper 8 bits of the external data memory access by MOVX A@R_I and MOVX @R_I, A instructions. The MSC1211 uses register MPAGE instead of Port 2. To access external data memory using the MOVX A@R_I and MOVX @R_I, A instructions, the user should preload the upper byte of the address into MPAGE (versus preloading into P2 for the standard 8051).

Configuration Address Register (CADDR) (write only)

	7	6	5	4	3	2	1	0	Reset Value
SFR 93_H									00_H

CADDR **Configuration Address Register.** This register supplies the address for reading bytes in the 128 bytes of Flash Configuration
bits 7-0 Memory. WARNING: If this register is written to while executing from Flash Memory, the CDATA register will be incorrect.

Configuration Data Register (CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR 94_H									00_H

CDATA **Configuration Data Register.** This register will contain the data in the 128 bytes of Flash Configuration Memory
bits 7-0 that is located at the last written address in the CADDR register. This is a read-only register.

Memory Control (MCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR 95_H	**BPSEL**	**0**	**0**	**—**	**—**	**—**	**—**	**RAMMAP**	00_H

BPSEL **Breakpoint Address Selection**
bit 7 Write: Select one of two Breakpoint registers: 0 or 1.
0: Select breakpoint register 0.
1: Select breakpoint register 1.
Read: Provides the Breakpoint register that created the last interrupt: 0 or 1.

RAMMAP Memory Map 1kB extended SRAM.
bit 0 0: Address is: 0000_H-$03FF_H$ (default) (Data Memory)
1: Address is 8400_H-$87FF_H$ (Data and Program Memory)

Serial Port 0 Control (SCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 98_H	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00_H

SM0-2 Serial Port 0 Mode. These bits control the mode of serial Port 0. Modes 1, 2, and 3 have 1 start and 1 stop bit
bits 7-5 in addition to the 8 or 9 data bits.

MODE	SM0	SM1	SM2	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 p_{CLK}(1)
0	0	0	1	Synchronous	8 bits	4 p_{CLK}(1)
1(2)	0	1	x	Asynchronous	10 bits	Timer 1 or 2 Baud Rate Equation
2	1	0	0	Asynchronous	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
2	1	0	1	Asynchronous with Multiprocessor Communication	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
3(2)	1	1	0	Asynchronous	11 bits	Timer 1 or 2 Baud Rate Equation
3(2)	1	1	1	Asynchronous with Multiprocessor Communication	11 bits	Timer 1 or 2 Baud Rate Equation

NOTE: (1) p_{CLK} will be equal to t_{CLK}, except that p_{CLK} will stop for IDLE. (2) For modes 1 and 3, the selection of Timer 1 or 2 for baud rate is specified via the T2CON ($C8_H$) register.

REN_0 **Receive Enable.** This bit enables/disables the serial Port 0 received shift register.
bit 4 0: Serial Port 0 reception disabled.
1: Serial Port 0 received enabled (modes 1, 2, and 3). Initiate synchronous reception (mode 0).

TB8_0 **9th Transmission Bit State.** This bit defines the state of the 9th transmission bit in serial Port 0 modes 2 and 3.
bit 3

RB8_0 **9th Received Bit State.** This bit identifies the state of the 9th reception bit of received data in serial Port 0 modes
bit 2 2 and 3. In serial port mode 1, when SM2_0 = 0, RB8_0 is the state of the stop bit. RB8_0 is not used in mode 0.

TI_0 **Transmitter Interrupt Flag.** This bit indicates that data in the serial Port 0 buffer has been completely shifted
bit 1 out. In serial port mode 0, TI_0 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be manually cleared by software.

RI_0 bit 0 — **Receiver Interrupt Flag.** This bit indicates that a byte of data has been received in the serial Port 0 buffer. In serial port mode 0, RI_0 is set at the end of the 8th bit. In serial port mode 1, RI_0 is set after the last sample of the incoming stop bit subject to the state of SM2_0. In modes 2 and 3, RI_0 is set after the last sample of RB8_0. This bit must be manually cleared by software.

Serial Data Buffer 0 (SBUF0)

	7	6	5	4	3	2	1	0	Reset Value
SFR 99_H									00_H

SBUF0 bits 7-0 — **Serial Data Buffer 0.** Data for Serial Port 0 is read from or written to this location. The serial transmit and receive buffers are separate registers, but both are addressed at this location.

SPI Control (SPICON). Any change resets the SPI interface, counters, and pointers. PDCON controls which is enabled.

	7	6	5	4	3	2	1	0	Reset Value
SFR $9A_H$	SCLK2	SCLK1	SCLK0	FIFO	ORDER	MSTR	CPHA	CPOL	00_H

SCLK bits 7-5 — **SCK Selection.** Selection of t_{CLK} divider for generation of SCK in Master mode.

SCLK2	SCLK1	SCLK0	SCK PERIOD
0	0	0	$t_{CLK}/2$
0	0	1	$t_{CLK}/4$
0	1	0	$t_{CLK}/8$
0	1	1	$t_{CLK}/16$
1	0	0	$t_{CLK}/32$
1	0	1	$t_{CLK}/64$
1	1	0	$t_{CLK}/128$
1	1	1	$t_{CLK}/256$

FIFO bit 4 — **Enable FIFO in on-chip indirect memory.**
0: Both transmit and receive are double buffers
1: Circular FIFO used for transmit and receive bytes

ORDER bit 3 — **Set Bit Order for Transmit and Receive.**
0: Most Significant Bits First
1: Least Significant Bits First

MSTR bit 2 — **SPI Master Mode.**
0: Slave Mode
1: Master Mode

CPHA bit 1 — **Serial Clock Phase Control.**
0: Valid data starting from half SCK period before the first edge of SCK
1: Valid data starting from the first edge of SCK

CPOL bit 0 — **Serial Clock Polarity.**
0: SCK idle at logic LOW
1: SCK idle at logic HIGH

I^2C Control Register (I2CCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9A_H$	START	STOP	ACK	0	FAST	MSTR	SCLS	FILEN	00_H

START bit 7 — **Start Condition (Master mode).**
Read: Current status of start condition or repeated start condition.
Write: When operating as a master, a start condition is transmitted when the START bit is set to 1. During a data transfer, if the START bit is set, a repeated start is transmitted after the current data transfer is complete. If no transfer is in progress when the START and STOP bits are set simultaneously, a START will be followed by a STOP.

STOP **Stop Condition (Master mode).**
bit 6 Read: Current status of stop condition.
Write: Setting STOP to logic 1 causes a stop condition to be transmitted. When a stop condition is received, hardware clears STOP to logic 0. If both START and STOP are set during a transfer, a stop condition is transmitted followed by a start condition.

ACK **Acknowledge.** Defines the ACK/NACK generation from the master/slave receiver during the acknowledge cycle.
bit 5 0: A NACK (high level on SDA) is returned during the acknowledge cycle.
1: An ACK (low level on SDA) is returned during the ackowledge cycle.

0 **Always set this value to zero.**
bit 4

FAST **Fast Mode Enable.**
bit 3 0: Standard Mode (100kHz)
1: Fast Mode (400kHz)

MSTR **SPI Master Mode.**
bit 2 0: Slave Mode
1: Master Mode

SCLS **Clock Stretch.**
bit 1 0: No effect
1: Release the clock line. For the slave mode, the clock is stretched for each data transfer. This bit releases the clock. This bit can be set during a transfer to eliminate any clock stretching.

FILEN **Filter Enable.** 50ns glitch filter.
bit 0 0: Filter disabled
1: Filter enabled

SPI Data Register (SPIDATA) / I²C Data Register (I2CDATA)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9B_H$									00_H

SPIDATA **SPI Data Register.** Data for SPI is read from or written to this location. The SPI transmit and receive buffers
bits 7-0 are separate registers, but both are addressed at this location.

I2CDATA **I2C Data Register.** Data for I²C is read from or written to this location. The I²C transmit and receive buffers
bits 7-0 are separate registers, but both are addressed at this location.

SPI Receive Control Register (SPIRCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9C_H$	RXCNT7 RXFLUSH	RXCNT6	RXCNT5	RXCNT4	RXCNT3	RXCNT2 RXIRQ2	RXCNT1 RXIRQ1	RXCNT0 RXIRQ0	00_H

RXCNT **Receive Counter.** Read only bits which read the number of bytes in the receive buffer (0 to 128).
bits 7-0

RXFLUSH **Flush Receive FIFO.** Write only.
bit 7 0: No Action
1: SPI Receive Buffer Set to Empty

RXIRQ **Read IRQ Level.** Write only.
bits 2-0

000	Generate IRQ when Receive Count = 1 or more.
001	Generate IRQ when Receive Count = 2 or more.
010	Generate IRQ when Receive Count = 4 or more.
011	Generate IRQ when Receive Count = 8 or more.
100	Generate IRQ when Receive Count = 16 or more.
101	Generate IRQ when Receive Count = 32 or more.
110	Generate IRQ when Receive Count = 64 or more.
111	Generate IRQ when Receive Count = 128 or more.

I²C GM Register (I2CGM)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9C_H$	GCMEN								00_H

GCMEN **General Call/Multiple Master Enable.** Write only.
bit 7 Slave mode: 0 = General call ignored, 1 = General call will be detected
Master mode: 0 = Single master, 1 = Multiple master mode

SPI Transmit Control Register (SPITCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9D_H$	TXCNT7 TXFLUSH	TXCNT6	TXCNT5 CLK_EN	TXCNT4 DRV_DLY	TXCNT3 DRV_EN	TXCNT2 TXIRQ2	TXCNT1 TXIRQ1	TXCNT0 TXIRQ0	00_H

TXCNT **Transmit Counter.** Read only bits which read the number of bytes in the transmit buffer (0 to 128).
bits 7-0

TXFLUSH **Flush Transmit FIFO.** This bit is write only. When set, the SPI transmit pointer is set equal to the FIFO Output pointer. This bit is 0 for a read operation.
bit 7

CLK_EN **SCLK Driver Enable.**
bit 5 0: Disable SCLK Driver (Master Mode)
1: Enable SCLK Driver (Master Mode)

DRV_DLY **Drive Delay (refer to DRV_EN bit)**.
bit 4 0: Drive Output Immediately
1: Drive Output After Current Byte Transfer

DRV_EN **Drive Enable**.
bit 3

DRV_DLY	DRV_EN	MOSI or MISO OUTPUT CONTROL
0	0	Tristate Immediately
0	1	Drive Immediately
1	0	Tristate After the Current Byte Transfer
1	1	Drive After the Current Byte Transfer

TXIRQ **Transmit IRQ Level.** Write only bits.
bits 2-0

000	Generate IRQ when Transmit count = 1 or less.
001	Generate IRQ when Transmit count = 2 or less.
010	Generate IRQ when Transmit count = 4 or less.
011	Generate IRQ when Transmit count = 8 or less.
100	Generate IRQ when Transmit count = 16 or less.
101	Generate IRQ when Transmit count = 32 or less.
110	Generate IRQ when Transmit count = 64 or less.
111	Generate IRQ when Transmit count = 128 or less.

I²C Status Register (I2CSTAT)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9D_H$	STAT7 SCKD7/SAE	STAT6 SCKD6/SA6	STAT5 SCKD5/SA5	STAT4 SCKD4/SA4	STAT3 SCKD3/SA3	0 SCKD2/SA2	0 SCKD1/SA1	0 SCKD0/SA0	00_H

STAT7-3 **Status Code.** Read only.
bit 7-3

SCKD7-0 **Serial Clock Divisor.** Write only, master mode.
bit 7-0 The frequency of the SCL line is set equal to Sysclk/[2 • (SCKD + 1)]. The minimum value for SCKD is 3.

SAE **Slave Address Enable.** Write only, slave mode.
bit 7 In slave mode, if this is set, address recognition is enabled.

SA6-0 **Slave Address.** Write only, slave mode.
bit 6-0 The address of this device is used in slave mode for address recognition.

SPI Buffer Start Address (SPISTART)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9E_H$	1								80_H

SPISTART bits 6-0 — **SPI FIFO Start Address.** Write only. This specifies the start address of the SPI data buffer. This is a circular FIFO that is located in the 128 bytes of indirect RAM. The FIFO starts at this address and ends at the address specified in SPIEND. Must be less than SPIEND. Writing clears SPI transmit and receive counters.

SPITP bits 6-0 — **SPI Transmit Pointer**. Read Only. This is the FIFO address for SPI transmissions. This is where the next byte will be written into the SPI FIFO buffer. This pointer increments after each write to the SPI Data register unless that would make it equal to the SPI Receive pointer.

SPI Buffer End Address (SPIEND)

	7	6	5	4	3	2	1	0	Reset Value
SFR $9F_H$	1								80_H

SPIEND bits 6-0 — **SPI FIFO End Address.** Write only. This specifies the end address of the SPI data FIFO. This is a circular buffer that is located in the 128 bytes of indirect RAM. The buffer starts at SPISTART and ends at this address.

SPIRP bits 6-0 — **SPI Receive Pointer**. Read Only. This is the FIFO address for SPI received bytes. This is the location of the next byte to be read from the SPI FIFO. This increments with each read from the SPI Data register until the RxCNT is zero.

Port 2 (P2)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A0_H$									FF_H

P2 bits 7-0 — **Port 2.** This port functions as an address bus during external memory access, and as a general-purpose I/O port. During external memory cycles, this port will contain the MSB of the address. Whether Port 2 is used as general-purpose I/O or for external memory access is determined by the Flash Configuration Register (HCR1.0).

PWM Control (PWMCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A1_H$	—	—	PPOL	PWMSEL	SPDSEL	TPCNTL.2	TPCNTL.1	TPCNTL.0	00_H

PPOL bit 5 — **Period Polarity.** Specifies the starting level of the PWM pulse.
0: ON Period. PWM Duty register programs the ON period.
1: OFF Period. PWM Duty register programs the OFF period.

PWMSEL bit 4 — **PWM Register Select.** Select which 16-bit register is accessed by PWMLOW/PWMHIGH**.**
0: Period (must be 0 for TONE mode)
1: Duty

SPDSEL bit 3 — **Speed Select.**
0: 1MHz (the USEC Clock)
1: SYSCLK

TPCNTL bits 2-0 — **Tone Generator/Pulse Width Modulation Control.**

TPCNTL.2	TPCNTL.1	TPCNTL.0	MODE
0	0	0	Disable (default)
0	0	1	PWM
0	1	1	TONE—Square
1	1	1	TONE—Staircase

Tone Low (TONELOW) /PWM Low (PWMLOW)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A2_H$	PWM7 TDIV7	PWM6 TDIV6	PWM5 TDIV5	PWM4 TDIV4	PWM3 TDIV3	PWM2 TDIV2	PWM1 TDIV1	PWM0 TDIV0	00_H

PWMLOW bits 7-0 — **Pulse Width Modulator Low Bits.** These 8 bits are the least significant 8 bits of the PWM register.

TDIV7-0 bits 7-0 — **Tone Divisor.** The low order bits that define the half-time period. For staircase mode the output is high impedance for the last 1/4 of this period.

Tone High (TONEHI)/PWM High (PWMHI)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A3_H$	PWM15 TDIV15	PWM14 TDIV14	PWM13 TDIV13	PWM12 TDIV12	PWM11 TDIV11	PWM10 TDIV10	PWM9 TDIV9	PWM8 TDIV8	00_H

PWMHI **Pulse Width Modulator High Bits.** These 8 bits are the high order bits of the PWM register.
bits 7-0

TDIV15-8 **Tone Divisor.** The high order bits that define the half time period. For staircase mode the output is high
bits 7-0 impedance for the last 1/4 of this period.

Pending Auxiliary Interrupt (PAI)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A5_H$	0	0	0	0	PAI3	PAI2	PAI1	PAI0	00_H

PAI **Pending Auxiliary Interrupt Register.** The results of this register can be used as an index to vector to the appropriate
bits 3-0 interrupt routine. All of these interrupts vector through address 0033_H.

PAI3	PAI2	PAI1	PAI0	AUXILIARY INTERRUPT STATUS
0	0	0	0	No Pending Auxiliary IRQ
0	0	0	1	Digital Low Voltage IRQ Pending
0	0	1	0	Analog Low Voltage IRQ Pending
0	0	1	1	SPI Receive IRQ Pending. I^2C Status Pending.
0	1	0	0	SPI Transmit IRQ Pending
0	1	0	1	One Millisecond System Timer IRQ Pending
0	1	1	0	Analog to Digital Conversion IRQ Pending
0	1	1	1	Accumulator IRQ Pending
1	0	0	0	One Second System Timer IRQ Pending

Auxiliary Interrupt Enable (AIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A6_H$	ESEC	ESUM	EADC	EMSEC	ESPIT	ESPIR/EI2C	EALV	EDLVB	00_H

Interrupts are enabled by EICON.4 (SFR $D8_H$). The other interrupts are controlled by the IE and EIE registers.

ESEC **Enable Seconds Timer Interrupt (lowest priority auxialiary interrupt).**
bit 7 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **Seconds Timer Interrupt** before masking.

ESUM **Enable Summation Interrupt.**
bit 6 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **Summation Interrupt** before masking.

EADC **Enable ADC Interrupt.**
bit 5 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **ADC Interrupt** before masking.

EMSEC **Enable Millisecond System Timer Interrupt.**
bit 4 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **Millisecond System Timer Interrupt** before masking.

ESPIT **Enable SPI Transmit Interrupt.**
bit 3 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **SPI Transmit Interrupt** before masking.

ESPIR/EI2C **Enable SPI Receive Interrupt. Enable I^2C Status Interrupt**.
bit 2 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **SPI Receive Interrupt** or **I2C Status Interrupt** before masking.

EALV **Enable Analog Low Voltage Interrupt.**
bit 1 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **Analog Low Voltage Interrupt** before masking.

EDLVB **Enable Digital Low Voltage or Breakpoint Interrupt (highest priority auxiliary interrupt).**
bit 0 Write: Set mask bit for this interrupt 0 = masked, 1 = enabled.
Read: Current value of **Digital Low Voltage or Breakpoint Interrupt** before masking.

Auxiliary Interrupt Status Register (AISTAT)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A7_H$	SEC	SUM	ADC	MSEC	SPIT	SPIR/I2CSI	ALVD	DLVD	00_H

SEC **Second System Timer Interrupt Status Flag (lowest priority AI).**
bit 7 0: SEC interrupt inactive or masked.
1: SEC Interrupt active.

SUM **Summation Register Interrupt Status Flag.**
bit 6 0: SUM interrupt inactive or masked (if active, it is set inactive by reading the lowest byte of the Summation register).
1: SUM interrupt active.

ADC **ADC Interrupt Status Flag.**
bit 5 0: ADC interrupt inactive or masked (If active, it is set inactive by reading the lowest byte of the Data Output Register).
1: ADC interrupt active (If active no new data will be written to the Data Output Register).

MSEC **Millisecond System Timer Interrupt Status Flag.**
bit 4 0: MSEC interrupt inactive or masked.
1: MSEC interrupt active.

SPIT **SPI Transmit Interrupt Status Flag.**
bit 3 0: SPI transmit interrupt inactive or masked.
1: SPI transmit interrupt active.

SPIR/I2CSI **SPI Receive Interrupt Status Flag. I^2C Status Interrupt**.
bit 2 0: SPI receive or I2CSI interrupt inactive or masked.
1: SPI receive or I2CSI interrupt active.

ALVD **Analog Low Voltage Detect Interrupt Status Flag.**
bit 1 0: ALVD interrupt inactive or masked.
1: ALVD interrupt active.

DLVD **Digital Low Voltage Detect or Breakpoint Interrupt Status Flag (highest priority AI).**
bit 0 0: DLVD interrupt inactive or masked.
1: DLVD interrupt active.

Interrupt Enable (IE)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A8_H$	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00_H

EA **Global Interrupt Enable.** This bit controls the global masking of all interrupts except those in AIE (SFR $A6_H$).
bit 7 0: Disable interrupt sources. This bit overrides individual interrupt mask settings for this register.
1: Enable all individual interrupt masks. Individual interrupts in this register will occur if enabled.

ES1 **Enable Serial Port 1 Interrupt.** This bit controls the masking of the serial Port 1 interrupt.
bit 6 0: Disable all serial Port 1 interrupts.
1: Enable interrupt requests generated by the RI_1 (SCON1.0, SFR $C0_H$) or TI_1 (SCON1.1, SFR $C0_H$) flags.

ET2 **Enable Timer 2 Interrupt.** This bit controls the masking of the Timer 2 interrupt.
bit 5 0: Disable all Timer 2 interrupts.
1: Enable interrupt requests generated by the TF2 flag (T2CON.7, SFR $C8_H$).

ES0 **Enable Serial port 0 interrupt.** This bit controls the masking of the serial Port 0 interrupt.
bit 4 0: Disable all serial Port 0 interrupts.
1: Enable interrupt requests generated by the RI_0 (SCON0.0, SFR 98_H) or TI_0 (SCON0.1, SFR 98_H) flags.

ET1 **Enable Timer 1 Interrupt.** This bit controls the masking of the Timer 1 interrupt.
bit 3 0: Disable Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag (TCON.7, SFR 88_H).

EX1 **Enable External Interrupt 1.** This bit controls the masking of external interrupt 1.
bit 2 0: Disable external interrupt 1.
1: Enable interrupt requests generated by the $\overline{INT1}$ pin.

ET0 **Enable Timer 0 Interrupt.** This bit controls the masking of the Timer 0 interrupt.
bit 1 0: Disable all Timer 0 interrupts.
1: Enable interrupt requests generated by the TF0 flag (TCON.5, SFR 88_H).

EX0 **Enable External Interrupt 0.** This bit controls the masking of external interrupt 0.
bit 0 0: Disable external interrupt 0.
1: Enable interrupt requests generated by the $\overline{INT0}$ pin.

Breakpoint Control (BPCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $A9_H$	BP	0	0	0	0	0	PMSEL	EBP	00_H

Writing to register sets the breakpoint condition specified by MCON, BPL, and BPH.

BP **Breakpoint Interrupt.** This bit indicates that a break condition has been recognized by a hardware breakpoint register(s).
bit 7 Read: Status of Breakpoint Interrupt. Will indicate a breakpoint match for any of the breakpoint registers.
Write: 0: No effect.
1: Clear Breakpoint 1 for breakpoint register selected by MCON (SFR 95_H).

PMSEL **Program Memory Select.** Write this bit to select memory for address breakpoints of register selected in
bit 1 MCON (SFR 95_H).
0: Break on address in data memory.
1: Break on address in program memory.

EBP **Enable Breakpoint.** This bit enables this breakpoint register. Address of breakpoint register selected by
bit 0 MCON (SFR 95_H).
0: Breakpoint disabled.
1: Breakpoint enabled.

Breakpoint Low (BPL) Address for BP Register Selected in MCON (95_H)

	7	6	5	4	3	2	1	0	Reset Value
SFR AA_H	BPL.7	BPL.6	BPL.5	BPL.4	BPL.3	BPL.2	BPL.1	BPL.0	00_H

BPL.7-0 **Breakpoint Low Address**. The low 8 bits of the 16 bit breakpoint address.
bits 7-0

Breakpoint High Address (BPH) Address for BP Register Selected in MCON (95_H)

	7	6	5	4	3	2	1	0	Reset Value
SFR AB_H	BPH.7	BPH.6	BPH.5	BPH.4	BPH.3	BPH.2	BPH.1	BPH.0	00_H

BPH.7-0 **Breakpoint High Address.** The high 8 bits of the 16 bit breakpoint address.
bits 7-0

Port 0 Data Direction Low Register (P0DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR AC_H	P03H	P03L	P02H	P02L	P01H	P01L	P00H	P00L	00_H

P0.3 **Port 0 bit 3 control.**

bits 7-6

P03H	P03L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.2 **Port 0 bit 2 control.**

bits 5-4

P02H	P02L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.1 **Port 0 bit 1 control.**

bits 3-2

P01H	P01L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.0 **Port 0 bit 0 control.**

bits 1-0

P00H	P00L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 0 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

Port 0 Data Direction High Register (P0DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR AD_H	P07H	P07L	P06H	P06L	P05H	P05L	P04H	P04L	00_H

P0.7 **Port 0 bit 7 control.**

bits 7-6

P07H	P07L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.6 **Port 0 bit 6 control.**

bits 5-4

P06H	P06L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.5 **Port 0 bit 5 control.**

bits 3-2

P05H	P05L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P0.4 **Port 0 bit 4 control.**

bits 1-0

P04H	P04L	
0	0	Standard 8051(Pull-Up)
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

T O N

Port 1 Data Direction Low Register (P1DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR AE_H	P13H	P13L	P12H	P12L	P11H	P11L	P10H	P10L	00_H

P1.3 **Port 1 bit 3 control.**

bits 7-6

P13H	P13L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.2 **Port 1 bit 2 control.**

bits 5-4

P12H	P12L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.1 **Port 1 bit 1 control.**

bits 3-2

P11H	P11L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.0 **Port 1 bit 0 control.**

bits 1-0

P10H	P10L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 1 Data Direction High Register (P1DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR AF_H	P17H	P17L	P16H	P16L	P15H	P15L	P14H	P14L	00_H

P1.7 **Port 1 bit 7 control.**

bits 7-6

P17H	P17L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.6 **Port 1 bit 6 control.**

bits 5-4

P16H	P16L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.5 **Port 1 bit 5 control.**

bits 3-2

P15H	P15L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P1.4 **Port 1 bit 4 control.**

bits 1-0

P14H	P14L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 (P3)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B0_H$	P3.7 $\overline{RD}$	P3.6 $\overline{WR}$	P3.5 T1	P3.4 T0	P3.3 $\overline{INT1}$	P3.2 $\overline{INT0}$	P3.1 TXD0	P3.0 RXD0	FF_H

P3.7-0 bits 7-0 **General-Purpose I/O Port 3**. This register functions as a general-purpose I/O port. In addition, all the pins have an alternative function listed below. Each of the functions is controlled by several other SFRs. The associated Port 3 latch bit must contain a logic '1' before the pin can be used in its alternate function capacity.

$\overline{RD}$ bit 7 **External Data Memory Read Strobe.** This pin provides an active low read strobe to an external memory device. If Port 0 or Port 2 is selected for external memory in the HCR1 register, this function will be enabled even if a 1 is not written to this latch bit. When external memory is selected, the settings of P3DRRH are ignored.

$\overline{WR}$ bit 6 **External Data Memory Write Strobe.** This pin provides an active low write strobe to an external memory device. If Port 0 or Port 2 is selected for external memory in the HCR1 register, this function will be enabled even if a 1 is not written to this latch bit. When external memory is selected, the settings of P3DRRH are ignored.

T1 bit 5 **Timer/Counter 1 External Input.** A 1 to 0 transition on this pin will increment Timer 1.

T0 bit 4 **Timer/Counter 0 External Input.** A 1 to 0 transition on this pin will increment Timer 0.

$\overline{INT1}$ bit 3 **External Interrupt 1.** A falling edge/low level on this pin will cause an external interrupt 1 if enabled.

$\overline{INT0}$ bit 2 **External Interrupt 0.** A falling edge/low level on this pin will cause an external interrupt 0 if enabled.

TXD0 bit 1 **Serial Port 0 Transmit.** This pin transmits the serial Port 0 data in serial port modes 1, 2, 3, and emits the synchronizing clock in serial port mode 0.

RXD0 bit 0 **Serial Port 0 Receive.** This pin receives the serial Port 0 data in serial port modes 1, 2, 3, and is a bidirectional data transfer pin in serial port mode 0.

Port 2 Data Direction Low Register (P2DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B1_H$	P23H	P23L	P22H	P22L	P21H	P21L	P20H	P20L	00_H

P2.3 bits 7-6 **Port 2 bit 3 control.**

P23H	P23L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.2 bits 5-4 **Port 2 bit 2 control.**

P22H	P22L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.1 bits 3-2 **Port 2 bit 1 control.**

P21H	P21L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.0 bits 1-0 **Port 2 bit 0 control.**

P20H	P20L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 2 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

Port 2 Data Direction High Register (P2DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B2_H$	P27H	P27L	P26H	P26L	P25H	P25L	P24H	P24L	00_H

P2.7 **Port 2 bit 7 control.**

bits 7-6

P27H	P27L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.6 **Port 2 bit 6 control.**

bits 5-4

P26H	P26L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.5 **Port 2 bit 5 control.**

bits 3-2

P25H	P25L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P2.4 **Port 2 bit 4 control.**

bits 1-0

P24H	P24L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 2 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

Port 3 Data Direction Low Register (P3DDRL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B3_H$	P33H	P33L	P32H	P32L	P31H	P31L	P30H	P30L	00_H

P3.3 **Port 3 bit 3 control.**

bits 7-6

P33H	P33L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.2 **Port 3 bit 2 control.**

bits 5-4

P32H	P32L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.1 **Port 3 bit 1 control.**

bits 3-2

P31H	P31L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.0 **Port 3 bit 0 control.**

bits 1-0

P30H	P30L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

Port 3 Data Direction High Register (P3DDRH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B4_H$	P37H	P37L	P36H	P36L	P35H	P35L	P34H	P34L	00_H

P3.7 **Port 3 bit 7 control.**

bits 7-6

P37H	P37L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.7 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.6 **Port 3 bit 6 control.**

bits 5-4

P36H	P36L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

NOTE: Port 3.6 also controlled by $\overline{EA}$ and Memory Access Control HCR1.1.

P3.5 **Port 3 bit 5 control.**

bits 3-2

P35H	P35L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

P3.4 **Port 3 bit 4 control.**

bits 1-0

P34H	P34L	
0	0	Standard 8051
0	1	CMOS Output
1	0	Open Drain Output
1	1	Input

DAC Low Byte (DACL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B5_H$									00_H

DACL7-0 **Least Significant Bit Register for DAC0-3 and DAC Control (0 and 2).**

bits 7-0

DAC High Byte (DACH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B6_H$									00_H

DACH7-0 **Most Significant Byte Register for DAC0-3 and DAC Control (1 and 3).**

bits 7-0

DAC Select Register (DACSEL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B7_H$	DSEL7	DSEL6	DSEL5	DSEL4	DSEL3	DSEL2	DSEL1	DSEL0	00_H

DSEL7-0 **DAC and DAC Control Select.** The DACSEL register selects which DAC output register or which DAC control register is accessed by the DACL and DACH registers.

bits 7-0

DACSEL ($B7_H$)	DACH (B6H)	DACL (B5H)	RESET VALUE
00_H	DAC0 (high)	DAC0 (low)	0000_H
01_H	DAC1 (high)	DAC1 (low)	0000_H
02_H	DAC2 (high)	DAC2 (low)	0000_H
03_H	DAC3 (high)	DAC3 (low)	0000_H
04_H	DACCON1	DACCON0	6363_H
05_H	DACCON3	DACCON2	0303_H
06_H	—	LOADCON	$--00_H$
07_H	—	—	—

DAC0 Control Register (DACCON0)

DACSEL = 04_H	7	6	5	4	3	2	1	0	Reset Value
SFR $B5_H$	COR0	EOD0	IDAC0DIS	0	0	SELREF0	DOM0_1	DOM0_0	63_H

COR0 **Current Over Range on DAC0**

bit 7 Write: 0 = Clear to release from high-impedance state back to normal mode unless an over-range exists.
1 = NOP

Read: 0 = No current over range for DAC0.
1 = COR0 signal after 3ms filter (EOD0 = 1) or raw signal (EOD0 = 0).

EOD0 **Enable Over-Current Detection**

bit 6 0 = Disable over-current detection.
1 = Enable over-current detection (default).

IDAC0DIS **IDAC0 Disable (for DOM0 = 00)**

bit 5 0 = IDAC on mode for DAC0.
1 = IDAC off mode for DAC0 (default).

Not Used

bits 4-3

SELREF0 **Select the Reference Voltage for DAC0 Voltage Reference.**

bit 2 0 = DAC0 V_{REF} = AV_{DD} (default).
1 = DAC0 V_{REF} = internal V_{REF}.

DOM0_1-0 **DAC Output Mode DAC0.**

bits 1-0

DOM0	OUTPUT MODE FOR DAC0
00	Normal VDAC output, IDAC controlled by IDAC0DIS bit.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC1 Control Register (DACCON1)

DACSEL = 04_H	7	6	5	4	3	2	1	0	Reset Value
SFR $B6_H$	COR1	EOD1	IDAC1DIS	0	0	SELREF1	DOM1_1	DOM1_0	63_H

COR1 **Current Over Range on DAC1**

bit 7 Write: 0 = Clear to release from high-impedance state back to normal mode unless an over-range exists.
1 = NOP

Read: 0 = No current over range for DAC1.
1 = COR1 signal after 3ms filter (EOD1 = 1) or raw signal (EOD1 = 0).

EOD1 **Enable Over-Current Detection**

bit 6 0 = Disable over-current detection.
1 = Enable over-current detection (default).

IDAC1DIS **IDAC1 Disable (for DOM1 = 00)**

bit 5 0 = IDAC on mode for DAC1.
1 = IDAC off mode for DAC1 (default).

Not Used

bits 4-3

SELREF1 **Select the Reference Voltage for DAC1 Voltage Reference.**

bit 2 0 = DAC1 V_{REF} = AV_{DD} (default).
1 = DAC1 V_{REF} = internal V_{REF}.

DOM1_1-0 **DAC Output Mode DAC0.**

bits 1-0

DOM1	OUTPUT MODE FOR DAC1
00	Normal VDAC output, IDAC controlled by IDAC1DIS bit.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC2 Control Register (DACCON2)

DACSEL = 05_H	7	6	5	4	3	2	1	0	Reset Value
SFR $B5_H$	0	0	0	0	0	SELREF2	DOM2_1	DOM2_0	03_H

SELREF2 **Select the Reference Voltage for DAC2 Voltage Reference.**

bit 2 0 = DAC2 V_{REF} = AV_{DD} (default).
1 = DAC2 V_{REF} = internal V_{REF}.

DOM2_1-0 **DAC Output Mode DAC2.**

bits 1-0

DOM2	OUTPUT MODE FOR DAC2
00	Normal VDAC output.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC3 Control Register (DACCON3)

DACSEL = 05_H	7	6	5	4	3	2	1	0	Reset Value
SFR $B6_H$	0	0	0	0	0	SELREF3	DOM3_1	DOM3_0	03_H

SELREF3 **Select the Reference Voltage for DAC3 Voltage Reference.**

bit 2 0 = DAC2 V_{REF} = AV_{DD} (default).
1 = DAC2 V_{REF} = internal V_{REF}.

DOM3_1-0 **DAC Output Mode DAC3.**

bits 1-0

DOM2	OUTPUT MODE FOR DAC2
00	Normal VDAC output.
01	Power-Down mode—VDAC output off 1kΩ to AGND, IDAC off.
10	Power-Down mode—VDAC output off 100kΩ to AGND, IDAC off.
11	Power-Down mode—VDAC output off high impedance, IDAC off (default).

DAC Load Control Register (LOADCON)

DACSEL = 06_H	7	6	5	4	3	2	1	0	Reset Value
SFR $B5_H$	D3LOAD1	D3LOAD0	D2LOAD1	D2LOAD0	D1LOAD1	D1LOAD0	D0LOAD1	D0LOAD0	00_H

D3LOAD1-0 **DAC Load Options.**

bit 7-6

D2LOAD1-0

bit 5-4

D1LOAD1-0

bit 3-2

D0LOAD1-0

bit 1-0

DxLOAD	OUTPUT MODE FOR DACx
00	Direct load: write to DACxL directly loads the DAC buffer and the DAC output (write to DACxH does not load DAC output).
01	Delay load: the values last written to DACxL/DACxH will be transferred to the DAC output on the next MSEC timer tick.
10	Delay load: the values last written to DACxL/DACxH will be transferred to the DAC output on the next HMSEC timer tick.
11	Sync load: the values contained in the DACxL/DACxH registers will be transferred to the DAC output immediately after 11_B is written to this register.

Interrupt Priority (IP)

	7	6	5	4	3	2	1	0	Reset Value
SFR $B8_H$	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	80_H

PS1 bit 6 — **Serial Port 1 Interrupt.** This bit controls the priority of the serial Port 1 interrupt.
0 = Serial Port 1 priority is determined by the natural priority order.
1 = Serial Port 1 is a high priority interrupt.

PT2 bit 5 — **Timer 2 Interrupt.** This bit controls the priority of the Timer 2 interrupt.
0 = Timer 2 priority is determined by the natural priority order.
1 = Timer 2 priority is a high priority interrupt.

PS0 bit 4 — **Serial Port 0 Interrupt.** This bit controls the priority of the serial Port 0 interrupt.
0 = Serial Port 0 priority is determined by the natural priority order.
1 = Serial Port 0 is a high priority interrupt.

PT1 bit 3 — **Timer 1 Interrupt.** This bit controls the priority of the Timer 1 interrupt.
0 = Timer 1 priority is determined by the natural priority order.
1 = Timer 1 priority is a high priority interrupt.

PX1 bit 2 — **External Interrupt 1.** This bit controls the priority of external interrupt 1.
0 = External interrupt 1 priority is determined by the natural priority order.
1 = External interrupt 1 is a high priority interrupt.

PT0 bit 1 — **Timer 0 Interrupt.** This bit controls the priority of the Timer 0 interrupt.
0 = Timer 0 priority is determined by the natural priority order.
1 = Timer 0 priority is a high priority interrupt.

PX0 bit 0 — **External Interrupt 0.** This bit controls the priority of external interrupt 0.
0 = External interrupt 0 priority is determined by the natural priority order.
1 = External interrupt 0 is a high priority interrupt.

Serial Port 1 Control (SCON1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $C0_H$	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00_H

SM0-2 bits 7-5 — Serial Port 1 Mode. These bits control the mode of serial Port 1. Modes 1, 2, and 3 have 1 start and 1 stop bit in addition to the 8 or 9 data bits.

MODE	SM0	SM1	SM2	FUNCTION	LENGTH	PERIOD
0	0	0	0	Synchronous	8 bits	12 p_{CLK}(1)
0	0	0	1	Synchronous	8 bits	4 p_{CLK}(1)
1(2)	0	1	x	Asynchronous	10 bits	Timer 1 or 2 Baud Rate Equation
2	1	0	0	Asynchronous	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
2	1	0	1	Asynchronous with Multiprocessor Communication	11 bits	64 p_{CLK}(1) (SMOD = 0) 32 p_{CLK}(1) (SMOD = 1)
3(2)	1	1	0	Asynchronous	11 bits	Timer 1 or 2 Baud Rate Equation
3(2)	1	1	1	Asynchronous with Multiprocessor Communication	11 bits	Timer 1 or 2 Baud Rate Equation

NOTE: (1) p_{CLK} will be equal to t_{CLK}, except that p_{CLK} will stop for IDLE. (2) For modes 1 and 3, the selection of Timer 1 or 2 for baud rate is specified via the SCON register.

REN_1 bit 4 — **Receive Enable.** This bit enables/disables the serial Port 1 received shift register.
0 = Serial Port 1 reception disabled.
1 = Serial Port 1 received enabled (modes 1, 2, and 3). Initiate synchronous reception (mode 0).

TB8_1 bit 3 — **9th Transmission Bit State.** This bit defines the state of the 9th transmission bit in serial Port 1 modes 2 and 3.

RB8_1 bit 2 — **9th Received Bit State.** This bit identifies the state of the 9th reception bit of received data in serial Port 1 modes 2 and 3. In serial port mode 1, when SM2_1 = 0, RB8_1 is the state of the stop bit. RB8_1 is not used in mode 0.

TI_1 bit 1 — **Transmitter Interrupt Flag.** This bit indicates that data in the serial Port 1 buffer has been completely shifted out. In serial port mode 0, TI_1 is set at the end of the 8th data bit. In all other modes, this bit is set at the end of the last data bit. This bit must be cleared by software to transmit the next byte.

RI_1 **Receiver Interrupt Flag.** This bit indicates that a byte of data has been received in the serial Port 1 buffer. In
bit 0 serial port mode 0, RI_1 is set at the end of the 8th bit. In serial port mode 1, RI_1 is set after the last sample of the incoming stop bit subject to the state of SM2_1. In modes 2 and 3, RI_1 is set after the last sample of RB8_1. This bit must be cleared by software to receive the next byte.

Serial Data Buffer 1 (SBUF1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $C1_H$									00_H

SBUF1.7-0 **Serial Data Buffer 1.** Data for serial Port 1 is read from or written to this location. The serial transmit and receive
bits 7-0 buffers are separate registers, but both are addressed at this location.

Enable Wake Up (EWU) Waking Up from IDLE Mode

	7	6	5	4	3	2	1	0	Reset Value
SFR $C6_H$	—	—	—	—	—	EWUWDT	EWUEX1	EWUEX0	00_H

Auxiliary interrupts will wake up from IDLE. They are enabled with EAI (EICON.5).

EWUWDT **Enable Wake Up Watchdog Timer.** Wake using watchdog timer interrupt.
bit 2 0 = Don't wake up on watchdog timer interrupt.
1 = Wake up on watchdog timer interrupt.

EWUEX1 **Enable Wake Up External 1.** Wake using external interrupt source 1.
bit 1 0 = Don't wake up on external interrupt source 1.
1 = Wake up on external interrupt source 1.

EWUEX0 **Enable Wake Up External 0.** Wake using external interrupt source 0.
bit 0 0 = Don't wake up on external interrupt source 0.
1 = Wake up on external interrupt source 0.

System Clock Divider Register (SYSCLK)

	7	6	5	40	3	2	1	0	Reset Value
SFR $C7_H$	0	0	DIVMOD1	DIVMOD0	0	DIV2	DIV1	DIV0	00_H

DIVMOD1-0 **Clock Divide Mode**
bits 5-4 Write:

DIVMOD	DIVIDE MODE
00	Normal mode (default, no divide)
01	Immediate mode: start divide immediately, return to Normal mode on IDLE wakeup condition..
10	Delay mode: same as Immediate mode, except that the mode changes with the millisecond interrupt (MSINT). If MSINT is enabled, the divide will start on the next MSINT and return to normal mode on the following MSINT. If MSINT is not enabled, the divide will start on the next MSINT condition (even if masked) but will not leave the divide mode until the MSINT counter overflows, which follows a wakeup condition.
11	Reserved

Read:

DIVMOD	DIVISION MODE STATUS
00	No divide
01	Divider is in Immediate mode
10	Divider is in Delay mode
11	Reserved

NOTE:
Do not clear the DIVMOD register to exit Immediate or Delay modes. Exit these modes only through the appropriate interrupt (the interrupt can be either normally generated or software generated).

DIV2-0 **Divide Mode**
bit 2-0

DIV	DIVISOR
000	Divide by 2 (default)
001	Divide by 4
010	Divide by 8
011	Divide by 16
100	Divide by 32
101	Divide by 1024
110	Divide by 2048
111	Divide by 4096

Timer 2 Control (T2CON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $C8_H$	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00_H

TF2 bit 7 — **Timer 2 Overflow Flag.** This flag will be set when Timer 2 overflows from $FFFF_H$. It must be cleared by software. TF2 will only be set if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.

EXF2 bit 6 — **Timer 2 External Flag.** A negative transition on the T2EX pin (P1.1) will cause this flag to be set based on the EXEN2 (T2CON.3) bit. If set by a negative transition, this flag must be cleared to 0 by software. Setting this bit in software will force a timer interrupt if enabled.

RCLK bit 5 — **Receive Clock Flag.** This bit determines the serial Port 0 timebase when receiving data in serial modes 1 or 3.
0 = Timer 1 overflow is used to determine receiver baud rate for UART0.
1 = Timer 2 overflow is used to determine receiver baud rate for UART0.
Setting this bit will force Timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

TCLK bit 4 — **Transmit Clock Flag.** This bit determines the serial Port 0 timerbase when transmitting data in serial modes 1 or 3.
0 = Timer 1 overflow is used to determine transmitter baud rate for UART0.
1 = Timer 2 overflow is used to determine transmitter baud rate for UART0.
Setting this bit will force Timer 2 into baud rate generation mode. The timer will operate from a divide by 2 of the external clock.

EXEN2 bit 3 — **Timer 2 External Enable.** This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud rates for the serial port.
0 = Timer 2 will ignore all external events at T2EX.
1 = Timer 2 will capture or reload a value if a negative transition is detected on the T2EX pin.

TR2 bit 2 — **Timer 1 Run Control.** This bit enables/disables the operation of Timer 2. Halting this timer will preserve the current count in TH2, TL2.
0 = Timer 2 is halted.
1 = Timer 2 is enabled.

C/$\overline{T2}$ bit 1 — **Counter/Timer Select.** This bit determines whether Timer 2 will function as a timer or counter. Independent of this bit, Timer 2 runs at 2 clocks per tick when used in baud rate generator mode.
0 = Timer 2 functions as a timer. The speed of Timer 2 is determined by the T2M bit (CKCON.5).
1 = Timer 2 will count negative transitions on the T2 pin (P1.0).

CP/$\overline{RL2}$ bit 0 — **Capture/Reload Select.** This bit determines whether the capture or reload function will be used for Timer 2. If either RCLK or TCLK is set, this bit will not function and the timer will function in an auto-reload mode following each overflow.
0 = Auto-reloads will occur when Timer 2 overflows or a falling edge is detected on T2EX if EXEN2 = 1.
1 = Timer 2 captures will occur when a falling edge is detected on T2EX if EXEN2 = 1.

Timer 2 Capture LSB (RCAP2L)

	7	6	5	4	3	2	1	0	Reset Value
SFR CA_H									00_H

RCAP2L bits 7-0 — **Timer 2 Capture LSB.** This register is used to capture the TL2 value when Timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when Timer 2 is configured in auto-reload mode.

Timer 2 Capture MSB (RCAP2H)

	7	6	5	4	3	2	1	0	Reset Value
SFR CB_H									00_H

RCAP2H bits 7-0 — **Timer 2 Capture MSB.** This register is used to capture the TH2 value when Timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16-bit reload value when Timer 2 is configured in auto-reload mode.

Timer 2 LSB (TL2)

	7	6	5	4	3	2	1	0	Reset Value
SFR CC_H									00_H

TL2 bits 7-0 — **Timer 2 LSB.** This register contains the least significant byte of Timer 2.

Timer 2 MSB (TH2)

	7	6	5	4	3	2	1	0	Reset Value
SFR CD_H									00_H

TH2 bits 7-0 — **Timer 2 MSB.** This register contains the most significant byte of Timer 2.

Program Status Word (PSW)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	00_H

CY bit 7 — **Carry Flag.** This bit is set when the last arithmetic operation resulted in a carry (during addition) or a borrow (during subtraction). Otherwise it is cleared to 0 by all arithmetic operations.

AC bit 6 — **Auxiliary Carry Flag.** This bit is set to 1 if the last arithmetic operation resulted in a carry into (during addition), or a borrow (during substraction) from the high order nibble. Otherwise it is cleared to 0 by all arithmetic operations.

F0 bit 5 — **User Flag 0.** This is a bit-adressable, general-purpose flag for software control.

RS1, RS0 bits 4-3 — **Register Bank Select 1-0.** These bits select which register bank is addressed during register accesses.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00_H-07_H
0	1	1	08_H-$0F_H$
1	0	2	10_H-17_H
1	1	3	18_H-$1F_H$

OV bit 2 — **Overflow Flag.** This bit is set to 1 if the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise it is cleared to 0 by all arithmetic operations.

F1 bit 1 — **User Flag 1.** This is a bit-addressable, general-purpose flag for software control.

P bit 0 — **Parity Flag.** This bit is set to 1 if the modulo-2 sum of the 8 bits of the accumulator is 1 (odd parity); and cleared to 0 on even parity.

ADC Offset Calibration Register Low Byte (OCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D1_H$									00_H

OCL bits 7-0 — **ADC Offset Calibration Register Low Byte.** This is the low byte of the 24-bit word that contains the ADC offset calibration. A value which is written to this location will set the ADC offset calibration value.

ADC Offset Calibration Register Middle Byte (OCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D2_H$									00_H

OCM bits 7-0 **ADC Offset Calibration Register Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC offset calibration. A value which is written to this location will set the ADC offset calibration value.

ADC Offset Calibration Register High Byte (OCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D3_H$									00_H

OCH bits 7-0 **ADC Offset Calibration Register High Byte.** This is the high byte of the 24-bit word that contains the ADC offset calibration. A value which is written to this location will set the ADC offset calibration value.

ADC Gain Calibration Register Low Byte (GCL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D4_H$									$5A_H$

GCL bits 7-0 **ADC Gain Calibration Register Low Byte.** This is the low byte of the 24-bit word that contains the ADC gain calibration. A value which is written to this location will set the ADC gain calibration value.

ADC Gain Calibration Register Middle Byte (GCM)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D5_H$									EC_H

GCM bits 7-0 **ADC Gain Calibration Register Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC gain calibration. A value which is written to this location will set the ADC gain calibration value.

ADC Gain Calibration Register High Byte (GCH)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D6_H$									$5F_H$

GCH bits 7-0 **ADC Gain Calibration Register High Byte.** This is the high byte of the 24-bit word that contains the ADC gain calibration. A value which is written to this location will set the ADC gain calibration value.

ADC Multiplexer Register (ADMUX)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D7_H$	INP3	INP2	INP1	INP0	INN3	INN2	INN1	INN0	01_H

INP3-0 bits 7-4 **Input Multiplexer Positive Channel.** This selects the positive signal input.

INP3	INP2	INP1	INP0	POSITIVE INPUT
0	0	0	0	AIN0 (default)
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (Requires ADMUX = FF_H)

INN3-0 **Input Multiplexer Negative Channel.** This selects the negative signal input.
bits 3-0

INN3	INN2	INN1	INN0	NEGATIVE INPUT
0	0	0	0	AIN0
0	0	0	1	AIN1 (default)
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AINCOM
1	1	1	1	Temperature Sensor (Requires ADMUX = FF_H)

Enable Interrupt Control (EICON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D8_H$	SMOD1	1	EAI	AI	WDTI	0	0	0	40_H

SMOD1 **Serial Port 1 Mode.** When this bit is set the serial baud rate for Port 1 will be doubled.
bit 7 0 = Standard baud rate for Port 1 (default).
1 = Double baud rate for Port 1.

EAI **Enable Auxiliary Interrupt.** The Auxiliary Interrupt accesses nine different interrupts which are masked and
bit 5 identified by SFR registers PAI (SFR $A5_H$), AIE (SFR $A6_H$), and AISTAT (SFR $A7_H$).
0 = Auxiliary Interrupt disabled (default).
1 = Auxiliary Interrupt enabled.

AI **Auxiliary Interrupt Flag.** AI must be cleared by software before exiting the interrupt service routine,
bit 4 after the source of the interrupt is cleared. Otherwise, the interrupt occurs again. Setting AI in software generates an Auxiliary Interrupt, if enabled.
0 = No Auxiliary Interrupt detected (default).
1 = Auxiliary Interrupt detected.

WDTI **Watchdog Timer Interrupt Flag.** WDTI must be cleared by software before exiting the interrupt service routine.
bit 3 Otherwise, the interrupt occurs again. Setting WDTI in software generates a watchdog time interrupt, if enabled. The Watchdog timer can generate an interrupt or reset. The interrupt is available only if the reset action is disabled in HCR0.
0 = No Watchdog Timer Interrupt Detected (default).
1 = Watchdog Timer Interrupt Detected.

ADC Results Register Low Byte (ADRESL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $D9_H$									00_H

ADRESL **The ADC Results Low Byte.** This is the low byte of the 24-bit word that contains the ADC
bits 7-0 Converter Results. Reading from this register clears the ADC interrupt.

ADC Results Register Middle Byte (ADRESM)

	7	6	5	4	3	2	1	0	Reset Value
SFR DA_H									00_H

ADRESM **The ADC Results Middle Byte.** This is the middle byte of the 24-bit word that contains the ADC
bits 7-0 Converter Results.

ADC Results Register High Byte (ADRESH)

	7	6	5	4	3	2	1	0	Reset Value
SFR DB_H									00_H

ADRESH **The ADC Results High Byte.** This is the high byte of the 24-bit word that contains the ADC
bits 7-0 Converter Results.

ADC Control Register 0 (ADCON0)

	7	6	5	4	3	2	1	0	Reset Value
SFR DC_H	—	BOD	EVREF	VREFH	EBUF	PGA2	PGA1	PGA0	30_H

BOD bit 6 — **Burnout Detect.** When enabled this connects a positive current source to the positive channel and a negative current source to the negative channel. If the channel is open circuit then the ADC results will be full-scale.
0 = Burnout Current Sources Off (default).
1 = Burnout Current Sources On.

EVREF bit 5 — **Enable Internal Voltage Reference.** If the internal voltage reference is not used, it should be turned off to save power and reduce noise.
0 = Internal Voltage Reference Off.
1 = Internal Voltage Reference On (default).

VREFH bit 4 — **Voltage Reference High Select.** The internal voltage reference can be selected to be 2.5V or 1.25V.
0 = REFOUT/REF IN+ is 1.25V.
1 = REFOUT/REF IN+ is 2.5V (default).

EBUF bit 3 — **Enable Buffer.** Enable the input buffer to provide higher input impedance but limits the input voltage range and dissipates more power.
0 = Buffer disabled (default).
1 = Buffer enabled.

PGA2-0 bits 2-0 — **Programmable Gain Amplifier.** Sets the gain for the PGA from 1 to 128.

PGA2	PGA1	PGA0	GAIN
0	0	0	1 (default)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Control Register 1 (ADCON1)

	7	6	5	4	3	2	1	0	Reset Value
SFR DD_H	—	POL	SM1	SM0	—	CAL2	CAL1	CAL0	x000 0000_B

POL bit 6 — **Polarity.** Polarity of the ADC result and Summation register.
0 = Bipolar.
1 = Unipolar.

POL	ANALOG INPUT	DIGITAL OUTPUT
0	+FSR	0x7FFFFF
	ZERO	0x000000
	–FSR	0x800000
1	+FSR	0xFFFFFF
	ZERO	0x000000
	–FSR	0x000000

SM1-0 bits 5-4 — **Settling Mode.** Selects the type of filter or auto select which defines the digital filter settling characteristics.

SM1	SM0	SETTLING MODE
0	0	Auto
0	1	Fast Settling Filter
1	0	$Sinc^2$ Filter
1	1	$Sinc^3$ Filter

CAL2-0 **Calibration Mode Control Bits.**
bits 2-0

CAL2	CAL1	CAL0	CALIBRATION MODE
0	0	0	No Calibration (default)
0	0	1	Self Calibration, Offset and Gain
0	1	0	Self Calibration, Offset Only
0	1	1	Self Calibration, Gain Only
1	0	0	System Calibration, Offset Only
1	0	1	System Calibration, Gain Only
1	1	0	Reserved
1	1	1	Reserved

Read Value—000_B.

ADC Control Register 2 (ADCON2)

	7	6	5	4	3	2	1	0	Reset Value
SFR DE_H	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0	$1B_H$

DR7-0 **Decimation Ratio LSB.**
bits 7-0

ADC Control Register 3 (ADCON3)

	7	6	5	4	3	2	1	0	Reset Value
SFR DF_H	—	—	—	—	—	DR10	DR9	DR8	06_H

DR10-8 **Decimation Ratio Most Significant 3 Bits.** The output data rate = (ACLK + 1)/64/Decimation Ratio.
bits 2-0

Accumulator (A or ACC)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E0_H$	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00_H

ACC.7-0 **Accumulator.** This register serves as the accumulator for arithmetic and logic operations.
bits 7-0

Summation/Shifter Control (SSCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E1_H$	SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	00_H

The Summation register is powered down when the ADC is powered down. If all zeroes are written to this register the 32-bit SUMR3-0 registers will be cleared. The Summation registers will do sign extend if Bipolar is selected in ADCON1.

SSCON1-0 **Summation/Shift Control.**
bits 7-6

SSCON1	SSCON0	SCNT2	SCNT1	SCNT0	SHF2	SHF1	SHF0	DESCRIPTION
0	0	0	0	0	0	0	0	Clear Summation Register
0	0	0	1	0	0	0	0	CPU Summation on Write to SUMR0
0	0	1	0	0	0	0	0	CPU Subtraction on Write to SUMR0
1	0	x	x	x	Note (1)	Note (1)	Note (1)	CPU Shift Only
0	1	Note (1)	Note (1)	Note (1)	x	x	x	ADC Summation Only
1	1	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	Note (1)	ADC Summation Completes then Shift Completes

NOTES: (1) Refer to register bit definition.

SCNT2-0 **Summation Count.** When the summation is complete an interrupt will be generated unless masked. Reading the
bits 5-3 SUMR0 register clears the interrupt.

SCNT2	SCNT1	SCNT0	SUMMATION COUNT
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

SHF2-0 **Shift Count.**
bits 2-0

SHF2	SHF1	SHF0	SHIFT	DIVIDE
0	0	0	1	2
0	0	1	2	4
0	1	0	3	8
0	1	1	4	16
1	0	0	5	32
1	0	1	6	64
1	1	0	7	128
1	1	1	8	256

Summation Register 0 (SUMR0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E2_H$									00_H

SUMR0 **Summation Register 0.** This is the least significant byte of the 32-bit summation register or bits 0 to 7.
bits 7-0 Write: will cause values in SUMR3-0 to be added to the summation register.
Read: will clear the Summation Count Interrupt.

Summation Register 1 (SUMR1)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E3_H$									00_H

SUMR1 **Summation Register 1.** This is the most significant byte of the lowest 16 bits of the summation register or bits 8-15.
bits 7-0

Summation Register 2 (SUMR2)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E4_H$									00_H

SUMR2 **Summation Register 2.** This is the most significant byte of the lowest 24 bits of the summation register or bits 16-23.
bits 7-0

Summation Register 3 (SUMR3)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E5_H$									00_H

SUMR3 **Summation Register 3.** This is the most significant byte of the 32-bit summation register or bits 24-31.
bits 7-0

Offset DAC Register (ODAC)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E6_H$									00_H

ODAC **Offset DAC Register.** This register will shift the input by up to half of the ADC input range. The least
bits 7-0 significant bit is equal to the input voltage range divided by 256. The input range will depend on the setting of the PGA. The ODAC is a signed magnitude register with bit 7 providing the sign of the offset and bits 6-0 providing the magnitude.

bit 7 Offset DAC Sign bit.
0 = Positive
1 = Negative

bit 6-0 $$\text{Offset} = \frac{V_{REF}}{2 \bullet \text{PGA}} \bullet \left(\frac{\text{ODAC}[6:0]}{127} \right) \bullet (-1)^{\text{bit 7}}$$

NOTE: The offset must be used after calibration or the calibration will nullify the effects.

Low Voltage Detect Control (LVDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E7_H$	ALVDIS	ALVD2	ALVD1	ALVD0	DLVDIS	DLVD2	DLVD1	DLVD0	00_H

ALVDIS **Analog Low Voltage Detect Disable.**
bit 7 0 = Enable Detection of Low Analog Supply Voltage.
1 = Disable Detection of Low Analog Supply Voltage.

ALVD2-0 **Analog Voltage Detection Level.**
bits 6-4

ALVD2	ALVD1	ALVD0	VOLTAGE LEVEL
0	0	0	AV_{DD} 2.7V (default)
0	0	1	AV_{DD} 3.0V
0	1	0	AV_{DD} 3.3V
0	1	1	AV_{DD} 4.0V
1	0	0	AV_{DD} 4.2V
1	0	1	AV_{DD} 4.5V
1	1	0	AV_{DD} 4.7V
1	1	1	External Voltage AIN7 Compared to 1.2V

DLVDIS **Digital Low Voltage Detect Disable.**
bit 3 0 = Enable Detection of Low Digital Supply Voltage.
1 = Disable Detection of Low Digital Supply Voltage.

DLVD2-0 **Digital Voltage Detection Level.**
bits 2-0

DLVD2	DLVD1	DLVD0	VOLTAGE LEVEL
0	0	0	DV_{DD} 2.7V (default)
0	0	1	DV_{DD} 3.0V
0	1	0	DV_{DD} 3.3V
0	1	1	DV_{DD} 4.0V
1	0	0	DV_{DD} 4.2V
1	0	1	DV_{DD} 4.5V
1	1	0	DV_{DD} 4.7V
1	1	1	External Voltage AIN6 Compared to 1.2V

Extended Interrupt Enable (EIE)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E8_H$	1	1	1	EWDI	EX5	EX4	EX3	EX2	$E0_H$

EWDI **Enable Watchdog Interrupt.** This bit enables/disables the watchdog interrupt. The Watchdog timer is enabled by the WDTCON (SFR FF_H) and PDCON (SFR $F1_H$) registers.
bit 4 0 = Disable the Watchdog Interrupt
1 = Enable Interrupt Request Generated by the Watchdog Timer

EX5 **External Interrupt 5 Enable.** This bit enables/disables external interrupt 5.
bit 3 0 = Disable External Interrupt 5
1 = Enable External Interrupt 5

EX4 **External Interrupt 4 Enable.** This bit enables/disables external interrupt 4.
bit 2 0 = Disable External Interrupt 4
1 = Enable External Interrupt 4

EX3 **External Interrupt 3 Enable.** This bit enables/disables external interrupt 3.
bit 1 0 = Disable External Interrupt 3
1 = Enable External Interrupt 3

EX2 **External Interrupt 2 Enable.** This bit enables/disables external interrupt 2.
bit 0 0 = Disable External Interrupt 2
1 = Enable External Interrupt 2

Hardware Product Code Register 0 (HWPC0)

	7	6	5	4	3	2	1	0	Reset Value
SFR $E9_H$	HWPC0.7	HWPC0.6	HWPC0.5	HWPC0.4	HWPC0.3	1	MEMORY SIZE		0000_001xx_B

HWPC0.7-0 **Hardware Product Code LSB.** Read only.
bits 7-0

MEMORY SIZE		MODEL	FLASH MEMORY
0	0	MSC1211Y2	4kB
0	1	MSC1211Y3	8kB
1	0	MSC1211Y4	16kB
1	1	MSC1211Y5	32kB

Hardware Product Code Register 1 (HWPC1)

	7	6	5	4	3	2	1	0	Reset Value
SFR EA_H					1				08_H

HWPC1.7-0 **Hardware Product Code MSB.** Read only.
bits 7-0

Hardware Version Register (HDWVER)

	7	6	5	4	3	2	1	0	Reset Value
SFR EB_H									

Flash Memory Control (FMCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EE_H	0	PGERA	0	FRCM	0	BUSY	1	0	02_H

PGERA **Page Erase.** Available in both user and program modes.
bit 6 0 = Disable Page Erase Mode
1 = Enable Page Erase Mode

FRCM **Frequency Control Mode.** The bypass is only used for slow clocks to save power.
bit 4 0 = Bypass (default)
1 = Use Delay Line. Saves power (Recommended).

BUSY **Write/Erase BUSY Signal.**
bit 2 0 = Idle or Available
1 = Busy

Flash Memory Timing Control Register (FTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR EF_H	FER3	FER2	FER1	FER0	FWR3	FWR2	FWR1	FWR0	$A5_H$

Refer to Flash Timing Characteristics

FER3-0 **Set Erase.** Flash Erase Time = (1 + FER) • (MSEC + 1) • t_{CLK}.
bits 7-4 11ms industrial temperature range.
5ms commercial temperature range.

FWR3-0 **Set Write.** Flash Write Time = (1 + FWR) • (USEC + 1) • 5 • t_{CLK}.
bits 3-0 30µs to 40µs.

B Register (B)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F0_H$	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00_H

B.7-0 **B Register.** This register serves as a second accumulator for certain arithmetic operations.
bits 7-0

Power-Down Control Register (PDCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F1_H$	0	PDDAC	PDI2C	PDPWM	PDAD	PDWDT	PDST	PDSPI	$7F_H$

Turning peripheral modules off puts the MSC1211 in the lowest power mode.

PDDAC **Pulse Width Module Control.**
bit 6 0 = DACs On
1 = DACs Power Down

PDI2C **I2C Control.**
bit 5 0 = I2C On (the state is undefined if PDSPI is also = 0)
1 = I2C Power Down

PDPWM **Pulse Width Module Control.**
bit 4 0 = PWM On
1 = PWM Power Down

PDAD **ADC Control.**
bit 3 0 = ADC On
1 = ADC, V_{REF}, Summation registers, and Analog Brownout are powered down. Analog current = 0.

PDWDT **Watchdog Timer Control.**
bit 2 0 = Watchdog Timer On
1 = Watchdog Timer Power Down

PDST **System Timer Control.**
bit 1 0 = System Timer On
1 = System Timer Power Down

PDSPI **SPI System Control.**
bit 0 0 = SPI System On (the state is undefined if PDI2C is also = 0)
1 = SPI System Power Down

$\overline{\text{PSEN}}$/ALE Select (PASEL)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F2_H$	0	0	PSEN2	PSEN1	PSEN0	0	ALE1	ALE0	00_H

PSEN2-0 **$\overline{\text{PSEN}}$ Mode Select.**
bits 5-3

PSEN2	PSEN1	PSEN0	
0	0	X	$\overline{\text{PSEN}}$
0	1	X	CLK
1	0	X	ADC MODCLK
1	1	0	LOW
1	1	1	HIGH

ALE1-0 **ALE Mode Select.**
bits 1-0

ALE1	ALE0	
0	X	ALE
1	0	LOW
1	1	HIGH

Analog Clock (ACLK)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F6_H$	0	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03_H

FREQ6-0 **Clock Frequency – 1.** This value + 1 divides the system clock to create the ADC clock.
bits 6-0 ACLK frequency = $f_{CLK}/(FREQ + 1)$
$f_{MOD} = f_{CLK}/(FREQ + 1)/64$
Data Rate = f_{MOD}/Decimation

System Reset Register (SRST)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F7_H$	0	0	0	0	0	0	0	RSTREQ	00_H

RSTREQ **Reset Request.** Setting this bit to 1 and then clearing to 0 will generate a system reset.
bit 0

Extended Interrupt Priority (EIP)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F8_H$	1	1	1	PWDI	PX5	PX4	PX3	PX2	$E0_H$

PWDI **Watchdog Interrupt Priority.** This bit controls the priority of the watchdog interrupt.
bit 4 0 = The watchdog interrupt is low priority.
1 = The watchdog interrupt is high priority.

PX5 **External Interrupt 5 Priority.** This bit controls the priority of external interrupt 5.
bit 3 0 = External interrupt 5 is low priority.
1 = External interrupt 5 is high priority.

PX4 **External Interrupt 4 Priority.** This bit controls the priority of external interrupt 4.
bit 2 0 = External interrupt 4 is low priority.
1 = External interrupt 4 is high priority.

PX3 **External Interrupt 3 Priority.** This bit controls the priority of external interrupt 3.
bit 1 0 = External interrupt 3 is low priority.
1 = External interrupt 3 is high priority.

PX2 **External Interrupt 2 Priority.** This bit controls the priority of external interrupt 2.
bit 0 0 = External interrupt 2 is low priority.
1 = External interrupt 2 is high priority.

Seconds Timer Interrupt (SECINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR $F9_H$	WRT	SECINT6	SECINT5	SECINT4	SECINT3	SECINT2	SECINT1	SECINT0	$7F_H$

This system clock is divided by the value of the 16-bit register MSECH:MSECL. Then that 1ms timer tick is divided by the register HMSEC which provides the 100ms signal used by this seconds timer. Therefore, this seconds timer can generate an interrupt which occurs from 100ms to 12.8 seconds. Reading this register will clear the Seconds Interrupt. This Interrupt can be monitored in the AIE register.

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished.
bit 7 Read = 0.
0 = Delay Write Operation. The SEC value is loaded when the current count expires.
1 = Write Immediately. The counter is loaded once the CPU completes the write operation.

SECINT6-0 **Seconds Count.** Normal operation would use 100ms as the clock interval.
bits 6-0 Seconds Interrupt = (1 + SEC) • (HMSEC + 1) • (MSEC + 1) • t_{CLK}.

Milliseconds Interrupt (MSINT)

	7	6	5	4	3	2	1	0	Reset Value
SFR FA_H	WRT	MSINT6	MSINT5	MSINT4	MSINT3	MSINT2	MSINT1	MSINT0	$7F_H$

The clock used for this timer is the 1ms clock which results from dividing the system clock by the values in registers MSECH:MSECL. Reading this register will clear the interrupt.

WRT **Write Control.** Determines whether to write the value immediately or wait until the current count is finished. Read = 0.
bit 7 0 = Delay Write Operation. The MSINT value is loaded when the current count expires.
1 = Write Immediately. The MSINT counter is loaded once the CPU completes the write operation.

MSINT6-0 **Seconds Count.** Normal operation would use 1ms as the clock interval.
bits 6-0 MS Interrupt Interval = (1 + MSINT) • (MSEC + 1) • t_{CLK}

One Microsecond Register (USEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FB_H	0	0	0	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0	03_H

FREQ4-0 **Clock Frequency – 1.** This value + 1 divides the system clock to create a 1µs Clock.
bits 4-0 USEC = CLK/(FREQ + 1). This clock is used to set Flash write time. See FTCON (SFR EF_H).

One Millisecond Low Register (MSECL)

	7	6	5	4	3	2	1	0	Reset Value
SFR FC_H	MSECL7	MSECL6	MSECL5	MSECL4	MSECL3	MSECL2	MSECL1	MSECL0	$9F_H$

MSECL7-0 **One Millisecond Low.** This value in combination with the next register is used to create a 1ms Clock.
bits 7-0 1ms Clock = (MSECH • 256 + MSECL + 1) • t_{CLK}. This clock is used to set Flash erase time. See FTCON (SFR EF_H).

One Millisecond High Register (MSECH)

	7	6	5	4	3	2	1	0	Reset Value
SFR FD_H	MSECH7	MSECH6	MSECH5	MSECH4	MSECH3	MSECH2	MSECH1	MSECH0	$0F_H$

MSECH7-0 **One Millisecond High.** This value in combination with the previous register is used to create a 1ms clock.
bits 7-0 1ms = (MSECH • 256 + MSECL + 1) • t_{CLK}.

One Hundred Millisecond Register (HMSEC)

	7	6	5	4	3	2	1	0	Reset Value
SFR FE_H	HMSEC7	HMSEC6	HMSEC5	HMSEC4	HMSEC3	HMSEC2	HMSEC1	HMSEC0	63_H

HMSEC7-0 **One Hundred Millisecond.** This clock divides the 1ms clock to create a 100ms clock.
bits 7-0 100ms = (MSECH • 256 + MSECL + 1) • (HMSEC + 1) • t_{CLK}.

Watchdog Timer Register (WDTCON)

	7	6	5	4	3	2	1	0	Reset Value
SFR FF_H	EWDT	DWDT	RWDT	WDCNT4	WDCNT3	WDCNT2	WDCNT1	WDCNT0	00_H

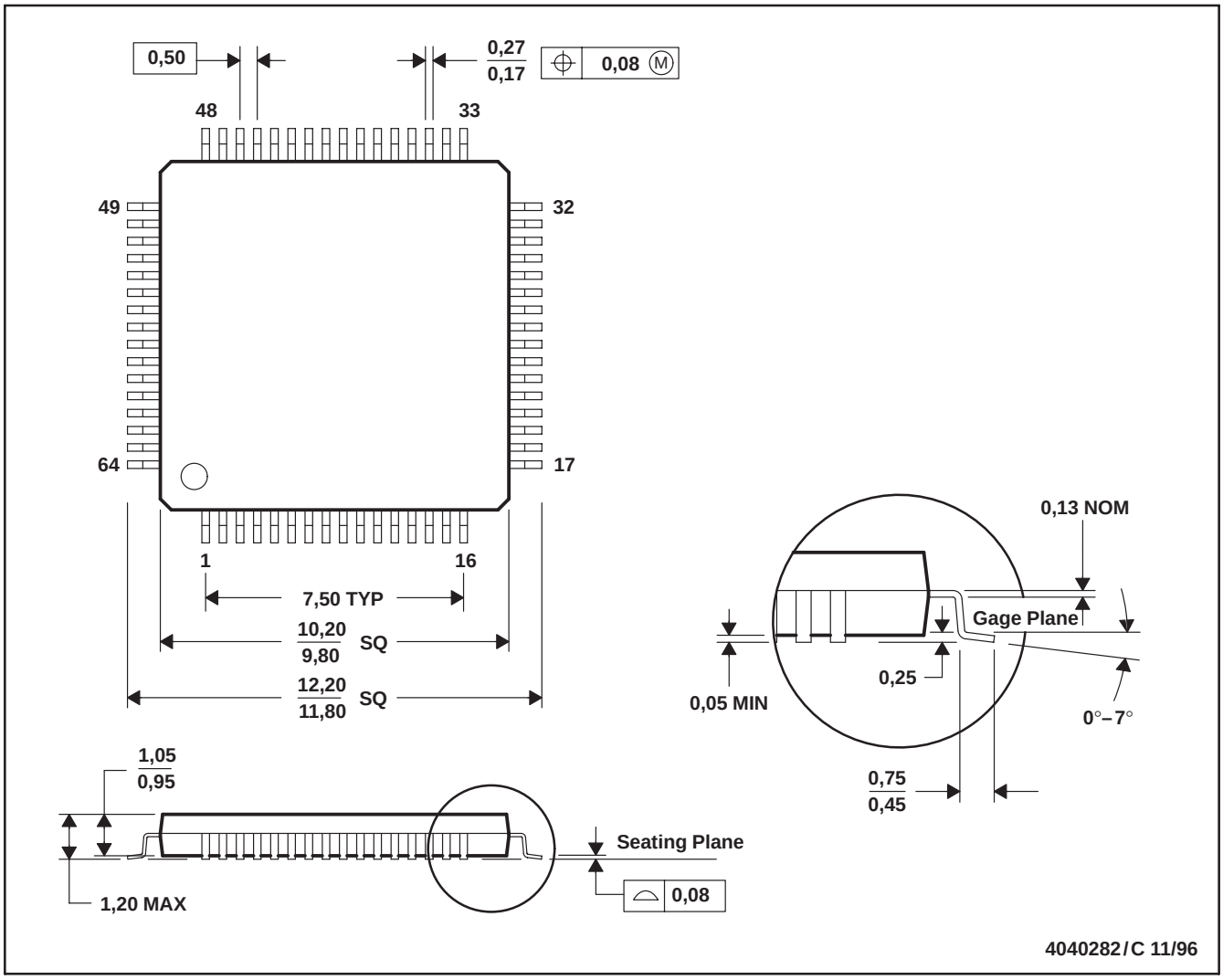
EWDT **Enable Watchdog (R/W).**
bit 7 Write 1/Write 0 sequence sets the Watchdog Enable Counting bit.

DWDT **Disable Watchdog (R/W).**
bit 6 Write 1/Write 0 sequence clears the Watchdog Enable Counting bit.

RWDT **Reset Watchdog (R/W).**
bit 5 Write 1/Write 0 sequence restarts the Watchdog Counter.

WDCNT4-0 **Watchdog Count (R/W).**
bits 4-0 Watchdog expires in (WDCNT + 1) • HMSEC to (WDCNT + 2) • HMSEC, if the sequence is not asserted. There is an uncertainty of 1 count.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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