



Universidade Federal de Santa Catarina
Centro Tecnológico – CTC
Departamento de Engenharia Elétrica



“EEL7020 – Sistemas Digitais”

Prof. Eduardo Augusto Bezerra

Eduardo.Bezerra@eel.ufsc.br

Florianópolis, março de 2013.

“Desenvolvimento de Sistemas Digitais com FPGAs”

Material utilizado no Lab 1:

- lab1_FPGAs.ppt
- DE2_introduction.pdf
- DE2_UserManual.pdf
- Capítulo 1 do livro texto

Roteiro da aula

1. Apresentação **lab1_FPGAs.ppt**
Slides 1..14, 31..33, 55..58
2. Na pasta *altera\DE2\DE2_user_manual DE2_introduction*
 - Arquivo **DE2_introduction.pdf** (*aplicações da placa*)
 - Arquivo **DE2_UserManual.pdf** (*pinagem da placa*)
3. Versão em PDF do capítulo 1 to livro texto disponível no site da disciplina
4. Seguir o tutorial **COMPLETO** descrito no livro texto, pois esse fluxo será utilizado em todas as aulas de laboratório do semestre.

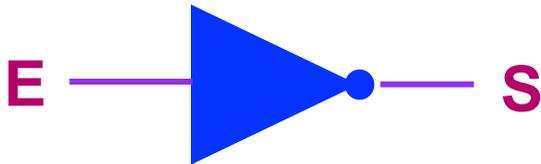
Motivação – Indústria de Circuitos Integrados

INVERSOR CMOS

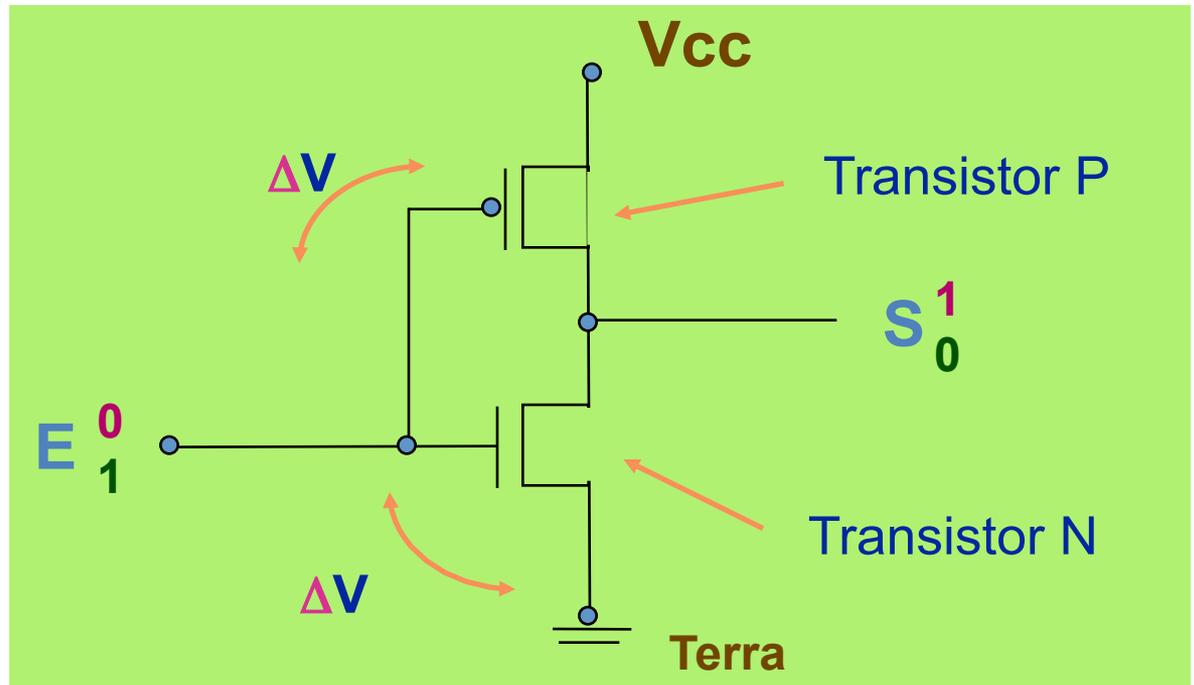
- Equação:

$$S = \overline{E}$$

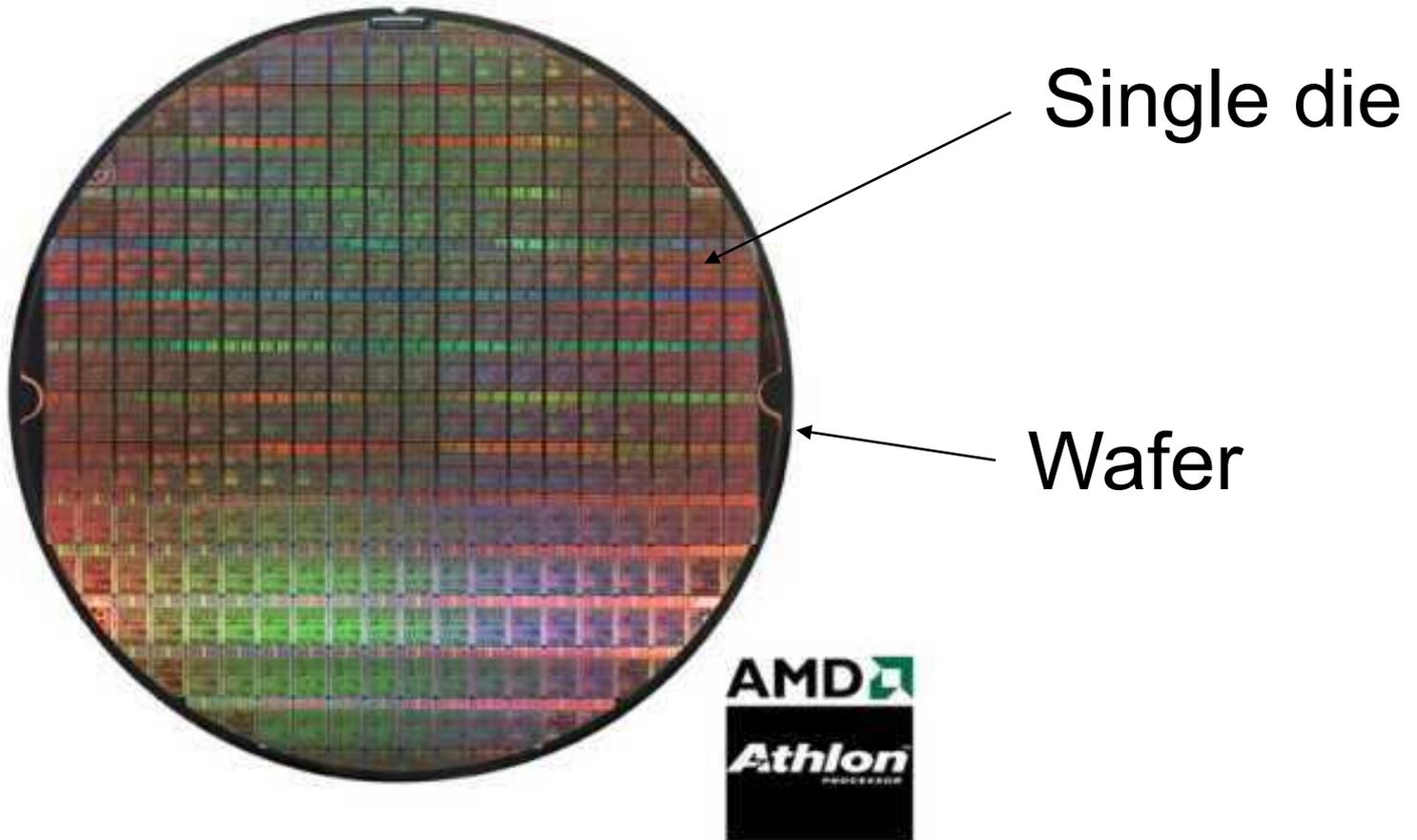
- Esquema Lógico



- Esquema Elétrico CMOS



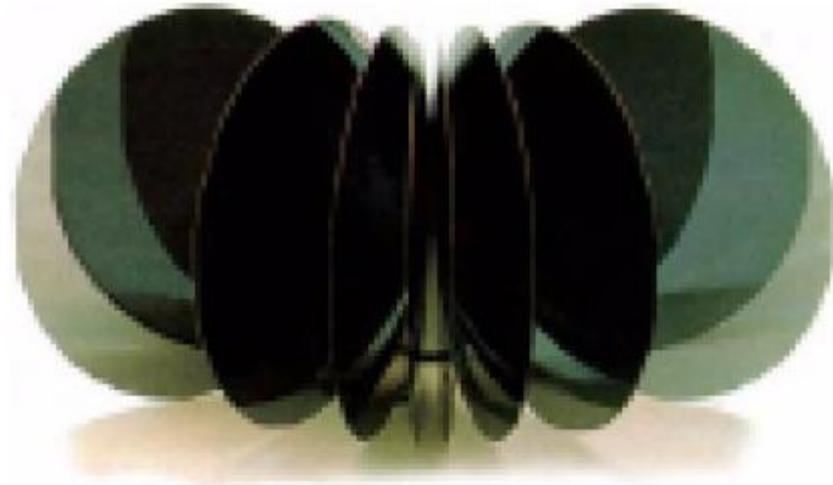
Motivação – Indústria de Circuitos Integrados



Obtido em <http://www.amd.com>

Motivação – Indústria de Circuitos Integrados

- SiO_2 , átomos de silício e oxigênio ligados por seus elétrons.
- O_2 é retirado em laboratório, e os átomos de silício resultantes formam cristal de silício puro.
- Próximo ao zero absoluto, os elétrons de silício se ocupam apenas em manter a estrutura do cristal.
- Aumentando para temperatura ambiente, átomos de Si vibram o suficiente para gerar energia térmica possibilitando seus elétrons saltar para camada de condução.
- Cristal de Silício a ser “fatiado”. Diâmetro varia de 10 a 30 cm.
- Wafers de silício (fatias) com espessura em torno de 1mm.



Tecnologia CMOS: fabricação

Processo de fotolitografia

- Depósito de produto químico (se altera na presença de luz) na superfície do chip;*
- Com lente micro, luz altera regiões do material com produto químico;*
- Solvente remove regiões alteradas;*
- Regiões não atingidas pela luz permanecem, formando transistores;*
- Processo se repete, com outros produtos, formando também isoladores e conexões.*

Remoção do revestimento foto-resistivo (*ashing*)

Outras etapas do processo

Girar, lavar, secar (*spin, rinse, dry*)

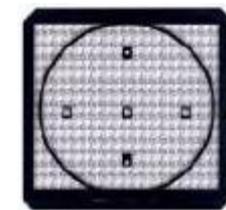
Ataque ácido

Desenvolvimento foto-resistivo

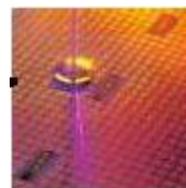
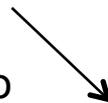
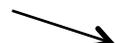
Revestimento foto-resistivo

Oxidação

Máscara Óptica



Exposição UV (*stepper exposure*)



Portas Lógicas Básicas e Tabela Verdade



OR

A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

$$S = A \text{ or } B$$

$$S = A + B$$

$$S = A | B$$

AND

A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

$$S = A \text{ and } B$$

$$S = A \cdot B$$

$$S = A \& B$$

XOR

A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

$$S = A \text{ xor } B$$

$$S = A \oplus B$$

$$S = A \wedge B$$

NOT

A	S
0	1
1	0

$$S = \text{not } A$$

$$S = \bar{A}$$

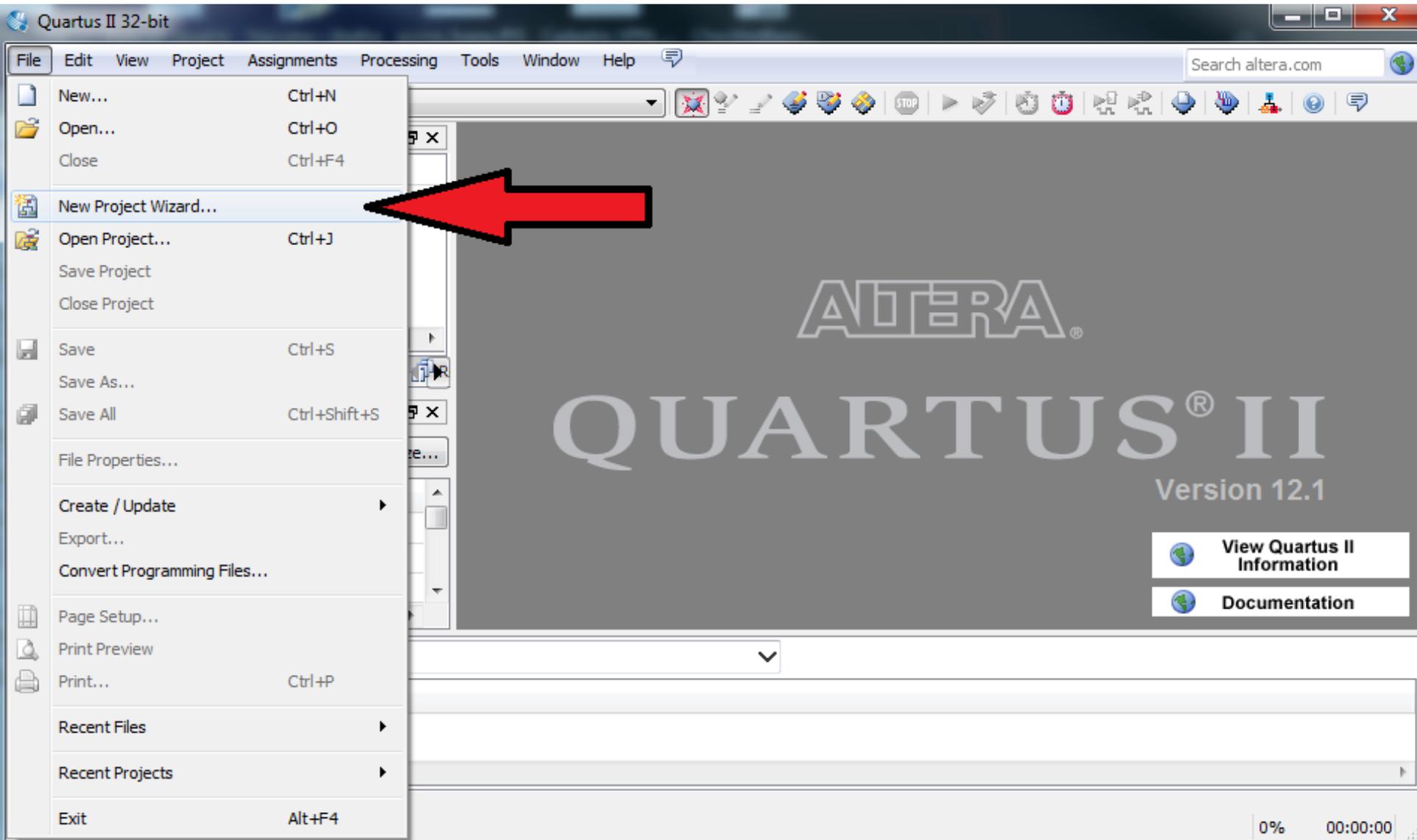
$$S = !A$$

Tarefa a ser realizada na aula prática

Tarefa a ser realizada na aula prática

- **Utilizando a ferramenta Quartus II da Altera, criar um projeto de circuito digital (esquemático) com as 4 portas lógicas apresentadas no slide 8.**
- **Realizar a simulação das portas lógicas no Quartus II, e levantar a tabela verdade para cada uma das portas.**
- **O objetivo principal dessa aula prática é possibilitar que o aluno tenha um primeiro contato com as ferramentas de desenvolvimento a serem utilizadas durante o semestre.**
- **Seguir o tutorial existente na seção “Laboratory assignment” do capítulo 1 do livro texto.**
- **Um resumo desse tutorial está incluído nos slides a seguir.**

Criar um novo projeto



Escolher a pasta e nome do projeto

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

 ...

What is the name of this project?

 ...

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

 ...

< Back **Next >** Finish Cancel Help

Seleccionar o dispositivo alvo (FPGA)

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone II

Devices: All

Target device

Auto device selected by the Fitter

Specific device selected in 'Available devices' list

Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

Show advanced devices HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	a1 C1
EP2C35F484C7	1.2V	33216	322	483840	70	4	16
EP2C35F484C8	1.2V	33216	322	483840	70	4	16
EP2C35F484I8	1.2V	33216	322	483840	70	4	16
EP2C35F672C6	1.2V	33216	475	483840	70	4	16
EP2C35F672C7	1.2V	33216	475	483840	70	4	16
EP2C35F672C8	1.2V	33216	475	483840	70	4	16
EP2C35F672I8	1.2V	33216	475	483840	70	4	16

Companion device

HardCopy:

Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

Configurar a ferramenta de simulação

New Project Wizard

EDA Tool Settings [page 4 of 5]

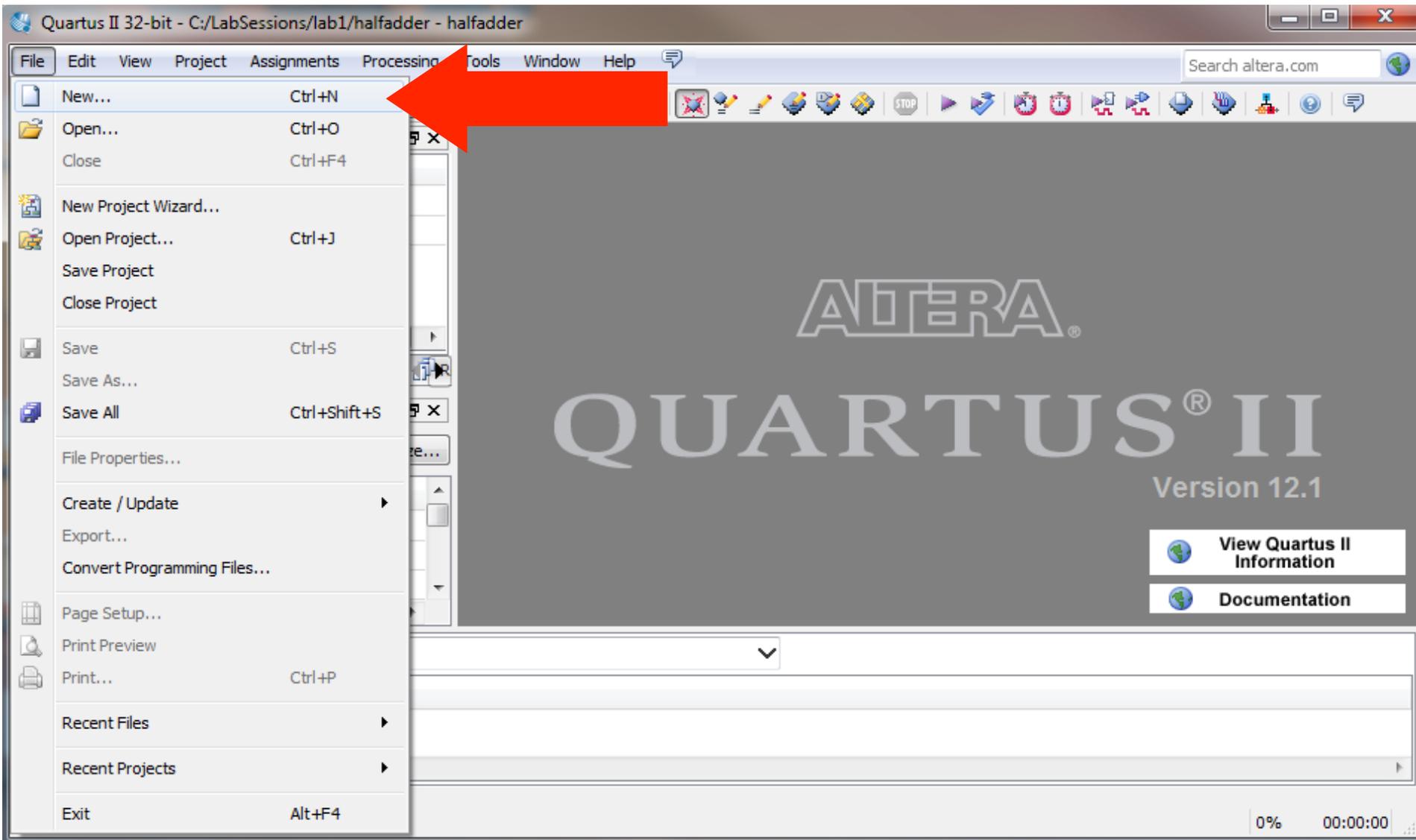
Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

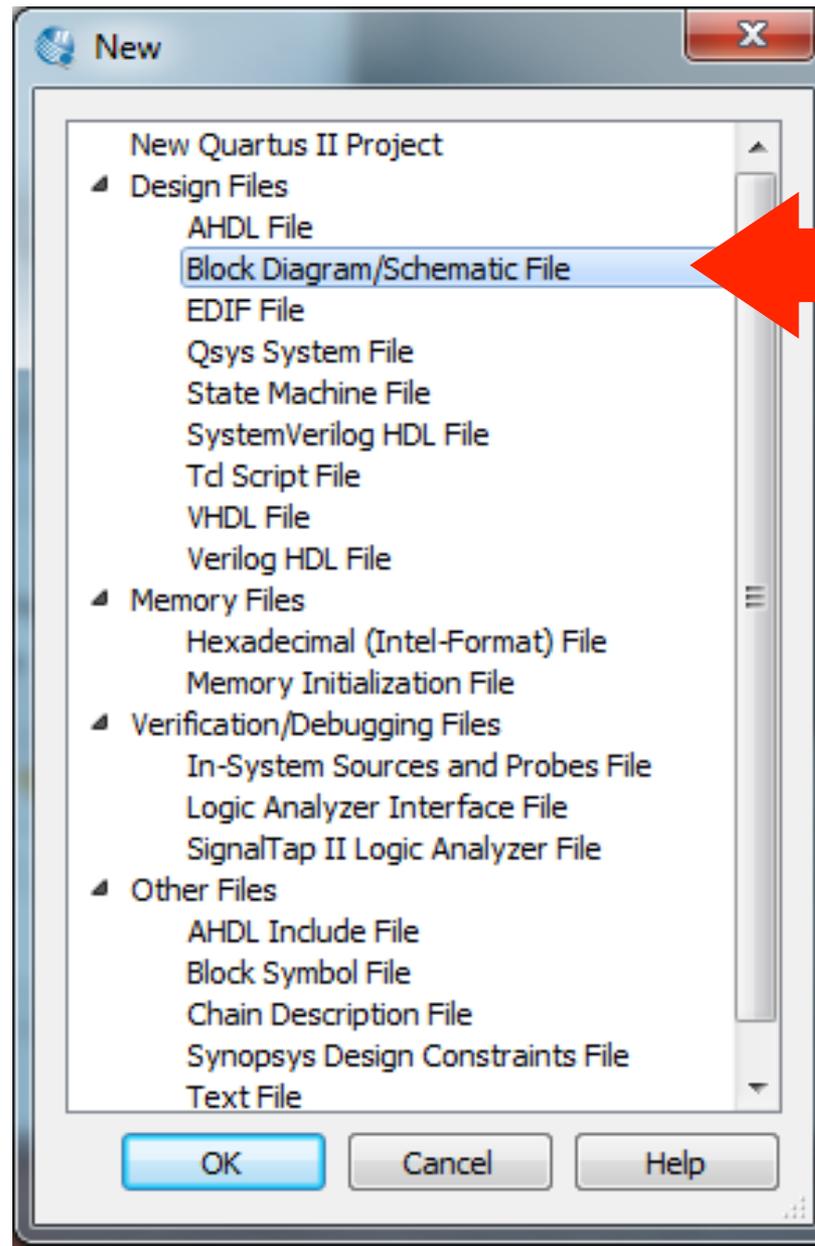
Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

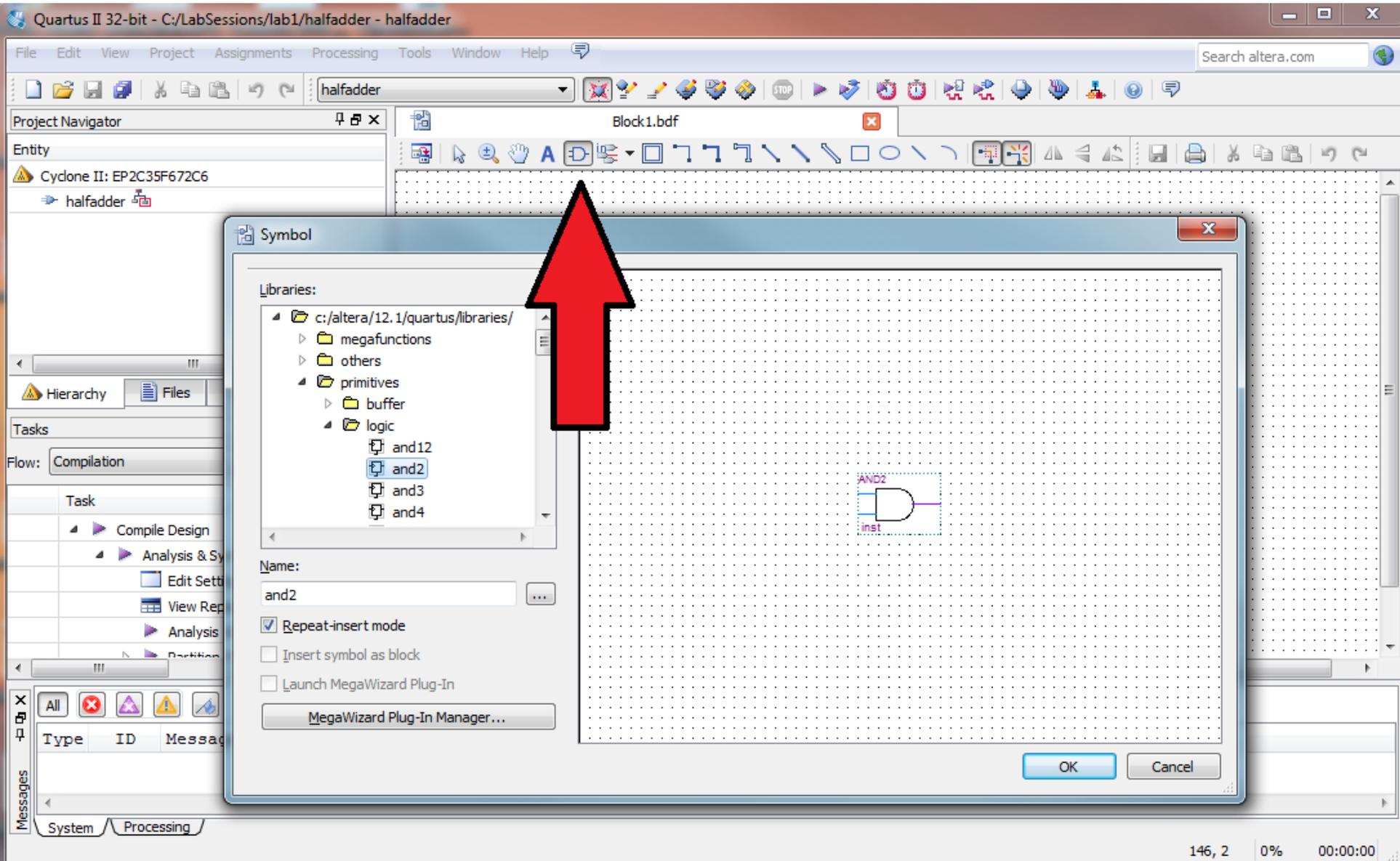
Criar um novo diagrama de esquemático



Criar um novo diagrama de esquemático



Entrar com as portas lógicas



The image shows the Quartus II software interface. The main window displays a schematic editor for a block named "Block1.bdf". A "Symbol" dialog box is open, showing a tree view of libraries. The "logic" folder is expanded, and the "and2" component is selected. A red arrow points from the "and2" component in the library to the schematic editor, where a 2-input AND gate symbol is visible. The dialog box also shows the "Name" field set to "and2" and the "Repeat-insert mode" checkbox checked. The background interface includes the Project Navigator, Entity list, and various toolbars.

Quartus II 32-bit - C:/LabSessions/lab1/halfadder - halfadder

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Block1.bdf

Entity

Cyclone II: EP2C35F672C6

halfadder

Symbol

Libraries:

- c:/altera/12.1/quartus/libraries/
 - megafunctions
 - others
 - primitives
 - buffer
 - logic
 - and12
 - and2
 - and3
 - and4

Name:

and2

Repeat-insert mode

Insert symbol as block

Launch MegaWizard Plug-In

MegaWizard Plug-In Manager...

OK Cancel

146, 2 0% 00:00:00

Realizar as conexões das portas lógicas

The image shows the Quartus II software interface for a logic design project. The main workspace displays a logic diagram for a half adder. The diagram features two input ports, A0 and B0, connected to two logic gates: an XOR gate (inst2) and an AND2 gate (inst). A large red arrow points to the connection point between the two gates. The interface includes a Project Navigator on the left, a toolbar at the top, and a Messages panel at the bottom.

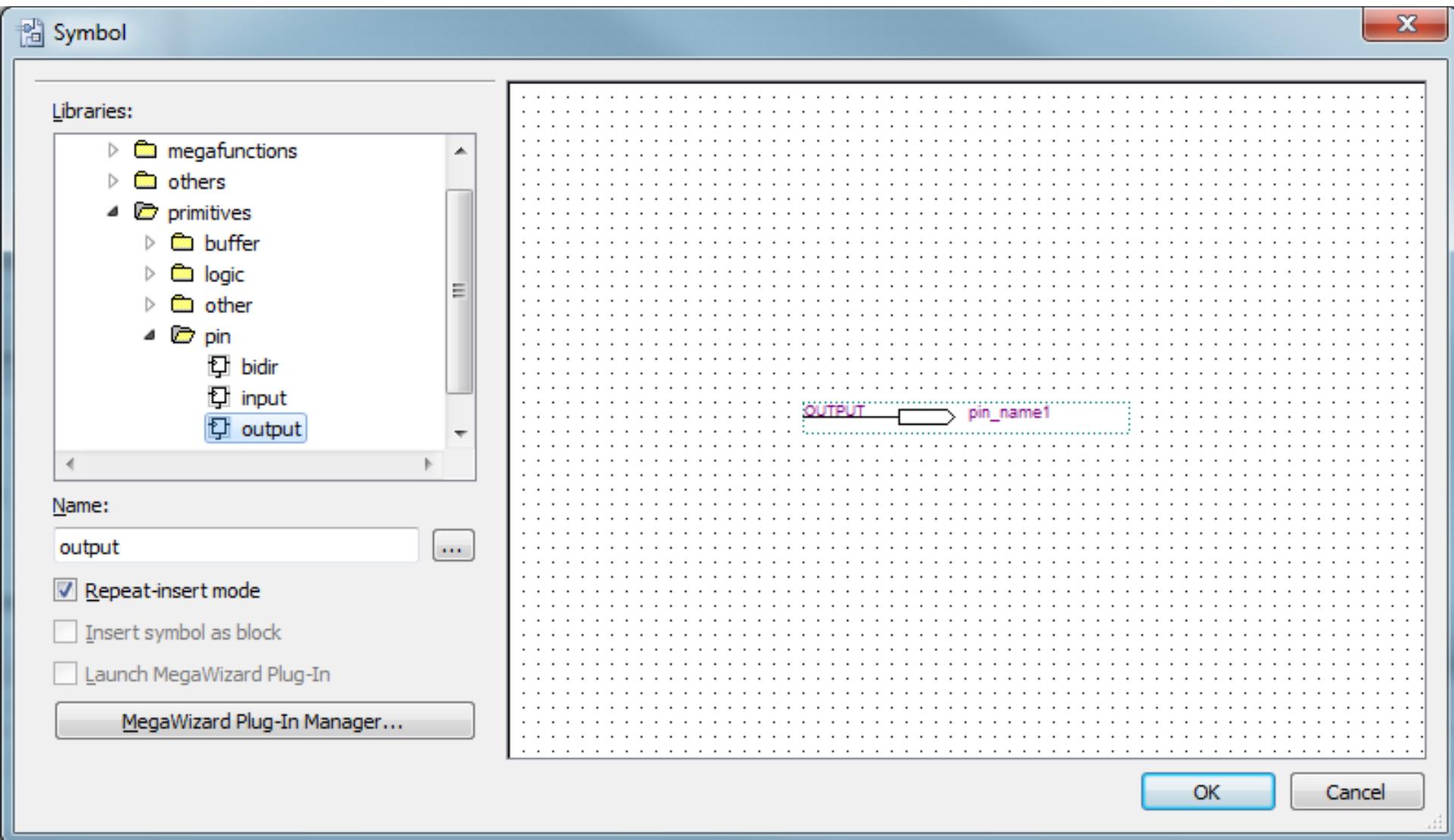
Project Navigator: Entity: Cydnone II: EP2C35F672C6, halfadder

Tasks: Flow: Compilation, Task: Compile Design, Analysis & Synthesis, Edit Settings, View Report, Analysis & Elaboration, Partition Merge

Messages: System, Processing

320,9 0% 00:00:00

Entrar com os pinos de entrada e saída



Conectar os pinos de entrada e saída e as portas lógicas

The image shows the Quartus II software interface for a half adder circuit. The main workspace displays a logic diagram with two input pins, A0 and B0, connected to an XOR gate (inst2) and an AND gate (inst). The XOR gate output is connected to an output pin labeled S0, and the AND gate output is connected to an output pin labeled pin_name2. The interface includes a Project Navigator on the left, a menu bar at the top, and a status bar at the bottom.

Project Navigator:

- Entity: Cystone II: EP2C35F672C6
- halfadder

Tasks:

- Flow: Compilation
- Task: Compile Design
- Analysis & Synthesis
- Edit Settings
- View Report
- Analysis & Elaboration
- Partition Merge

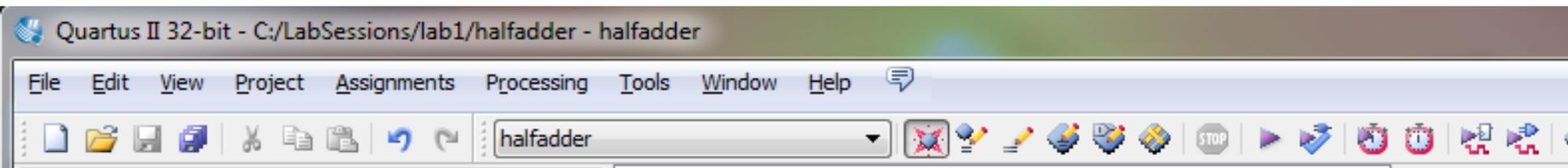
Logic Diagram:

- Inputs: A0, B0
- Logic: XOR (inst2), AND (inst)
- Outputs: S0, pin_name2

Status Bar:

- 727,246 | 0% | 00:00:00

Realizar a síntese do circuito (*compile*)



Configurar a ferramenta de simulação

The screenshot displays the Quartus II 32-bit software interface. The 'Tools' menu is open, and the 'Options...' option is highlighted with a red arrow. The interface includes a Project Navigator on the left, a Tasks pane, and a Messages pane at the bottom. The Messages pane shows a successful compilation report for the 'halfadder' project.

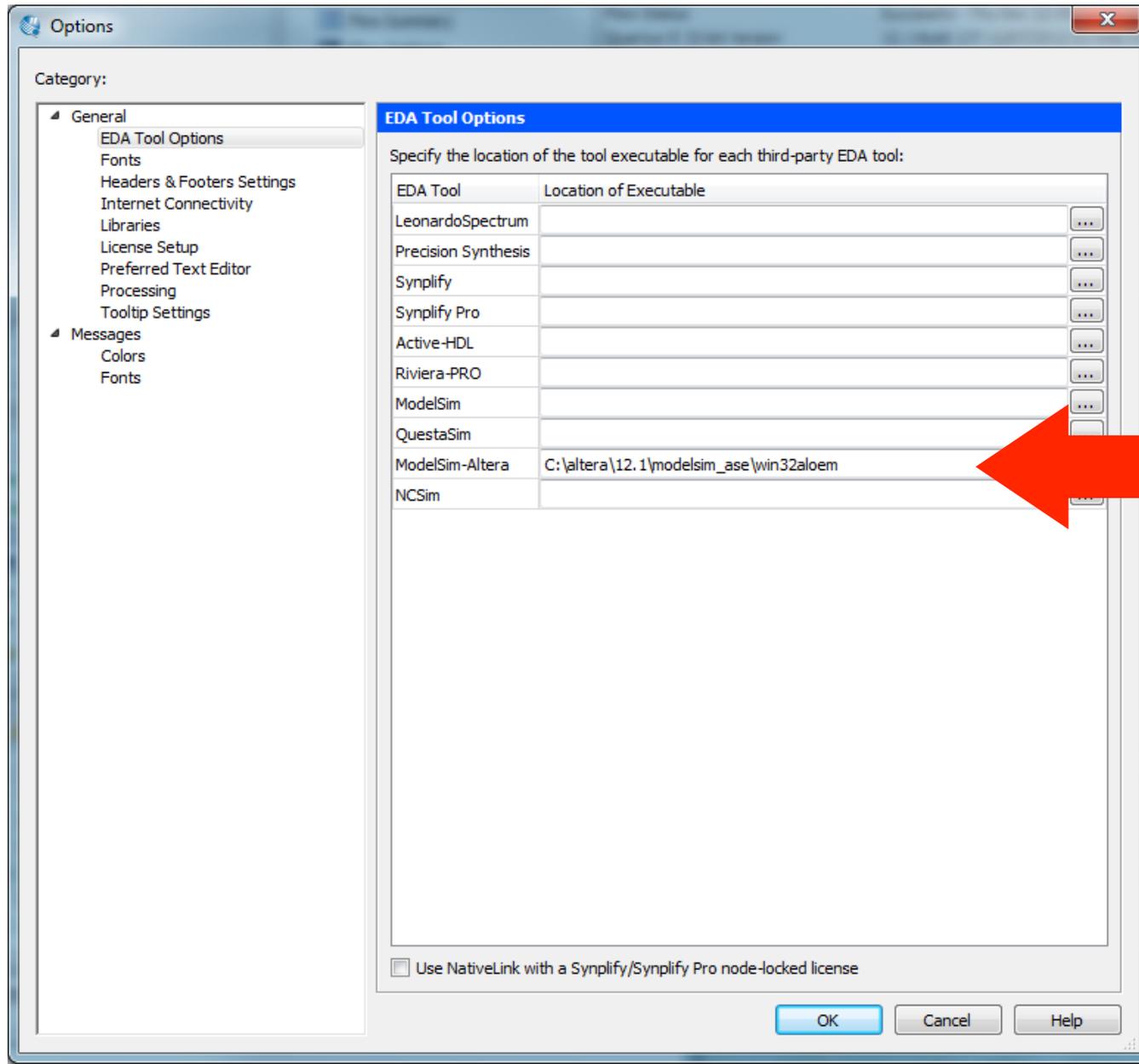
Compilation Report - halfadder

Summary	
Status	Successful - Thu Nov 22 09:17:35 2012
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Project Name	halfadder
Level Entity Name	halfadder
Device	Cyclone II EP2C35F672C6
Model	Final
Logic elements	2 / 33,216 (< 1 %)
Total combinational functions	2 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Registers	0
Pins	4 / 475 (< 1 %)
Virtual pins	0
Memory bits	0 / 483,840 (0 %)
Added Multiplier 9-bit elements	0 / 70 (0 %)
PLLs	0 / 4 (0 %)

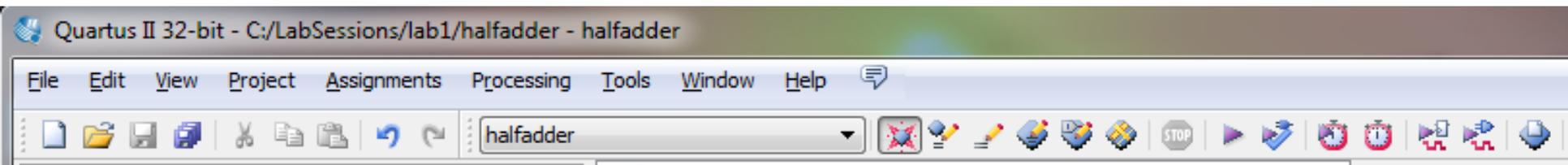
Messages

```
*****
Running Quartus II 32-bit EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off halfadder -c halfadder
204026 Generated files "halfadder.vho", "halfadder_fast.vho", "halfadder_vhd.sdo" and "halfadder_vhd_fast.sdo" in directory "C:/LabSes.
Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 8 warnings
```

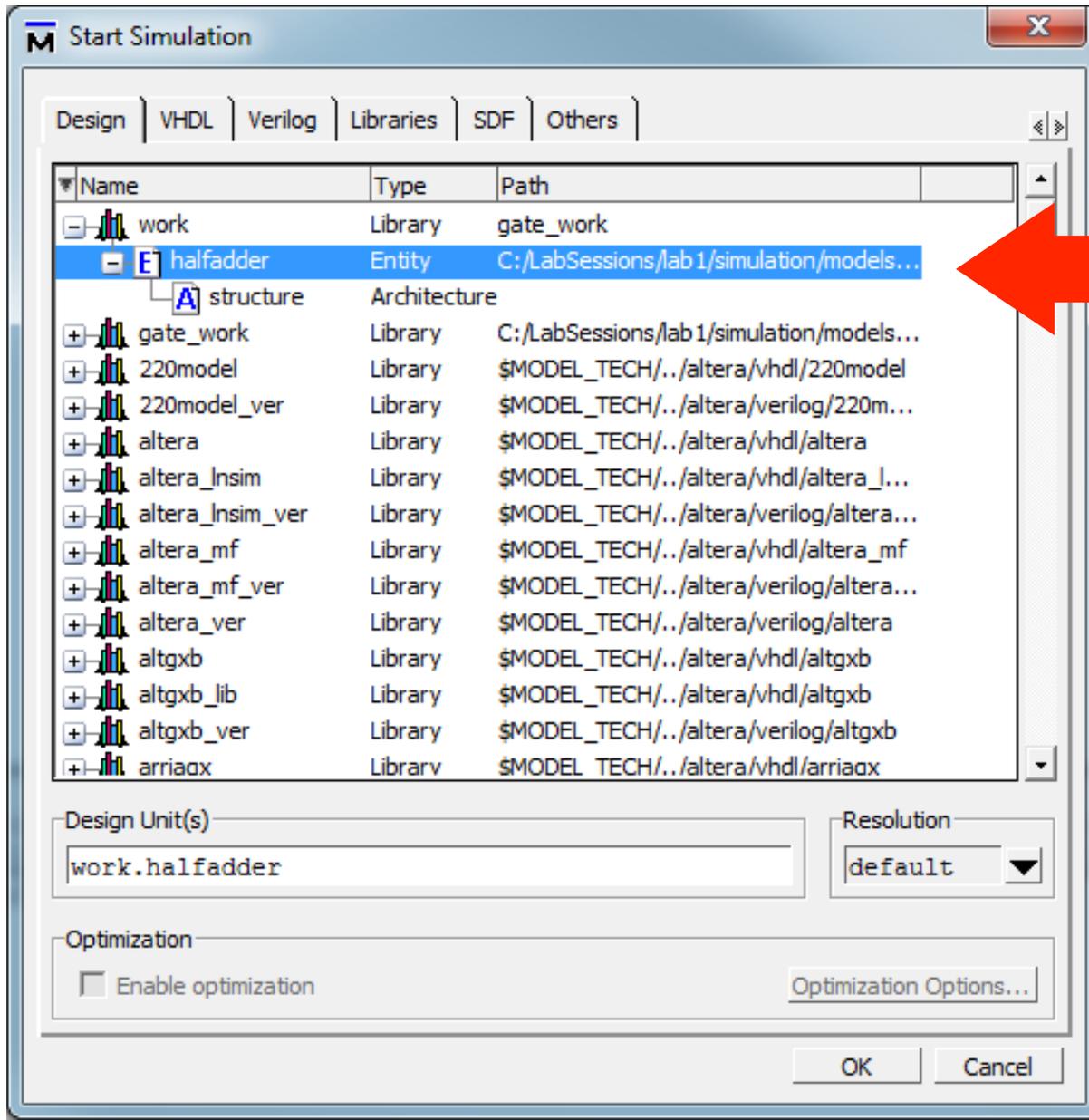
Configurar a ferramenta de simulação



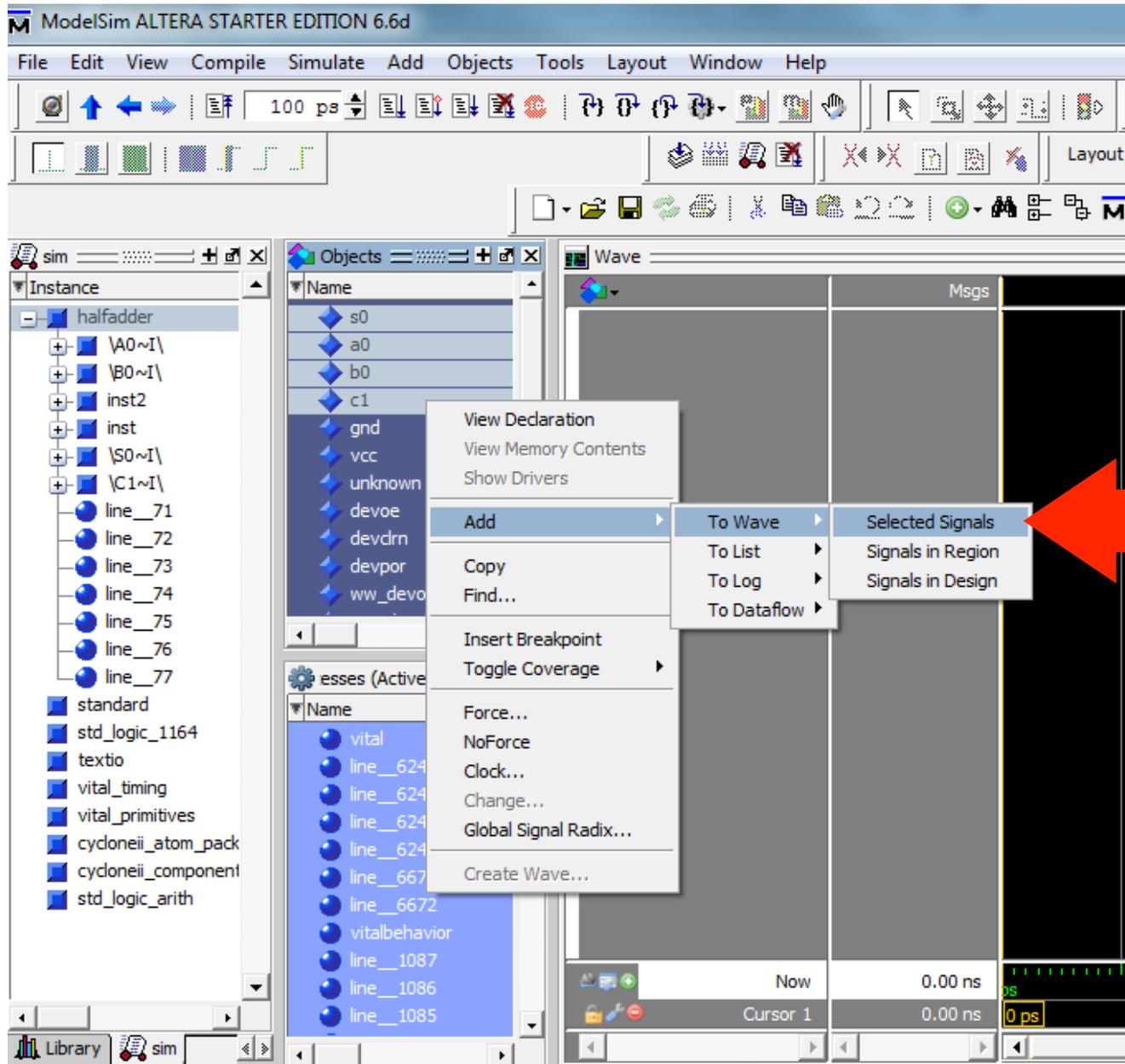
Executar o ModelSim (ferramenta de simulação)



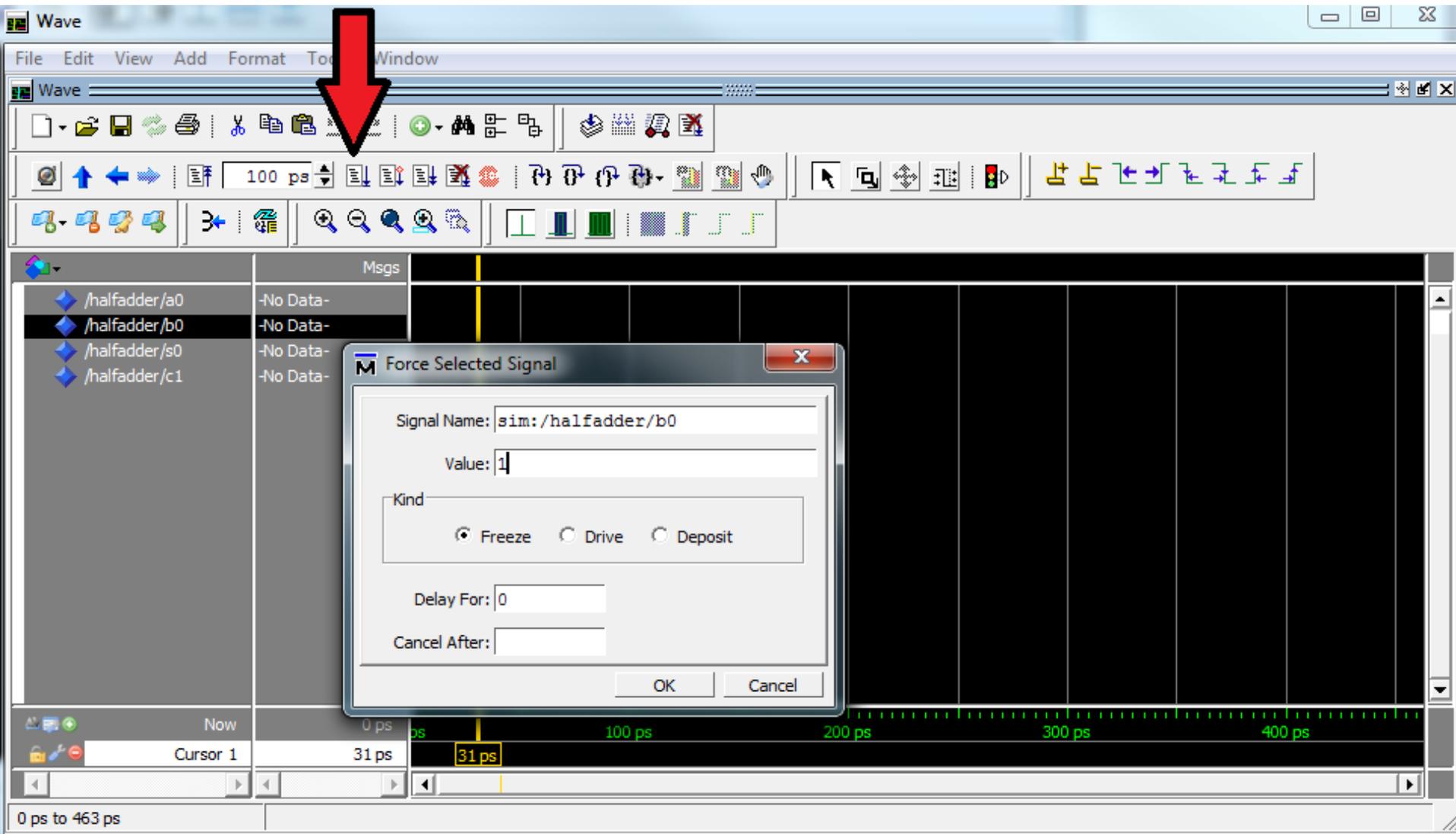
Seleccionar o módulo a ser simulado



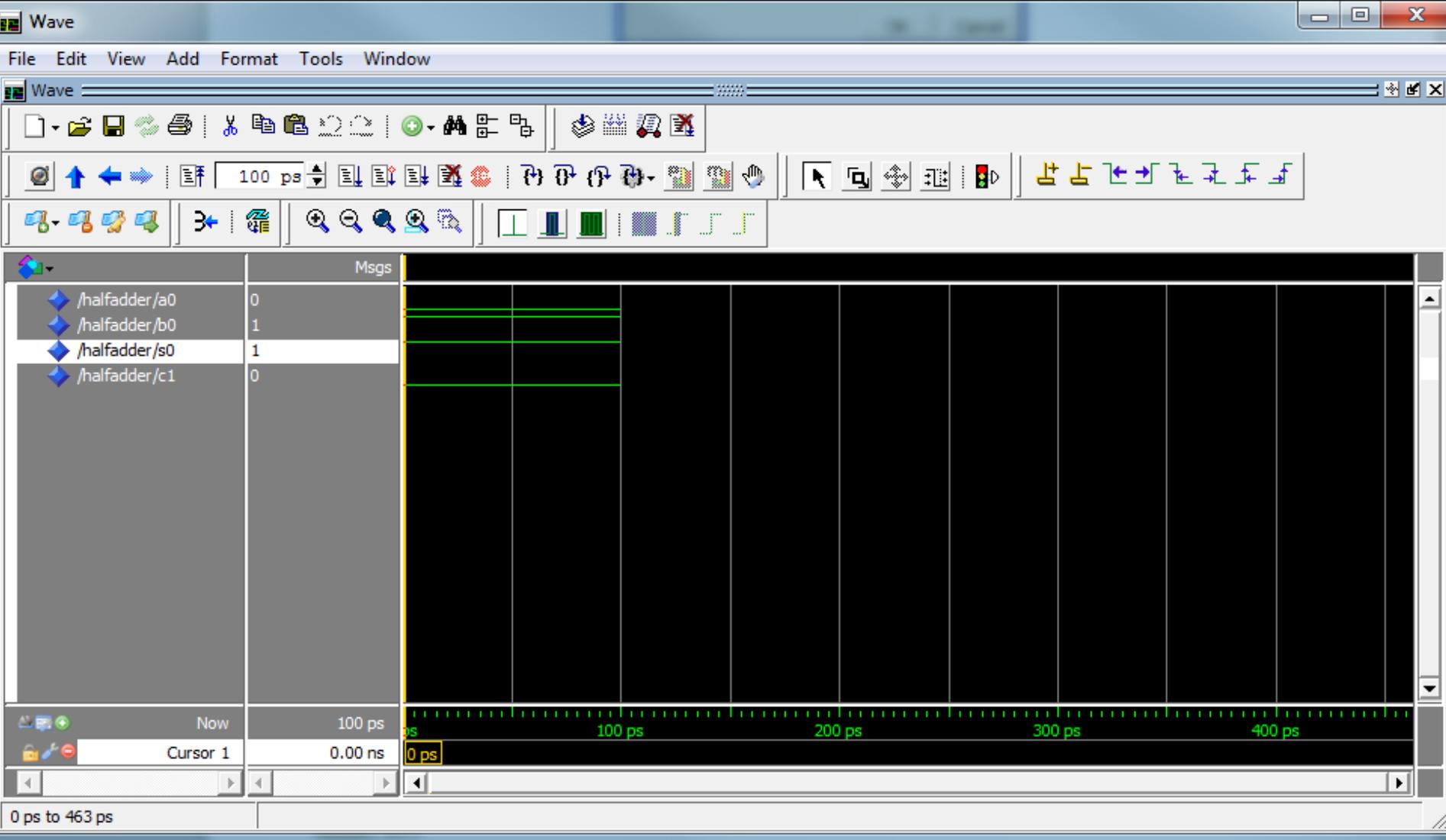
Adicionar os sinais de interesse ao diagrama de formas de onda



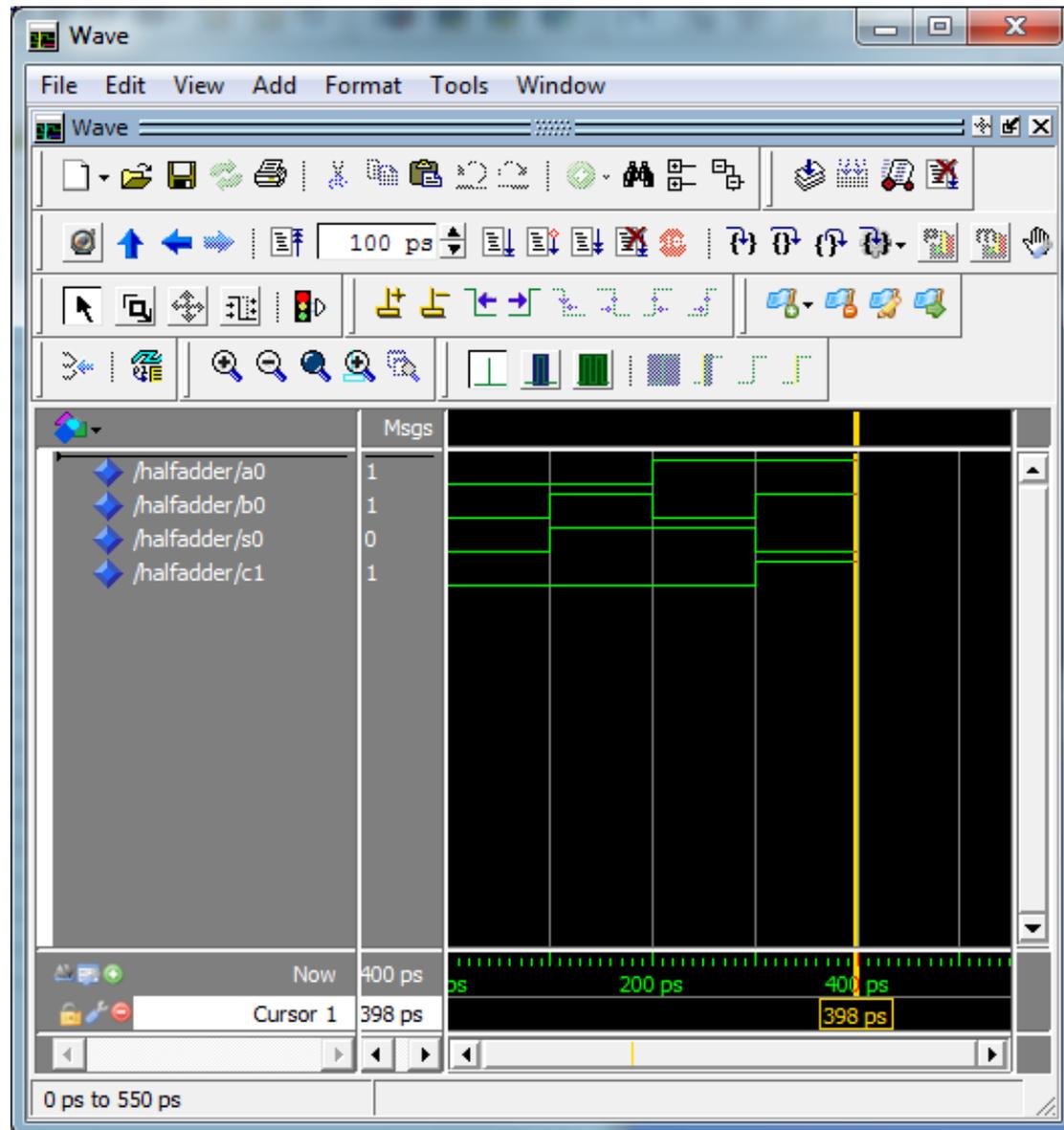
- Fixar os sinais em '0' ou '1' utilizando o botão direito do mouse sobre o sinal desejado.
- Pressionar o botão *Run* indicado na figura.



Para $A0 = '0'$ e $B0 = '1'$, o resultado da simulação será $0 + 1 = 1$ (S0), com vai-um = $'0'$ (C0).

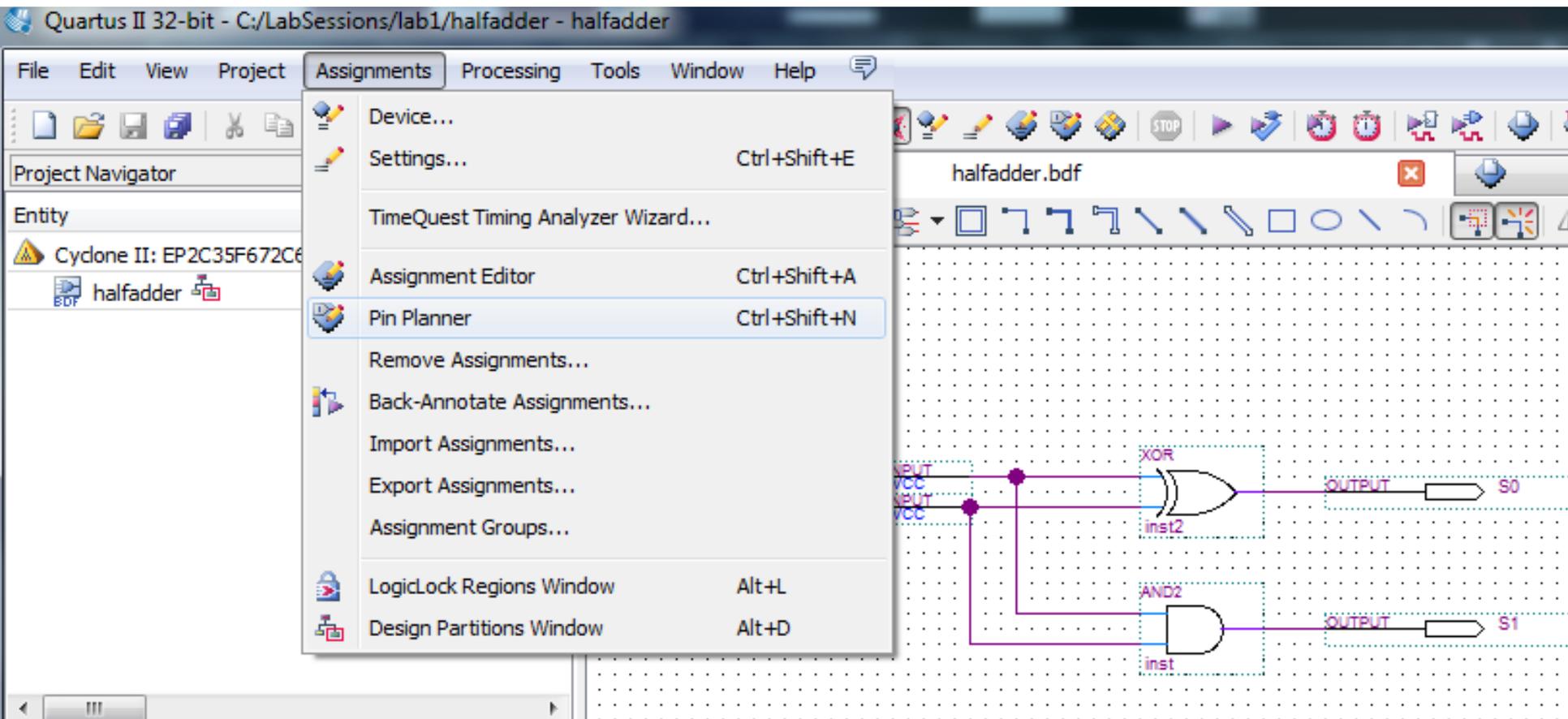


Resultado da simulação para todas as combinações de A0 e B0



Testar o circuito na placa com o FPGA

Primeiro passo, associar os pinos do FPGA aos sinais de entrada e saída definidos no projeto (esquemático).



Pinagem a ser utilizada no projeto

N25 = SW(0)

AE23 = LEDR(0)

N26 = SW(1)

AF23 = LEDR(1)

The screenshot shows the Pin Planner software interface for a Cyclone II - EP2C35F672C6 chip. The main window displays a top view of the chip with a grid of pins. The left sidebar contains various toolbars and panels, including Groups, Report, and Tasks. The bottom panel shows a table of pin assignments.

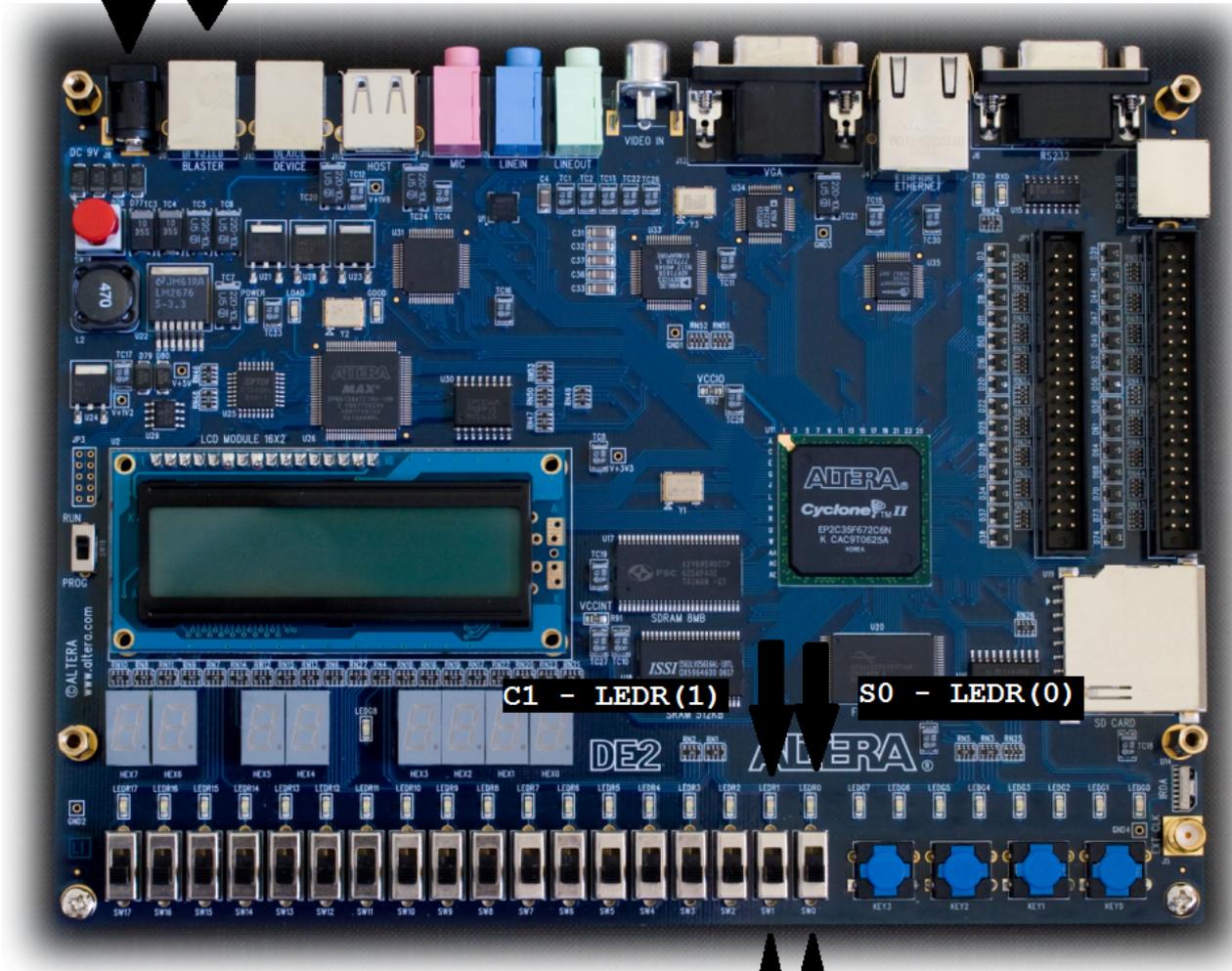
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O St
A0	Input	PIN_N25	5	B5_N1	PIN_C13	3.3-V LV..
B0	Input	PIN_N26	5	B5_N1	PIN_D13	3.3-V LV..
S0	Output	PIN_AE23	7	B7_N0	PIN_B12	3.3-V LV..
S1	Output	PIN_AF23	7	B7_N0	PIN_C11	3.3-V LV..

A placa DE2 com o FPGA da Altera

1 - 9V DC Power Supply



2 - USB Blaster



C1 - LEDR (1)

S0 - LEDR (0)



B0 - SW (1)



A0 - SW (0)

Download do arquivo de configuração para o FPGA

The screenshot displays the Altera Programmer software interface. The title bar indicates the file path: `C:/LabSessions/lab1/halfadder - halfadder - [Chain1.cdf]*`. The menu bar includes File, Edit, View, Processing, Tools, Window, and Help. A search bar for `altera.com` is present in the top right.

The hardware setup section shows `USB-Blaster [USB-0]` selected, with the mode set to `JTAG`. The progress bar indicates `100% (Successful)`. A checkbox for `Enable real-time ISP to allow background programming (for MAX II and MAX V devices)` is currently unchecked.

The main table lists the programming details:

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
<code>output_files/halfadder.sof</code>	<code>EP2C35F672</code>	<code>002F8B53</code>	<code>FFFFFFFF</code>	<input checked="" type="checkbox"/>	<input type="checkbox"/>					

On the left side, there is a vertical toolbar with buttons for `Start`, `Stop`, `Auto Detect`, `Delete`, `Add File...`, `Change File...`, `Save File`, `Add Device...`, `Up`, and `Down`.

At the bottom, a diagram shows the `ALTERA EP2C35F672` device with `TDI` (Test Data In) and `TDO` (Test Data Out) connections.