



Universidade Federal de Santa Catarina
Centro Tecnológico – CTC
Departamento de Engenharia Elétrica



“EEL7020 – Sistemas Digitais”

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“Desenvolvimento de Sistemas Digitais com FPGAs”

Material utilizado no Lab 1:

- lab1_FPGAs.ppt
- DE2_introduction.pdf
- DE2_UserManual.pdf
- Capítulo 1 do livro texto

Roteiro da aula

1. Apresentação **lab1_FPGAs.ppt**
Slides 1..14, 31..33, 55..58
2. Na pasta *altera\DE2\DE2_user_manual DE2_introduction*
 - Arquivo **DE2_introduction.pdf** (*aplicações da placa*)
 - Arquivo **DE2_UserManual.pdf** (*pinagem da placa*)
3. Versão em PDF do capítulo 1 to livro texto disponível no site da disciplina
4. Seguir o tutorial COMPLETO descrito no livro texto, pois esse fluxo será utilizado em todas as aulas de laboratório do semestre.

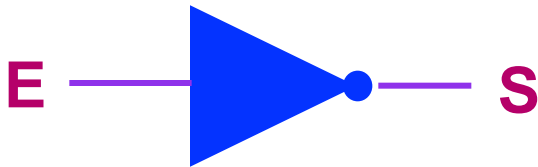
Motivação – Indústria de Circuitos Integrados

INVERSOR CMOS

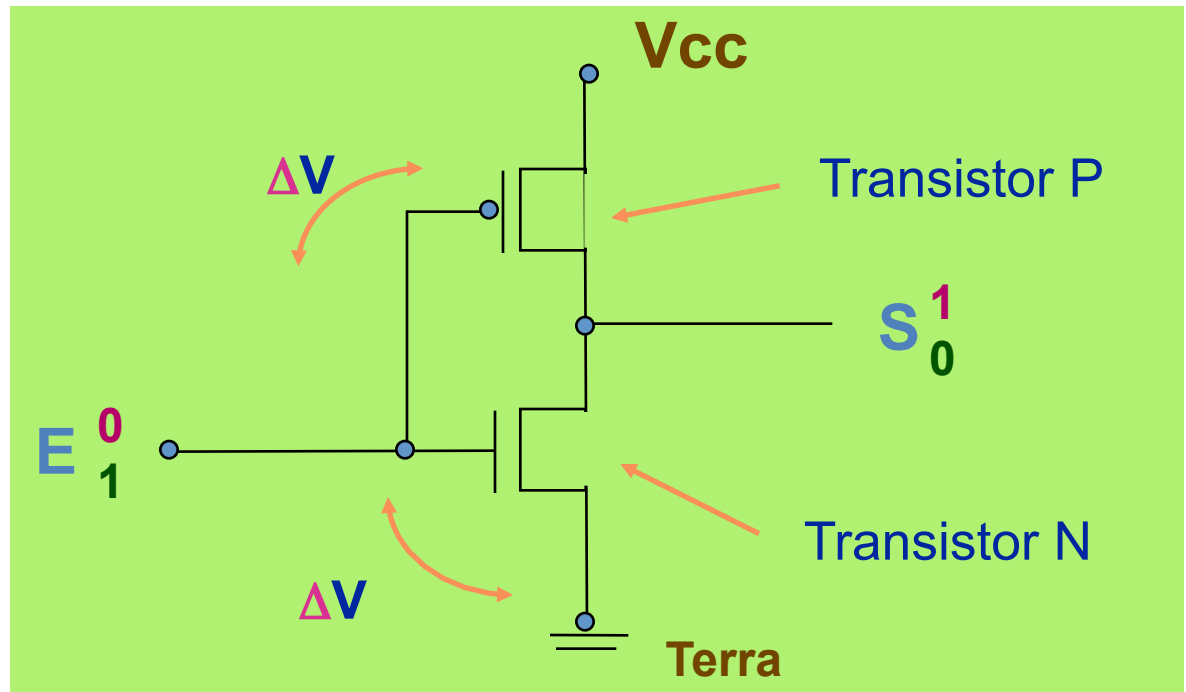
- Equação:

$$S = \overline{E}$$

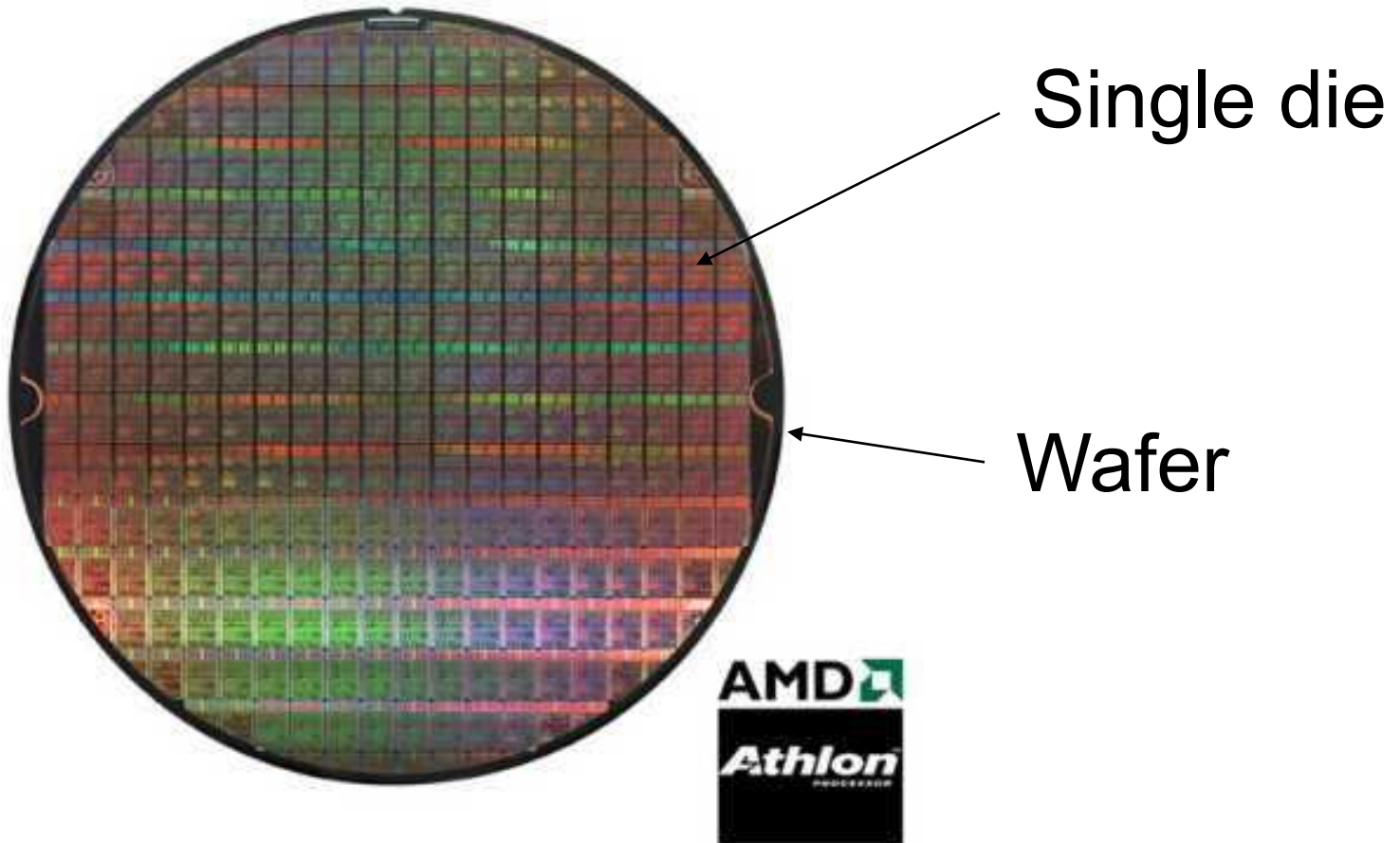
- Esquema Lógico



- Esquema Elétrico CMOS



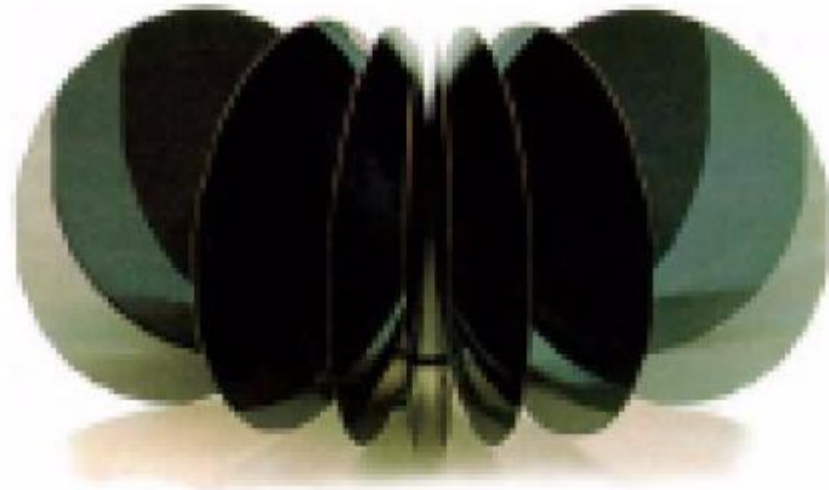
Motivação – Indústria de Circuitos Integrados



Obtido em <http://www.amd.com>

Motivação – Indústria de Circuitos Integrados

- SiO_2 , átomos de silício e oxigênio ligados por seus elétrons.
- O_2 é retirado em laboratório, e os átomos de silício resultantes formam cristal de silício puro.
- Próximo ao zero absoluto, os elétrons de silício se ocupam apenas em manter a estrutura do cristal.
- Aumentando para temperatura ambiente, átomos de Si vibram o suficiente para gerar energia térmica possibilitando seus elétrons saltar para camada de condução.
- Cristal de Silício a ser “fatiado”. Diâmetro varia de 10 a 30 cm.
- Wafers de silício (fatias) com espessura em torno de 1mm.



Tecnologia CMOS: fabricação

Processo de fotolitografia

- Depósito de produto químico (se altera na presença de luz) na superfície do chip;
- Com lente micro, luz altera regiões do material com produto químico;
- Solvente remove regiões alteradas;
- Regiões não atingidas pela luz permanecem, formando transistores;
- Processo se repete, com outros produtos, formando também isoladores e conexões.

Remoção do revestimento foto-resistivo (ashing)

Outras etapas do processo

Girar, lavar, secar (spin, rinse, dry)

Ataque ácido

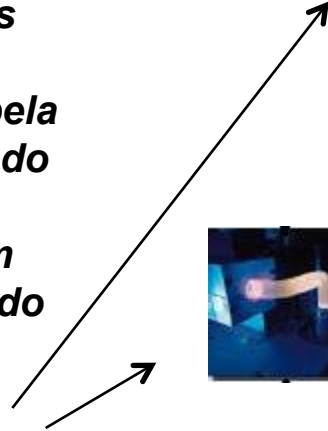
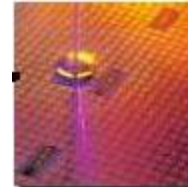
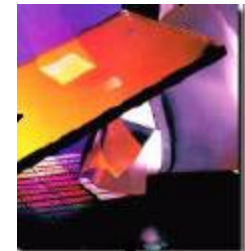
Desenvolvimento foto-resistivo

Revestimento foto-resistivo

Oxidação

Máscara Óptica

Exposição UV (stepper exposure)



Portas Lógicas Básicas e Tabela Verdade



OR

A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

S = A or B

S = A + B

S = A | B

AND

A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

S = A and B

S = A . B

S = A & B

XOR

A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

S = A xor B

S = A \oplus B

S = A ^ B

NOT

A	S
0	1
1	0

S = not A

S = \bar{A}

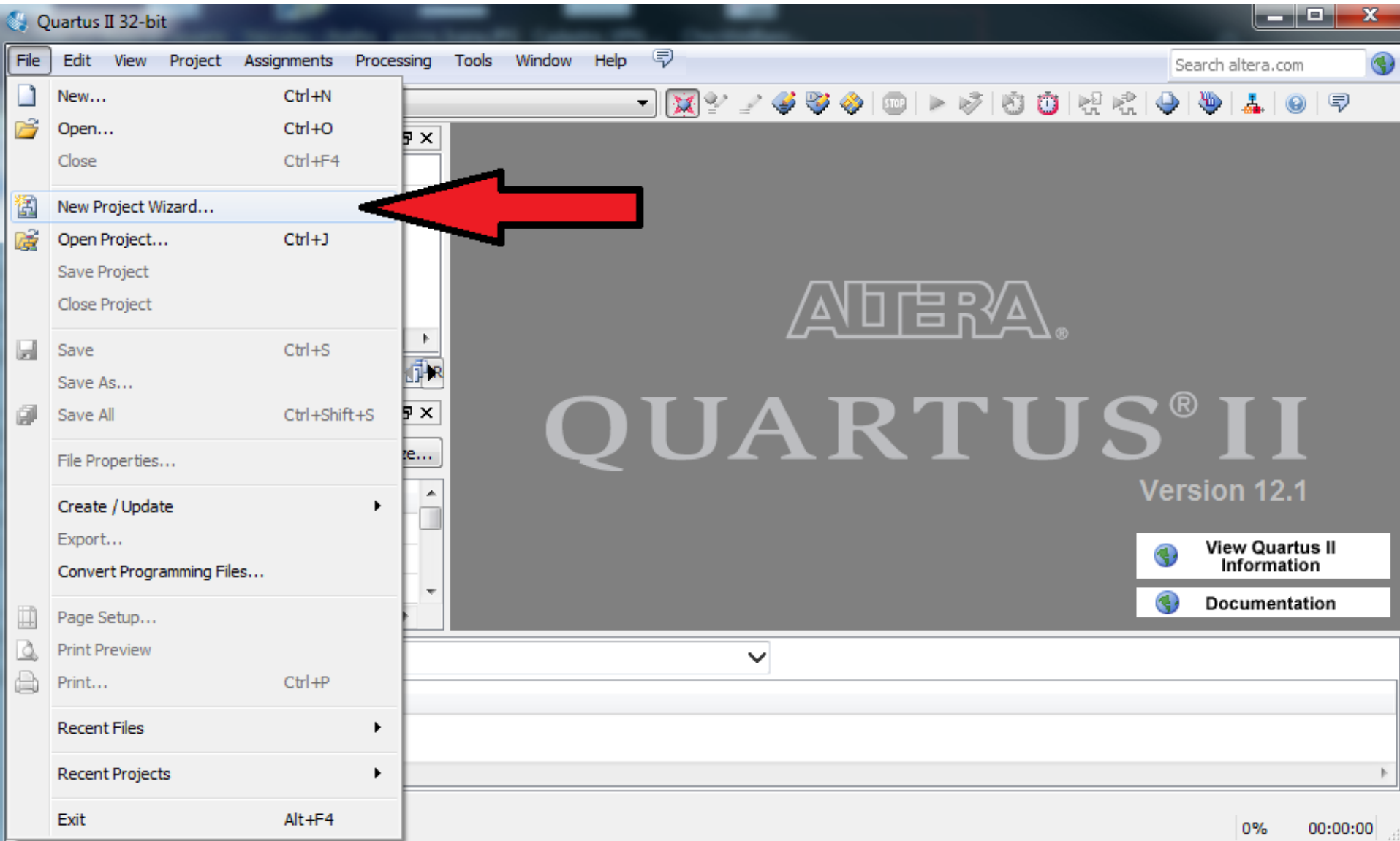
S = !A

Tarefa a ser realizada na aula prática

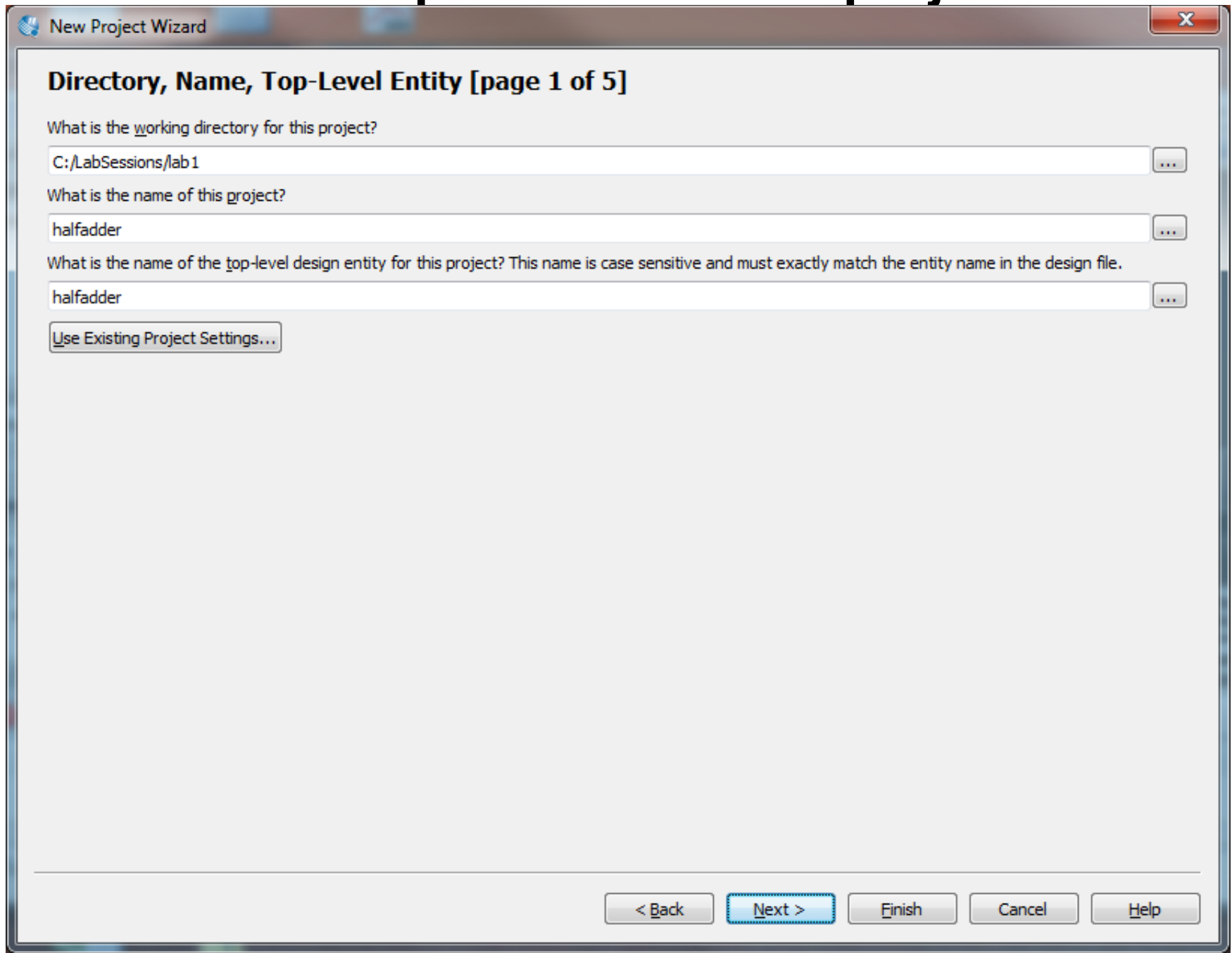
Tarefa a ser realizada na aula prática

- Utilizando a ferramenta Quartus II da Altera, criar um projeto de circuito digital (esquemático) com as 4 portas lógicas apresentadas no slide 8.
- Realizar a simulação das portas lógicas no Quartus II, e levantar a tabela verdade para cada uma das portas.
- O objetivo principal dessa aula prática é possibilitar que o aluno tenha um primeiro contato com as ferramentas de desenvolvimento a serem utilizadas durante o semestre.
- Seguir o tutorial existente na seção “Laboratory assignment” do capítulo 1 do livro texto.
- Um resumo desse tutorial está incluído nos slides a seguir.

Criar um novo projeto



Escolher a pasta e nome do projeto



The image shows a 'New Project Wizard' dialog box with a title bar containing a gear icon and the text 'New Project Wizard'. The main content area is titled 'Directory, Name, Top-Level Entity [page 1 of 5]'. It contains three text input fields with prompts: 'What is the working directory for this project?' (containing 'C:/LabSessions/lab1'), 'What is the name of this project?' (containing 'halfadder'), and 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' (containing 'halfadder'). Each field has a browse button (three dots) to its right. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom of the dialog are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a blue dashed border.

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

C:/LabSessions/lab1

What is the name of this project?

halfadder

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

halfadder

Use Existing Project Settings...

< Back Next > Finish Cancel Help

Seleccionar o dispositivo alvo (FPGA)

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone II

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter:

☒ Show advanced devices ☐ HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	al Cl
EP2C35F484C7	1.2V	33216	322	483840	70	4	16
EP2C35F484C8	1.2V	33216	322	483840	70	4	16
EP2C35F484I8	1.2V	33216	322	483840	70	4	16
EP2C35F672C6	1.2V	33216	475	483840	70	4	16
EP2C35F672C7	1.2V	33216	475	483840	70	4	16
EP2C35F672C8	1.2V	33216	475	483840	70	4	16
EP2C35F672I8	1.2V	33216	475	483840	70	4	16

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

Configurar a ferramenta de simulação

New Project Wizard

EDA Tool Settings [page 4 of 5]

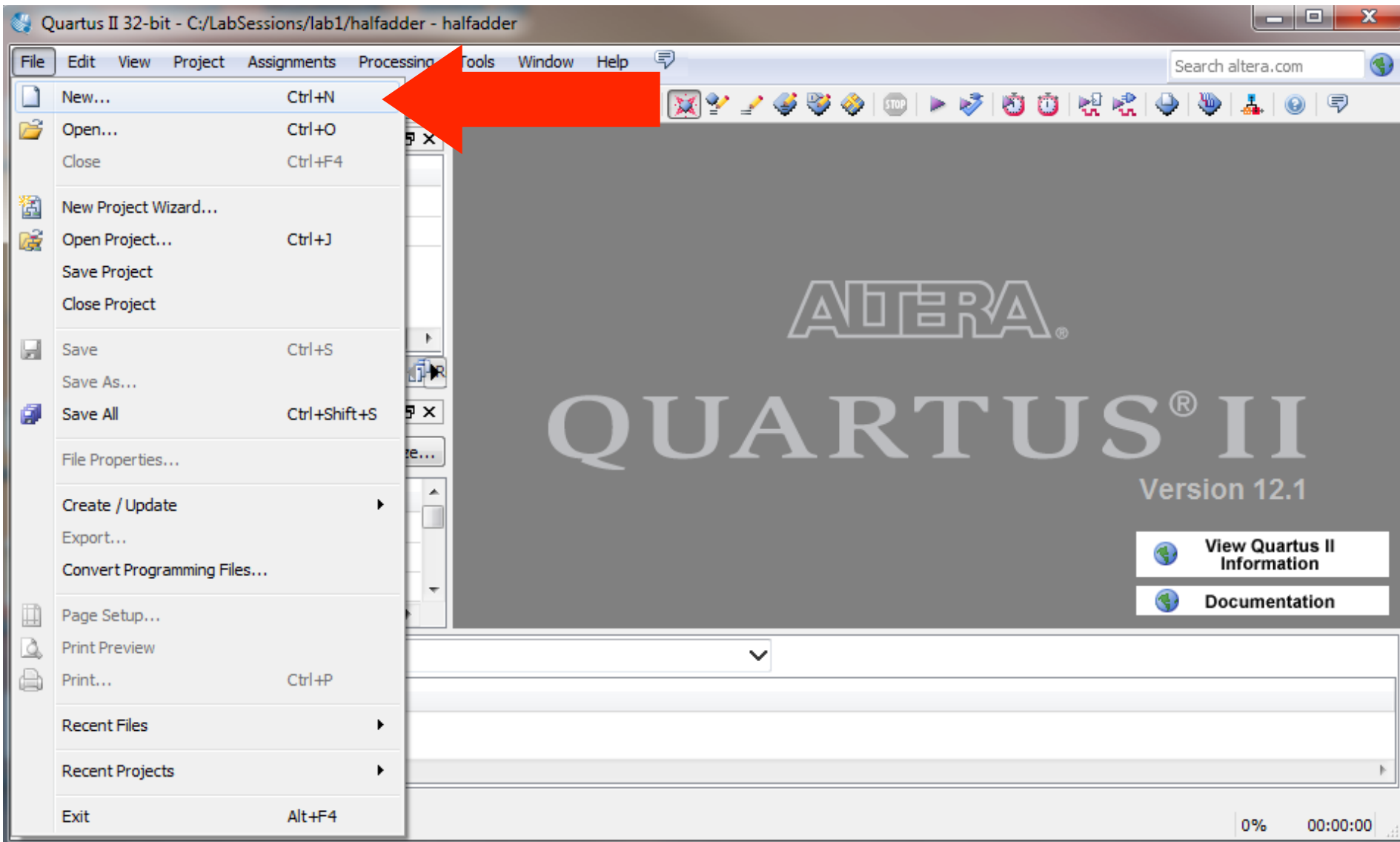
Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

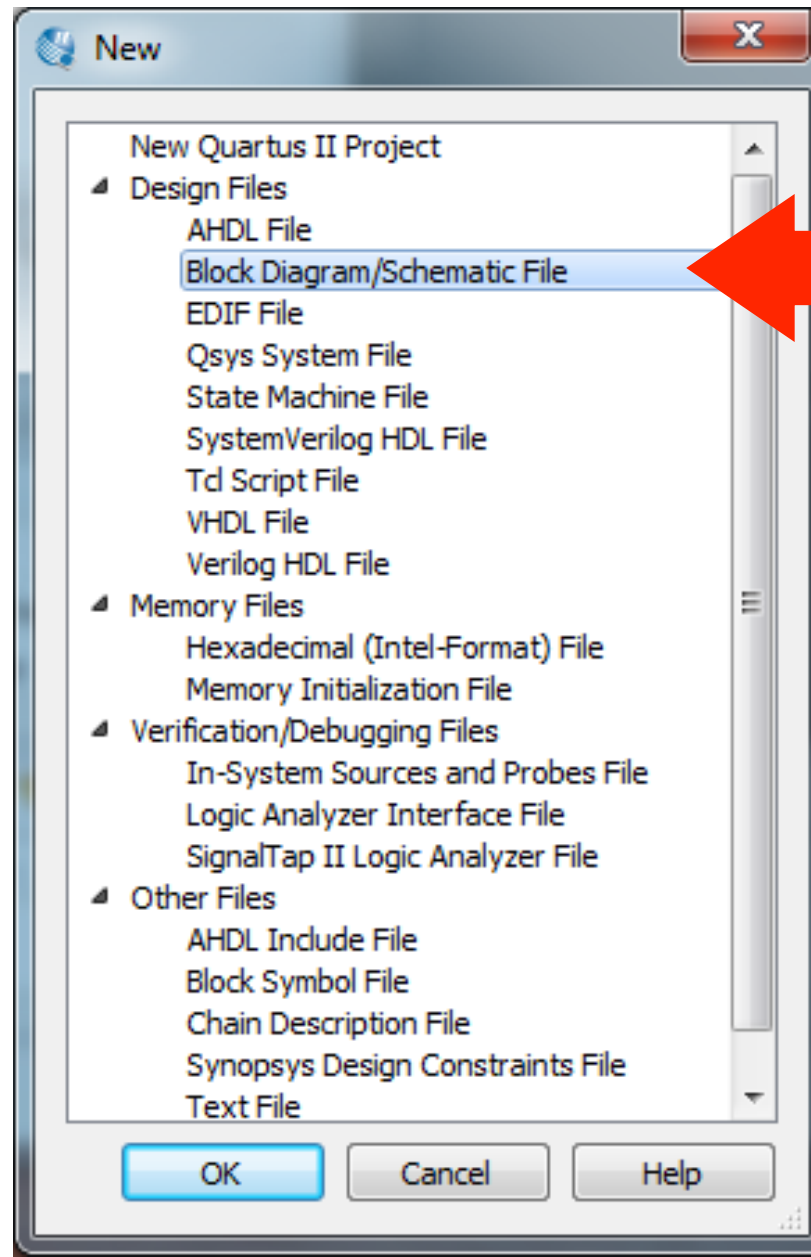
Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

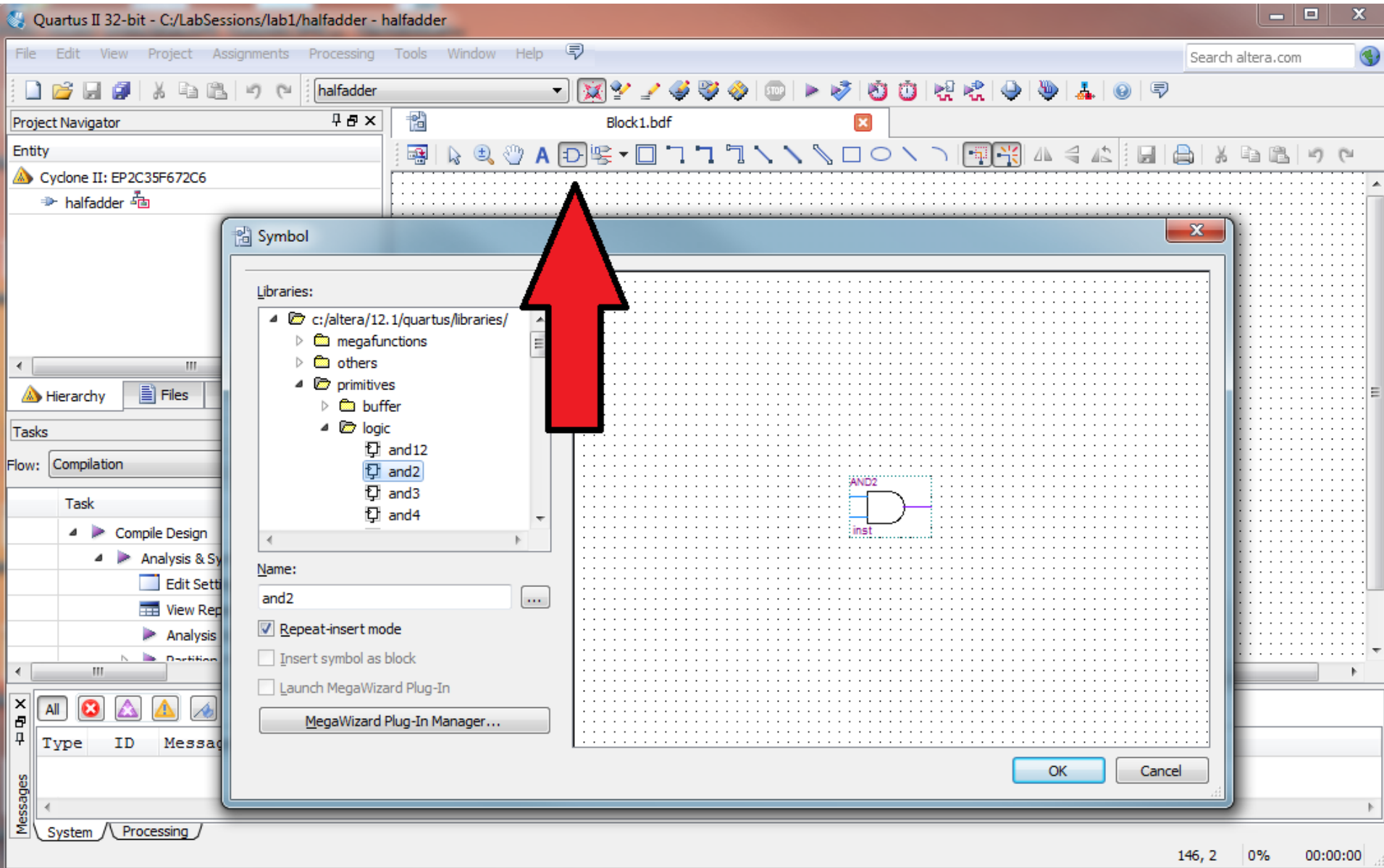
Criar um novo diagrama de esquemático



Criar um novo diagrama de esquemático



Entrar com as portas lógicas



Realizar as conexões das portas lógicas

The screenshot displays the Quartus II 32-bit IDE interface. The main workspace shows a logic circuit diagram for a half adder. The circuit consists of two input signals, A0 and B0, which are connected to an XOR gate (inst2) and an AND gate (inst). The output of the XOR gate is connected to the output of the AND gate. A red arrow points to the connection point between the two gates. The interface includes a Project Navigator on the left, a Tasks pane, and a Messages pane at the bottom.

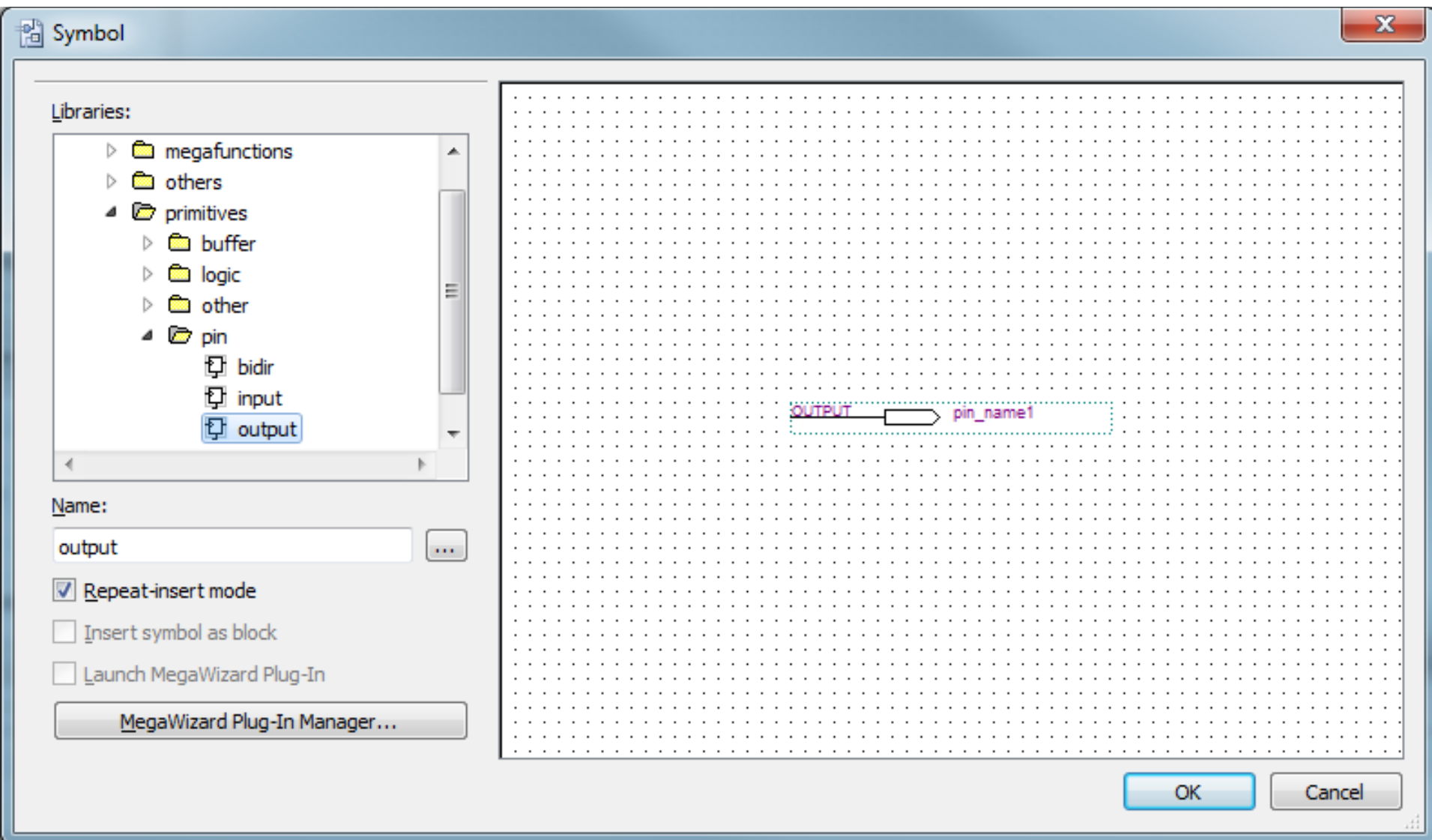
Project Navigator: Entity: Cydome II: EP2C35F672C6, halfadder

Tasks: Flow: Compilation, Customize... Task: Compile Design, Analysis & Synthesis, Edit Settings, View Report, Analysis & Elaboration, Partition Merge

Messages: System, Processing

320,9 0% 00:00:00

Entrar com os pinos de entrada e saída



Conectar os pinos de entrada e saída e as portas lógicas

The screenshot displays the Quartus II 32-bit IDE interface for a project named "halfadder" located at "C:/LabSessions/lab1/halfadder". The main workspace shows a logic circuit diagram for a half adder, titled "Block1.bdf*".

Project Navigator (Left Panel):

- Entity:** Cystone II: EP2C35F672C6
- halfadder** (selected)
- Tasks:** Compile Design, Analysis & Synthesis, Edit Settings, View Report, Analysis & Elaboration, Partition Merge.

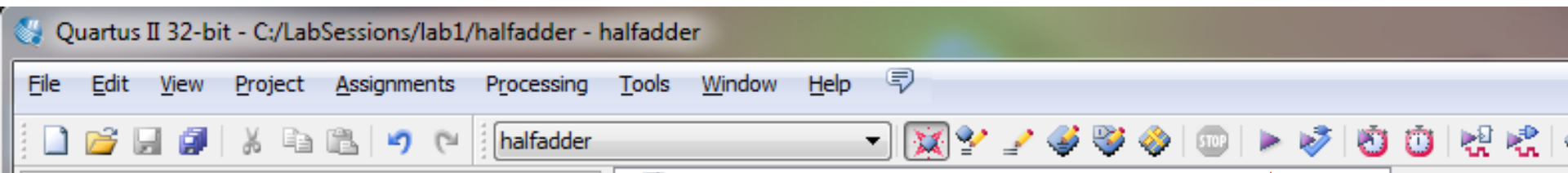
Logic Circuit Diagram (Main Workspace):

- Inputs:** A0 and B0 are connected to the inputs of the logic gates.
- Logic Gates:** An XOR gate (labeled "inst2") and an AND gate (labeled "inst1") are used.
- Outputs:** The XOR gate output is connected to a pin labeled "S0". The AND gate output is connected to a pin labeled "pin_name2".

Messages Panel (Bottom):

- System / Processing:** The status bar shows "727,246 0% 00:00:00".

Realizar a síntese do circuito (*compile*)



Configurar a ferramenta de simulação

The screenshot displays the Quartus II 32-bit IDE interface. The 'Tools' menu is open, and the 'Options...' option is highlighted. A large red arrow points to this option. The background shows a 'Compilation Report - halfadder' window with a 'Summary' section indicating a successful compilation.

Compilation Report - halfadder

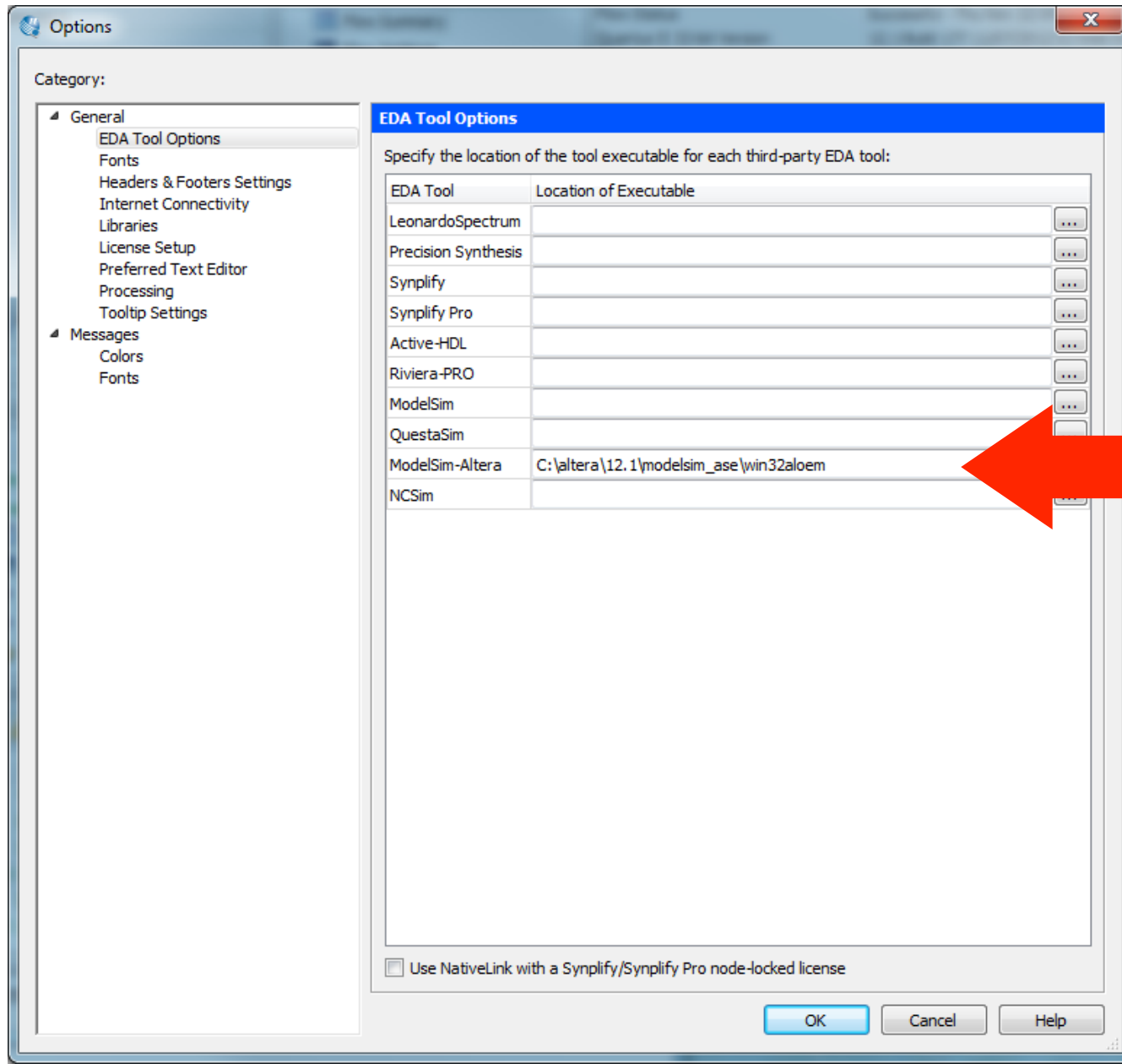
Summary	
Status	Successful - Thu Nov 22 09:17:35 2012
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Project Name	halfadder
Target Device	halfadder
Device Family	Cyclone II
Device Part	EP2C35F672C6
Model	Final
Logic elements	2 / 33,216 (< 1 %)
Combinational functions	2 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Registers	0
Pins	4 / 475 (< 1 %)
Virtual pins	0
Memory bits	0 / 483,840 (0 %)
Added Multiplier 9-bit elements	0 / 70 (0 %)
PLLs	0 / 4 (0 %)

Messages

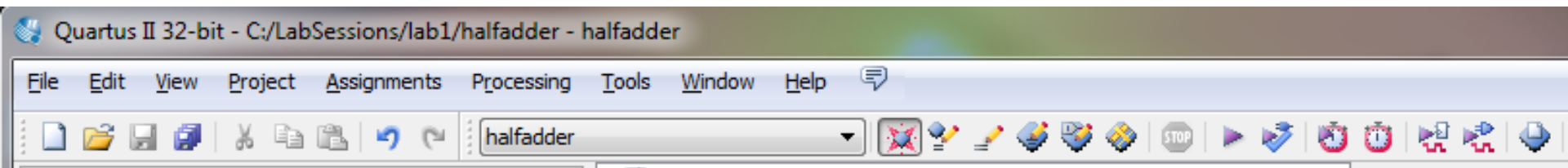
Type	ID	Message
Info		*****
Info		Running Quartus II 32-bit EDA Netlist Writer
Info		Command: quartus_eda --read_settings_files=off --write_settings_files=off halfadder -c halfadder
Info	204026	Generated files "halfadder.vho", "halfadder_fast.vho", "halfadder_vhd.sdo" and "halfadder_vhd_fast.sdo" in directory "C:/LabSes.
Info		Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	293000	Quartus II Full Compilation was successful. 0 errors, 8 warnings

Changes user preferences and options

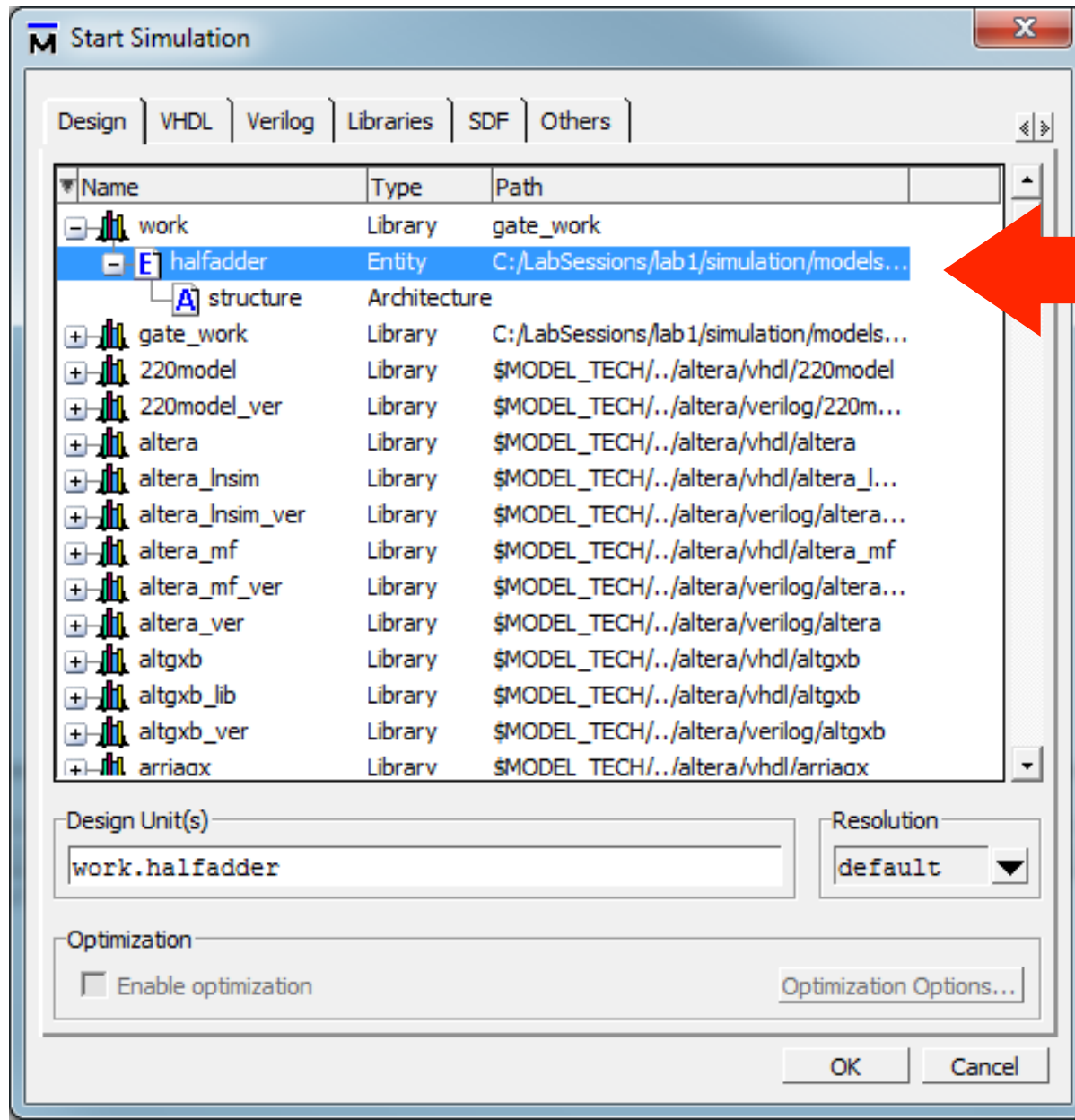
Configurar a ferramenta de simulação



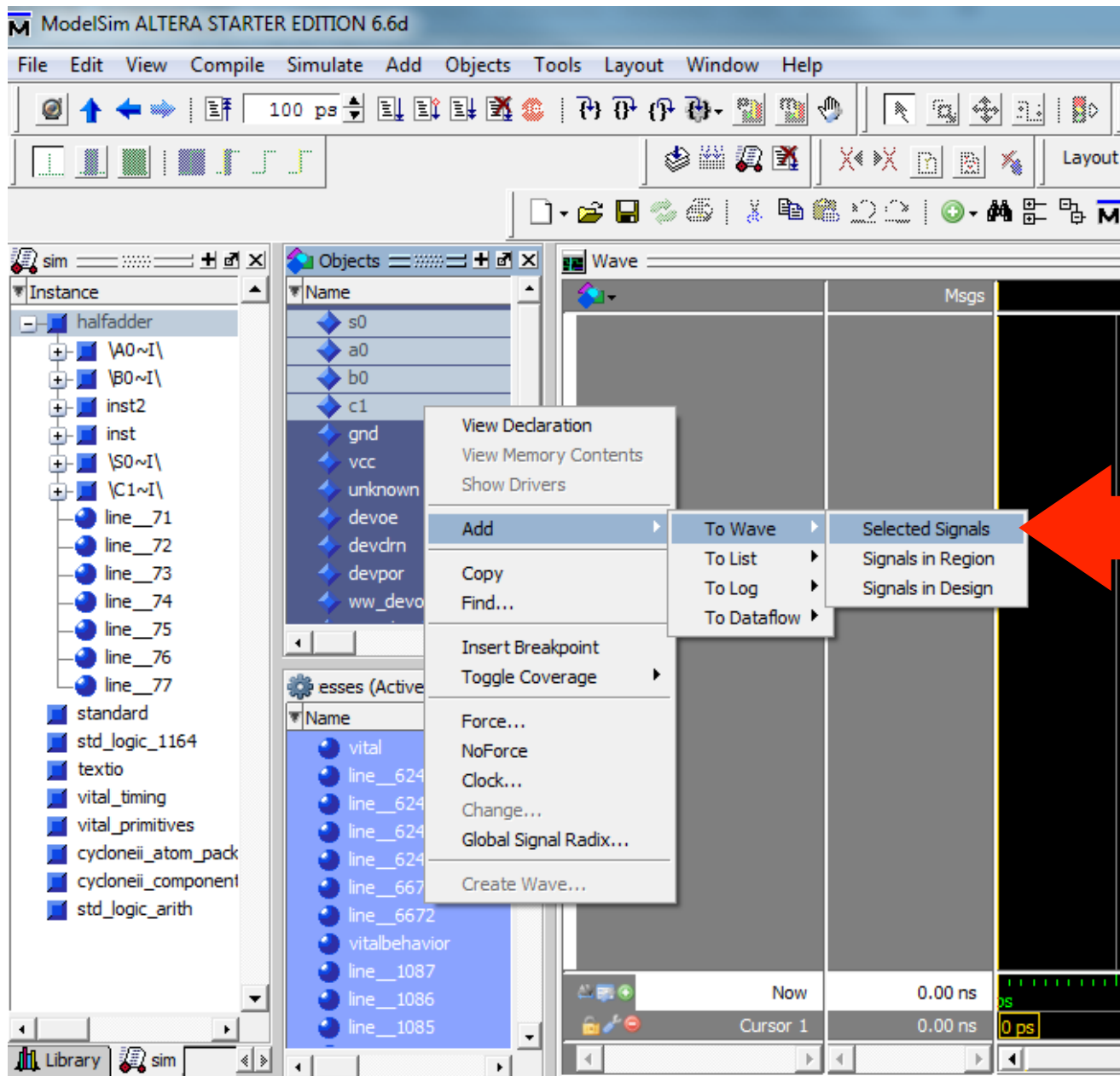
Executar o ModelSim (ferramenta de simulação)



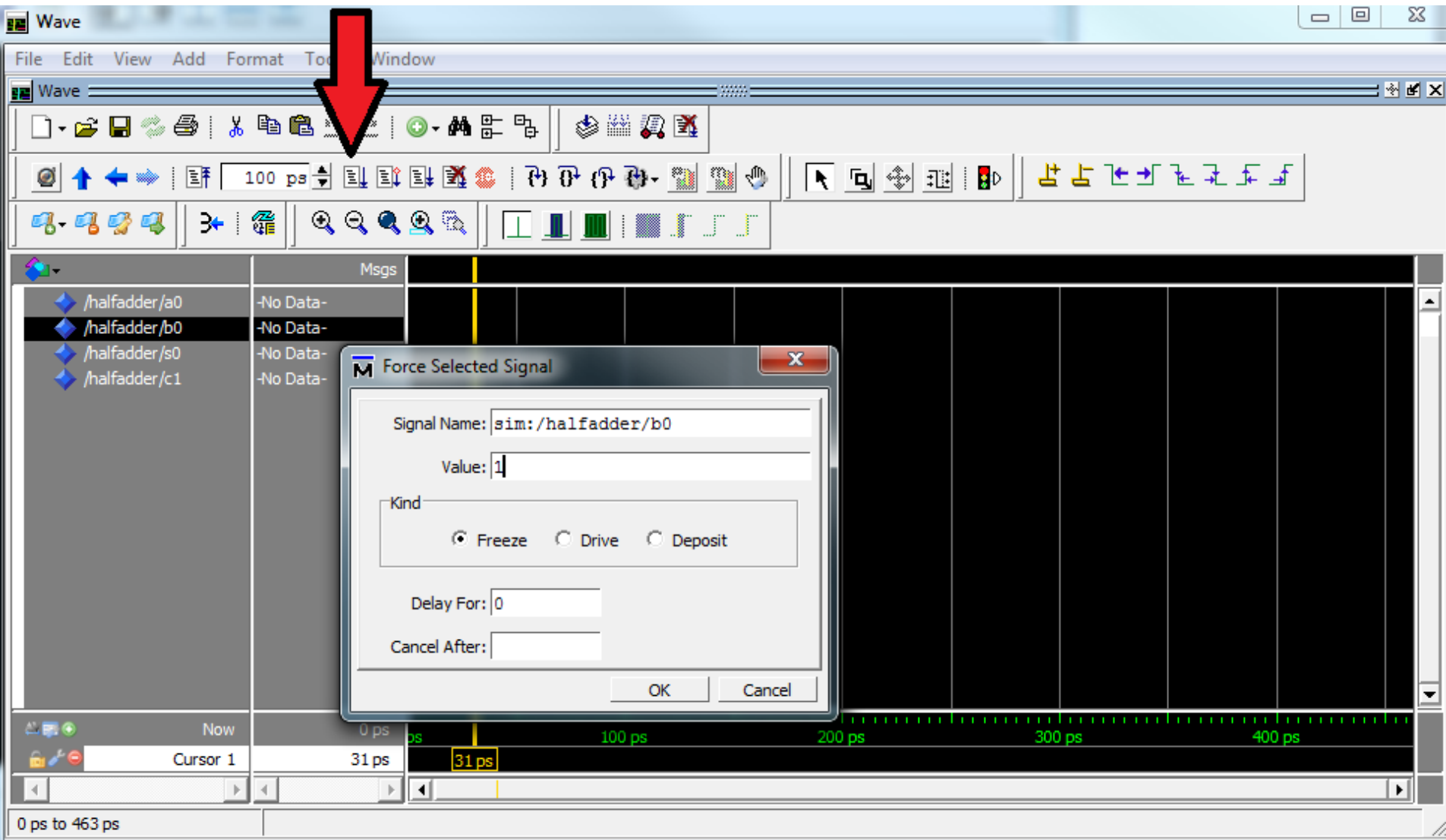
Selecionar o módulo a ser simulado



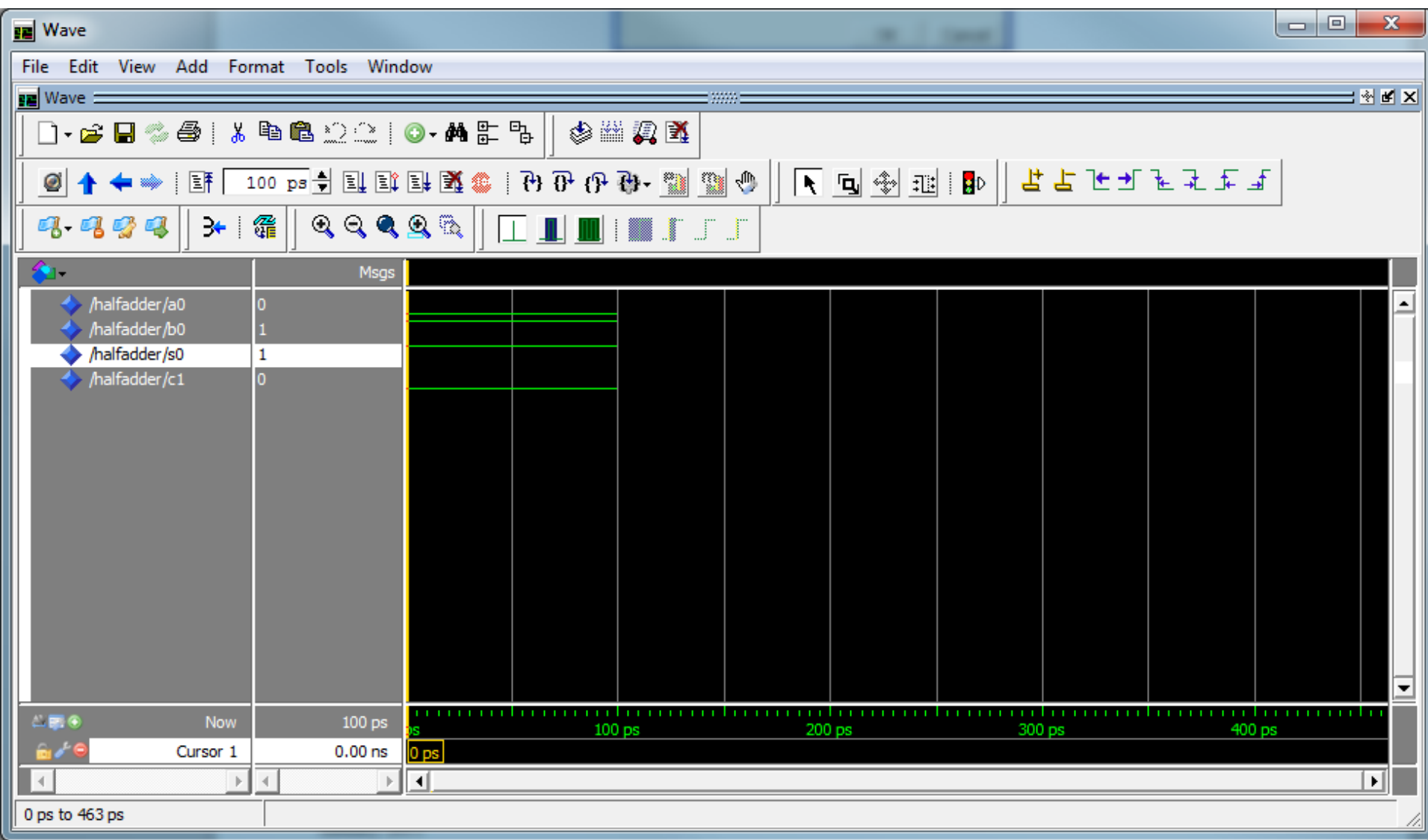
Adicionar os sinais de interesse ao diagrama de formas de onda



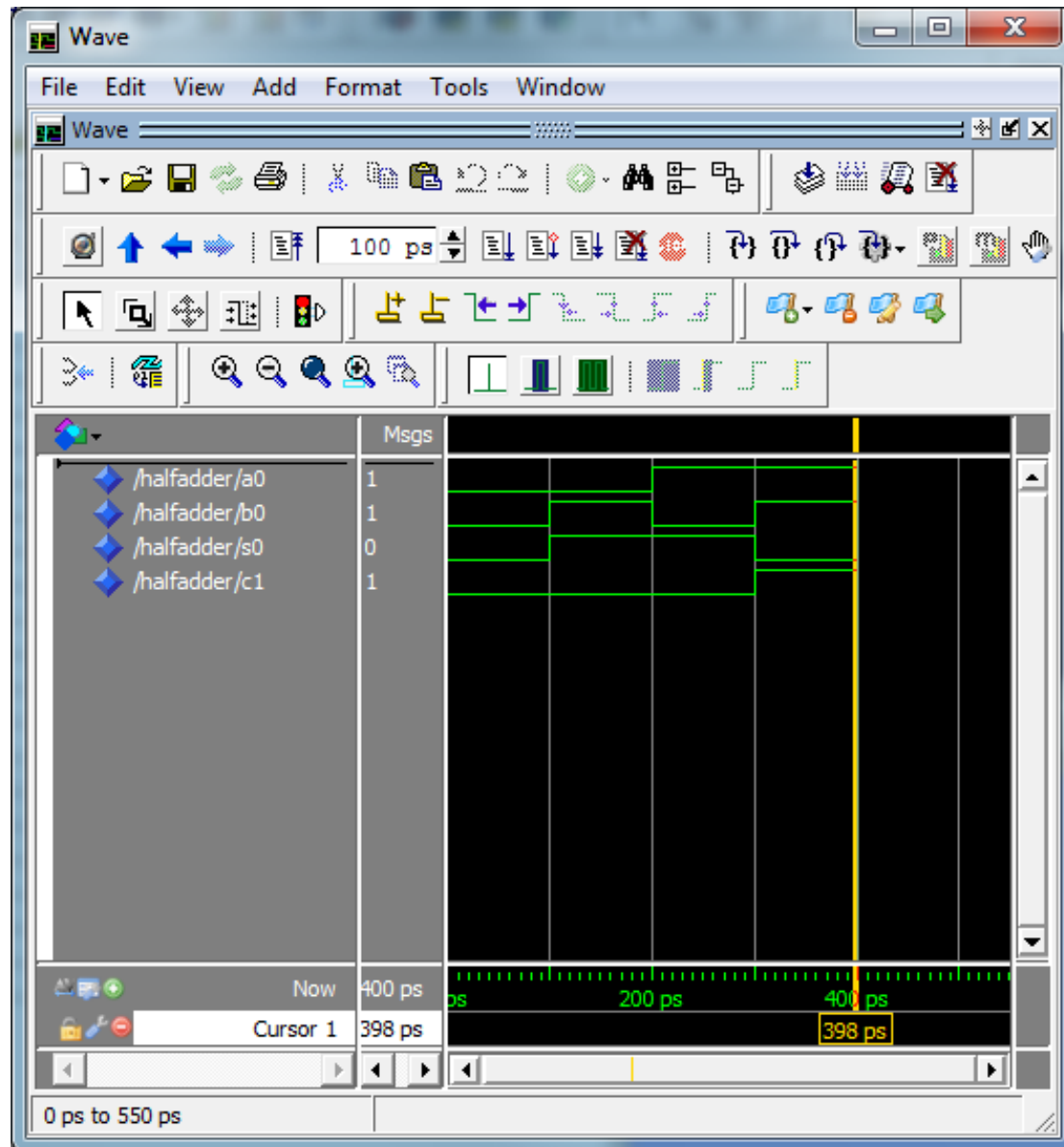
- Fixar os sinais em '0' ou '1' utilizando o botão direito do mouse sobre o sinal desejado.
- Pressionar o botão *Run* indicado na figura.



Para $A0 = '0'$ e $B0 = '1'$, o resultado da simulação será $0 + 1 = 1$ (S0), com vai-um = $'0'$ (C0).

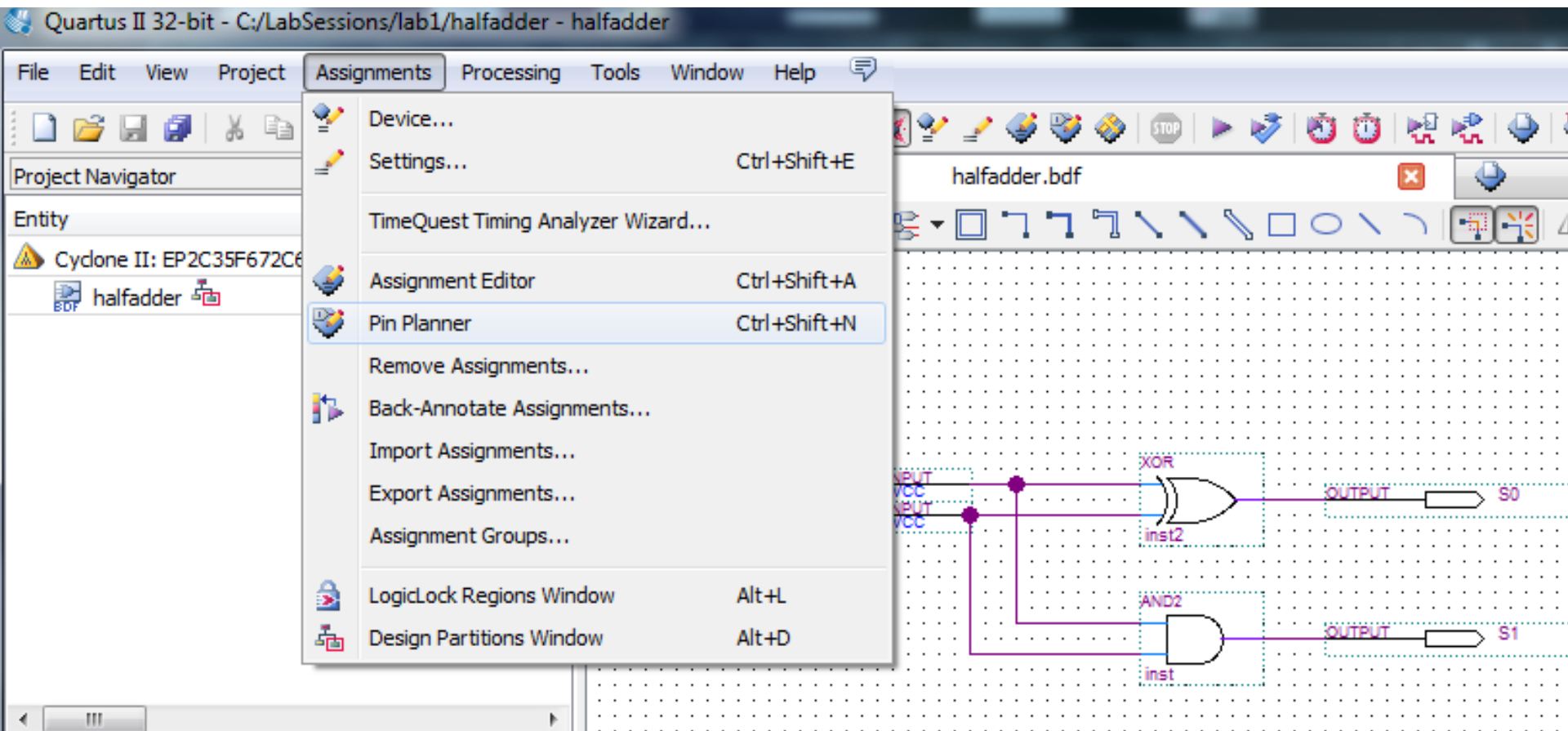


Resultado da simulação para todas as combinações de A0 e B0



Testar o circuito na placa com o FPGA

Primeiro passo, associar os pinos do FPGA aos sinais de entrada e saída definidos no projeto (esquemático).



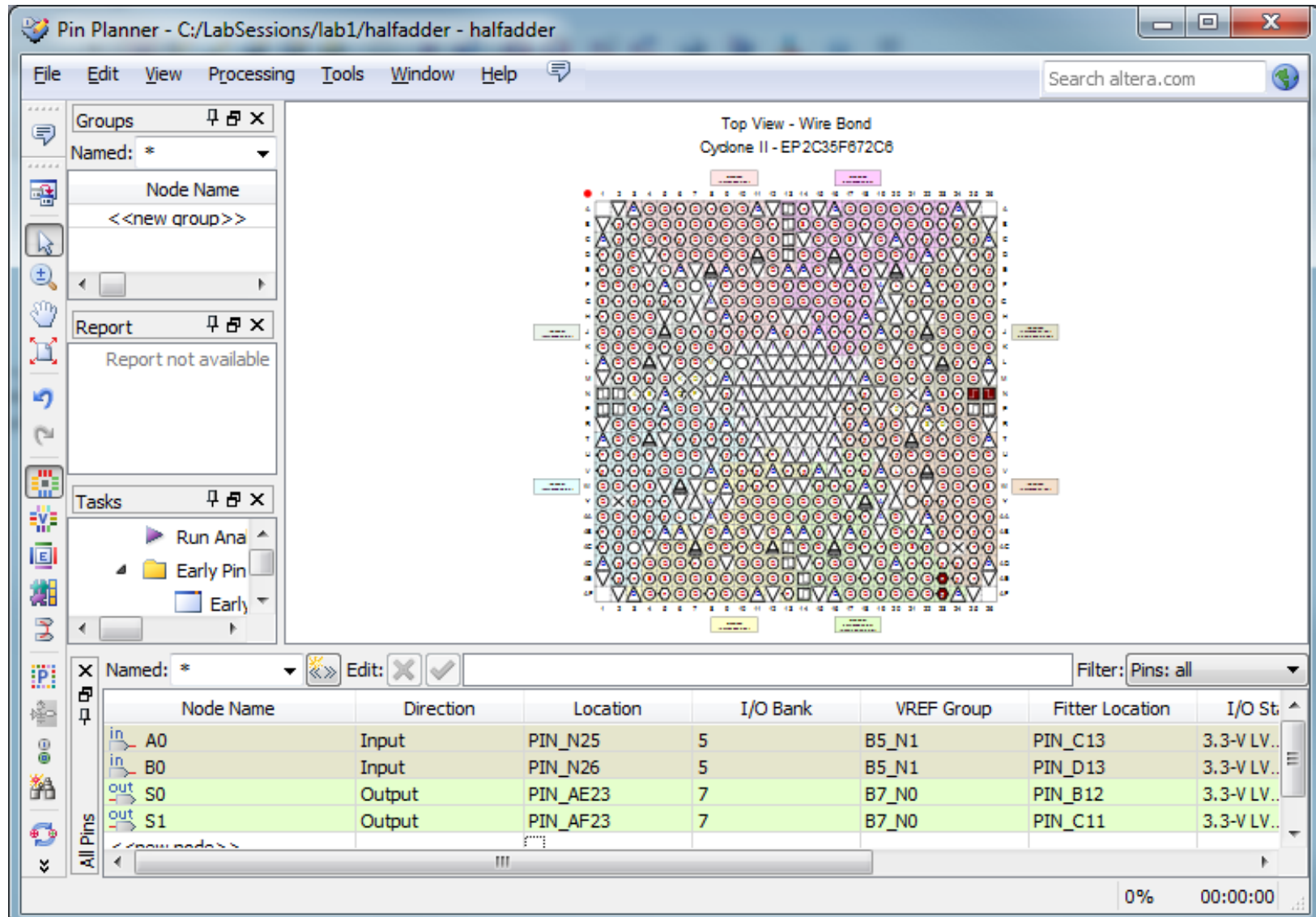
Pinagem a ser utilizada no projeto

N25 = SW(0)

AE23 = LEDR(0)

N26 = SW(1)

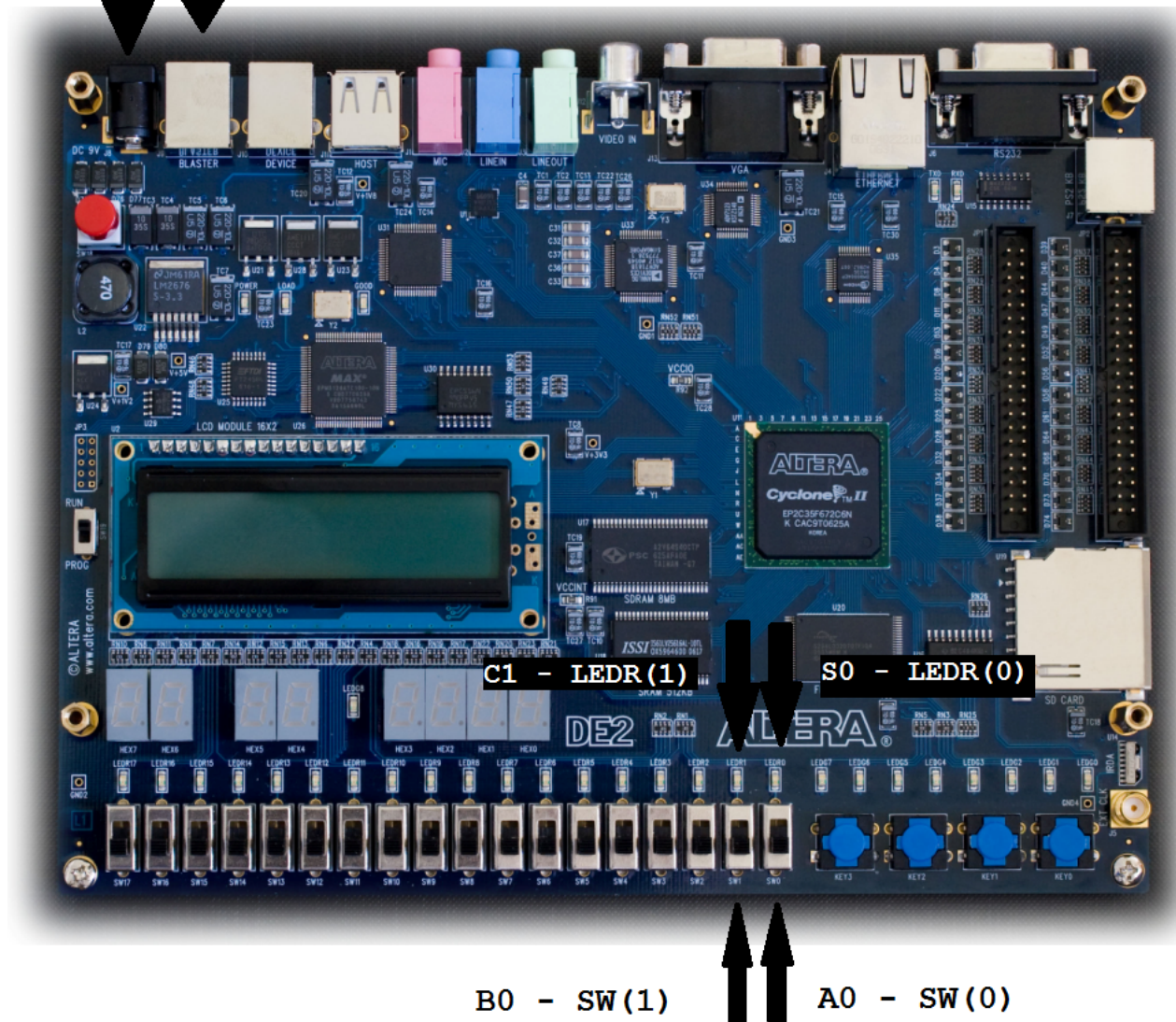
AF23 = LEDR(1)



A placa DE2 com o FPGA da Altera

1 - 9V DC Power Supply

2 - USB Blaster



Download do arquivo de configuração para o FPGA

