



Universidade Federal de Santa Catarina
Centro Tecnológico – CTC
Departamento de Engenharia Elétrica



“EEL5105 – Circuitos e Técnicas Digitais”

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“EEL 5105 – Circuitos e Técnicas Digitais”

Fluxo de projeto – Quartus II

“Desenvolvimento de Sistemas Digitais com FPGAs”

Material utilizado no Lab 1:

- lab1_FPGAs.ppt
- DE1-SoC_User_manual_0C0D.pdf
- Capítulo 1 do livro texto

Roteiro da aula

1. Apresentação **lab1_FPGAs.ppt**
Slides 1..14, 31..33, 55..58
2. Documentação do kit de desenvolvimento, incluindo informações de pinagem disponível em:
 - **DE1-SoC_User_manual_0C0D.pdf**
3. Versão em PDF do capítulo 1 do livro texto disponível no site da disciplina
4. Seguir o tutorial **COMPLETO** descrito no livro texto e nessa apresentação, pois esse fluxo de projeto será utilizado em todas as aulas de laboratório do semestre.

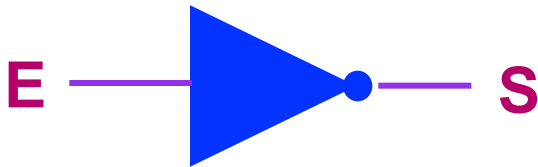
Motivação – Indústria de Circuitos Integrados

INVERSOR CMOS

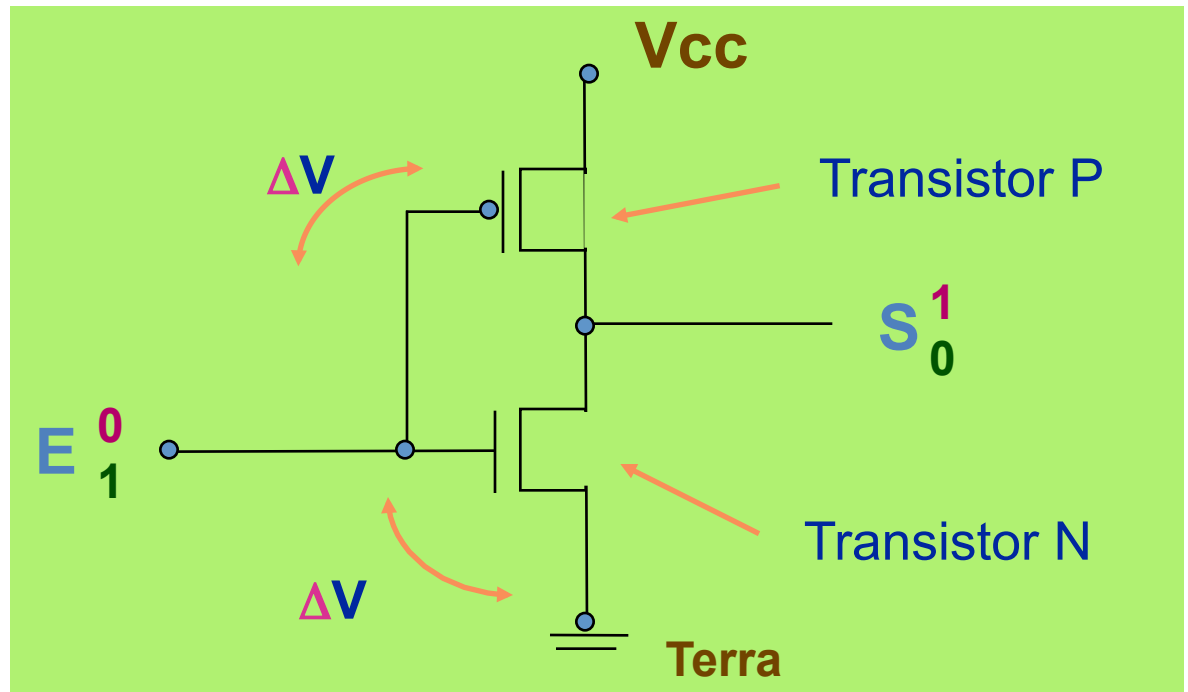
- Equação:

$$S = \overline{E}$$

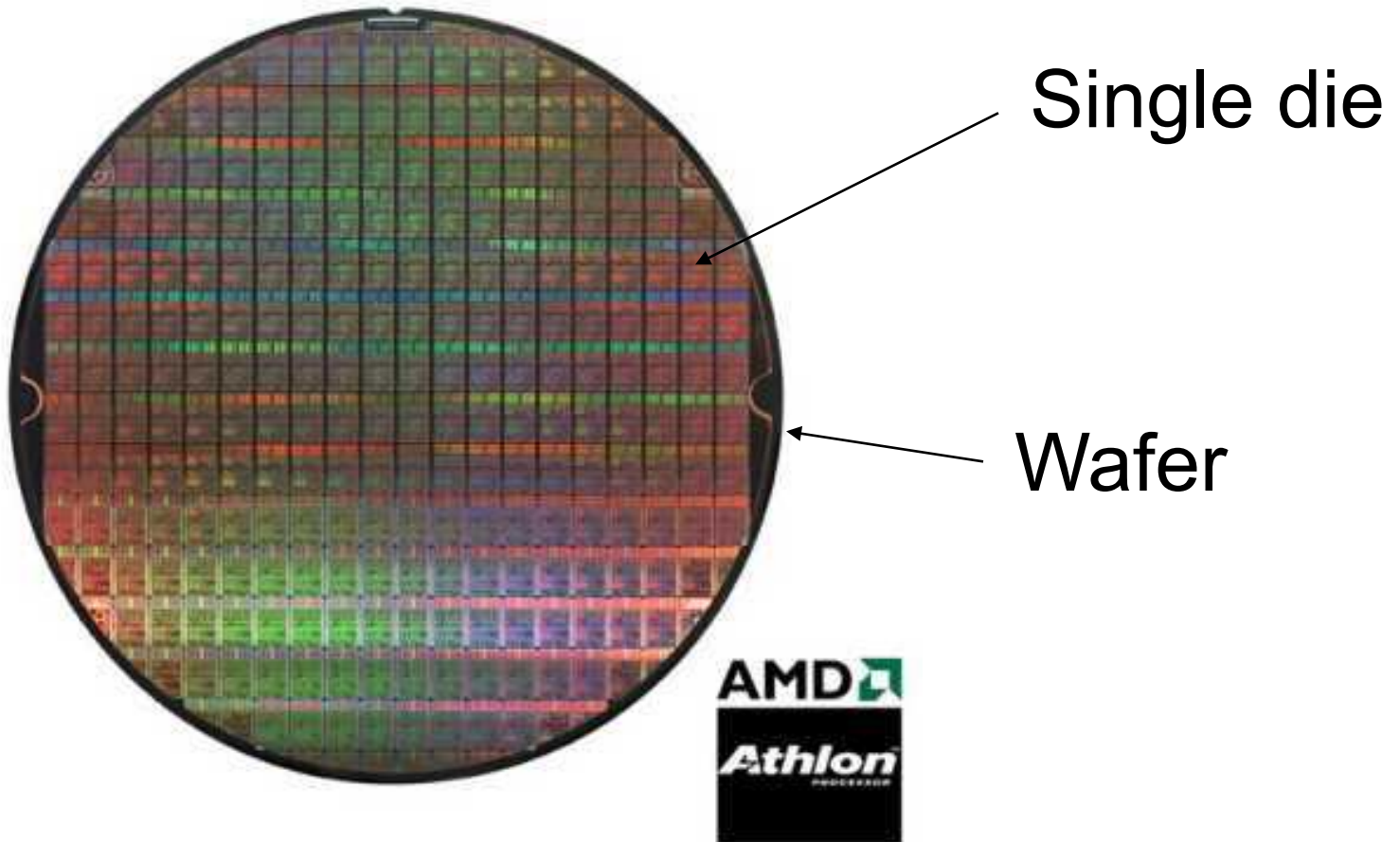
- Esquema Lógico



- Esquema Elétrico CMOS



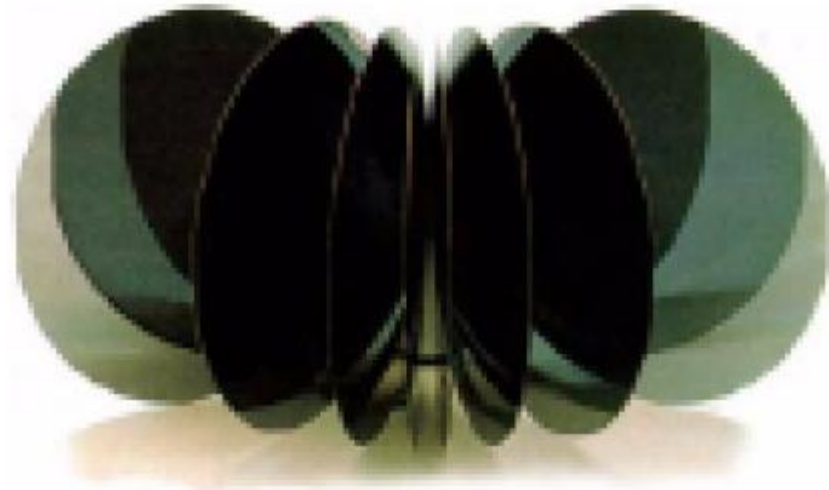
Motivação – Indústria de Circuitos Integrados



Obtido em <http://www.amd.com>

Motivação – Indústria de Circuitos Integrados

- SiO_2 , átomos de silício e oxigênio ligados por seus elétrons.
- O_2 é retirado em laboratório, e os átomos de silício resultantes formam cristal de silício puro.
- Próximo ao zero absoluto, os elétrons de silício se ocupam apenas em manter a estrutura do cristal.
- Aumentando para temperatura ambiente, átomos de Si vibram o suficiente para gerar energia térmica possibilitando seus elétrons saltar para camada de condução.
- Cristal de Silício a ser “fatiado”. Diâmetro varia de 10 a 30 cm.
- Wafers de silício (fatias) com espessura em torno de 1mm.



Tecnologia CMOS: fabricação

Processo de fotolitografia

- Depósito de produto químico (se altera na presença de luz) na superfície do chip;*
- Com lente micro, luz altera regiões do material com produto químico;*
- Solvente remove regiões alteradas;*
- Regiões não atingidas pela luz permanecem, formando transistores;*
- Processo se repete, com outros produtos, formando também isoladores e conexões.*

Remoção do revestimento foto-resistivo (*ashing*)

Outras etapas do processo

Girar, lavar, secar (*spin, rinse, dry*)

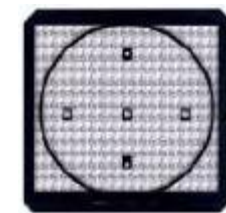
Ataque ácido

Desenvolvimento foto-resistivo

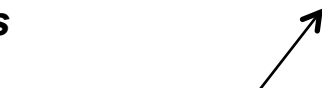
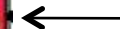
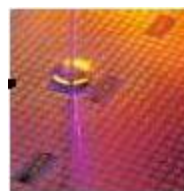
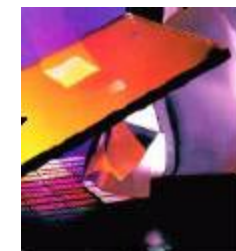
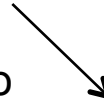
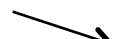
Revestimento foto-resistivo

Oxidação

Máscara Óptica



Exposição UV (*stepper exposure*)



Portas Lógicas Básicas e Tabela Verdade



OR

A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

$$S = A \text{ or } B$$

$$S = A + B$$

$$S = A | B$$

AND

A	B	S
0	0	0
0	1	0
1	0	0
1	1	1

$$S = A \text{ and } B$$

$$S = A \cdot B$$

$$S = A \& B$$

XOR

A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

$$S = A \text{ xor } B$$

$$S = A \oplus B$$

$$S = A \wedge B$$

NOT

A	S
0	1
1	0

$$S = \text{not } A$$

$$S = \bar{A}$$

$$S = !A$$

Tarefa a ser realizada na aula prática

Tarefa a ser realizada na aula prática

- **Utilizando a ferramenta Quartus II da Altera, criar um projeto de circuito digital (esquemático) com as 4 portas lógicas apresentadas no slide 9. Pode ser um circuito qualquer, com apenas uma das portas lógicas, ou um meio somador usando duas das portas, por exemplo.**
- **Realizar a simulação no Modelsim, visando descobrir a tabela verdade do circuito desenvolvido.**
- **O objetivo principal dessa aula prática é possibilitar que o aluno tenha um primeiro contato com as ferramentas de desenvolvimento a serem utilizadas durante o semestre.**
- **Seguir o tutorial existente na seção “Laboratory assignment” do capítulo 1 do livro texto.**
- **Um resumo desse tutorial está incluído nos slides a seguir.**

1. Edição do circuito

Criar um novo projeto

The image shows the Quartus II 64-Bit software interface. The 'File' menu is open, and the 'New Project Wizard...' option is highlighted in orange. A large red arrow points to this option. The background displays the 'ALTERA QUARTUS II Version 15.0' splash screen. The bottom status bar shows the message 'Starts the New Project Wizard'.

Quartus II 64-Bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4

ALTERA
QUARTUS[®] II
Version 15.0

Buy Software
Download New Software Release
Documentation
Notification Center

Messages
System Processing
Starts the New Project Wizard

100% 00:01:28

Escolher a pasta e nome do projeto

New Project Wizard

Directory, Name, Top-Level Entity

What is the working directory for this project?

 ...

What is the name of this project?

 ...

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

 ...

Use Existing Project Settings...

[Help](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Seleccionar o dispositivo alvo (FPGA)

New Project Wizard

Family & Device Settings

Select the family and device you want to target for compilation.

You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Devices: Cyclone V SE Mainstream

Show in 'Available devices' list

Package: Any

Pin count: Any

Core Speed grade: Any

Name filter:

Show advanced devices

Target device

- Auto device selected by the Fitter
- Specific device selected in 'Available devices' list
- Other: n/a

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	
5CSEMA5U23C8	1.1V	32070	314	314	0	0	0
5CSEMA5U23I7	1.1V	32070	314	314	0	0	0
5CSEMA6F31A7	1.1V	41910	457	457	0	0	0
5CSEMA5F31C6	1.1V	41910	457	457	0	0	0
5CSEMA6F31C7	1.1V	41910	457	457	0	0	0

Help

< Back

Next >

Finish

Cancel

Configurar a ferramenta de simulação

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

Criar um novo diagrama de esquemático

The screenshot shows the Quartus II 15.0 software interface. The 'File' menu is open, and a red arrow points to the 'New...' option. The background features the 'ALTERA QUARTUS II Version 15.0' logo. The bottom of the screen shows a 'Messages' panel with 'System' and 'Processing' tabs, and a status bar with '100%' and '00:01:28'.

File Edit View Project Assignments Processing Tools Window Help

New...
Open...
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4

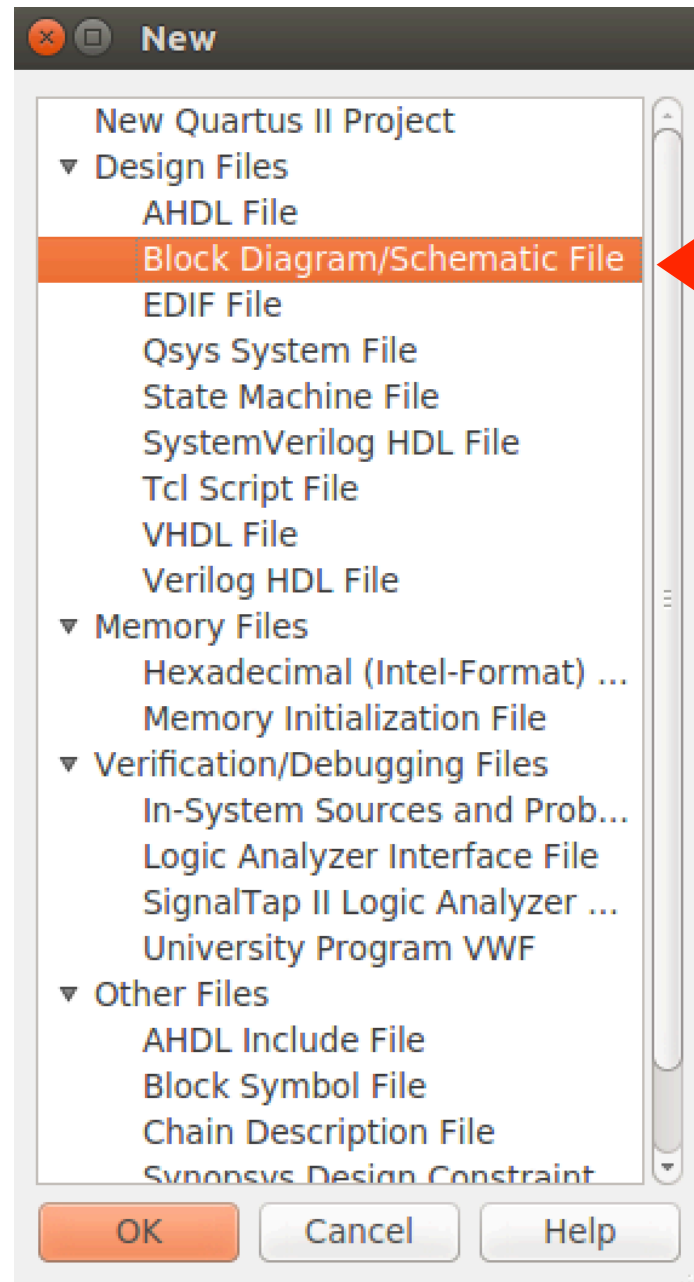
ALTERA
QUARTUS® II
Version 15.0

Buy Software
Download New Software Release
Documentation
Notification Center

Messages
System Processing

100% 00:01:28

Criar um novo diagrama de esquemático



Entrar com as portas lógicas

Quartus II 64-Bit - /home/parallels/Documents/halfadder/halfadder - halfadder

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Block1.bdf

Entity

Cyclone V: 5CSEMA6F31C6

halfadder

Symbol

Libraries:

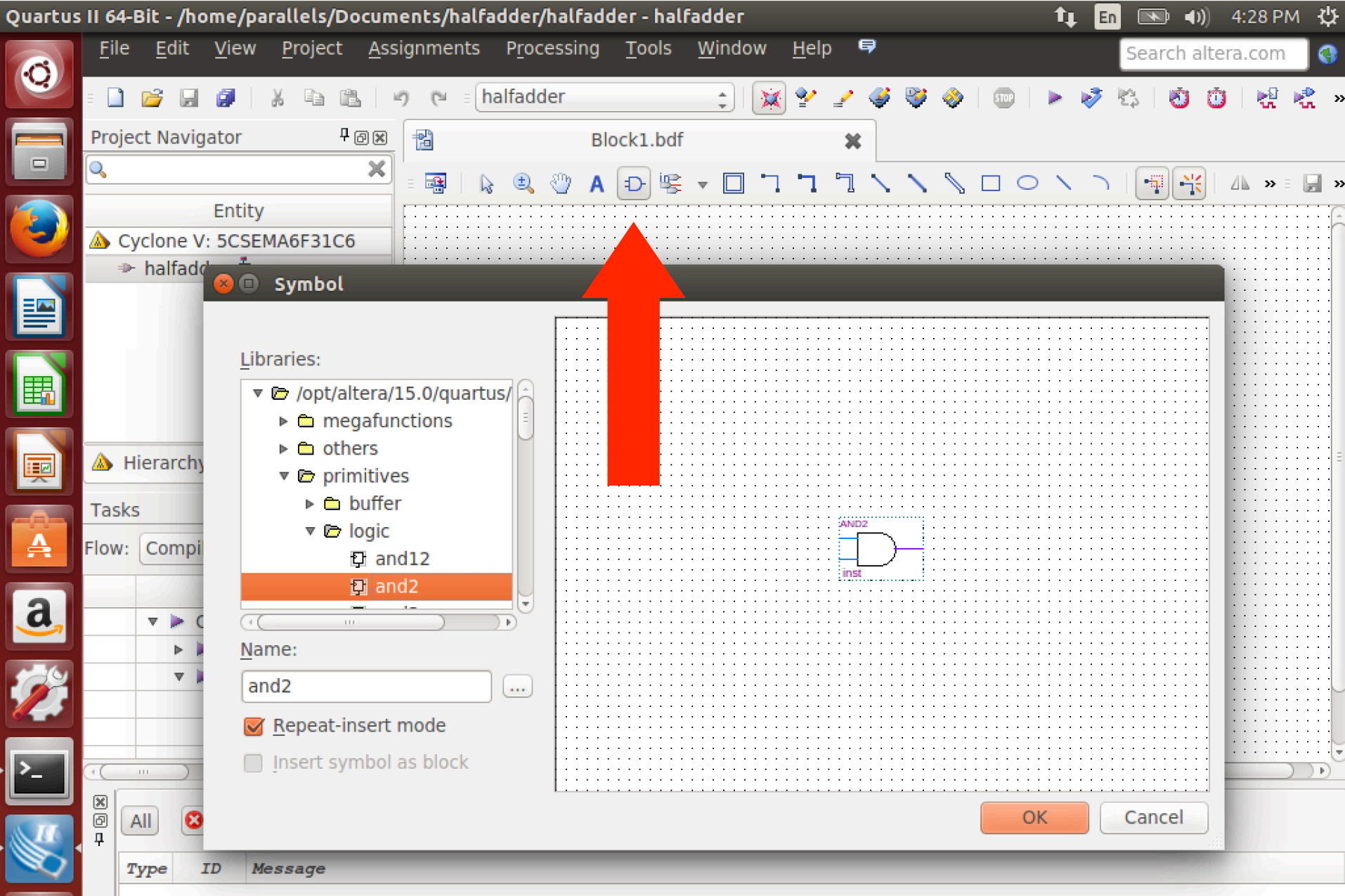
- /opt/altera/15.0/quartus/
 - megafunctions
 - others
 - primitives
 - buffer
 - logic
 - and12
 - and2**

Name: and2

Repeat-insert mode

Insert symbol as block

OK Cancel



The image shows the Quartus II software interface. The main workspace displays a grid with a small AND gate symbol labeled 'AND2 inst'. A red arrow points from the 'Symbol' dialog box to the workspace. The 'Symbol' dialog box is open, showing the 'Libraries' section with the path '/opt/altera/15.0/quartus/' and the 'primitives/logic' folder expanded. The 'and2' component is selected in the list. The 'Name' field contains 'and2', and the 'Repeat-insert mode' checkbox is checked. The 'OK' and 'Cancel' buttons are visible at the bottom of the dialog.

Realizar as conexões das portas lógicas

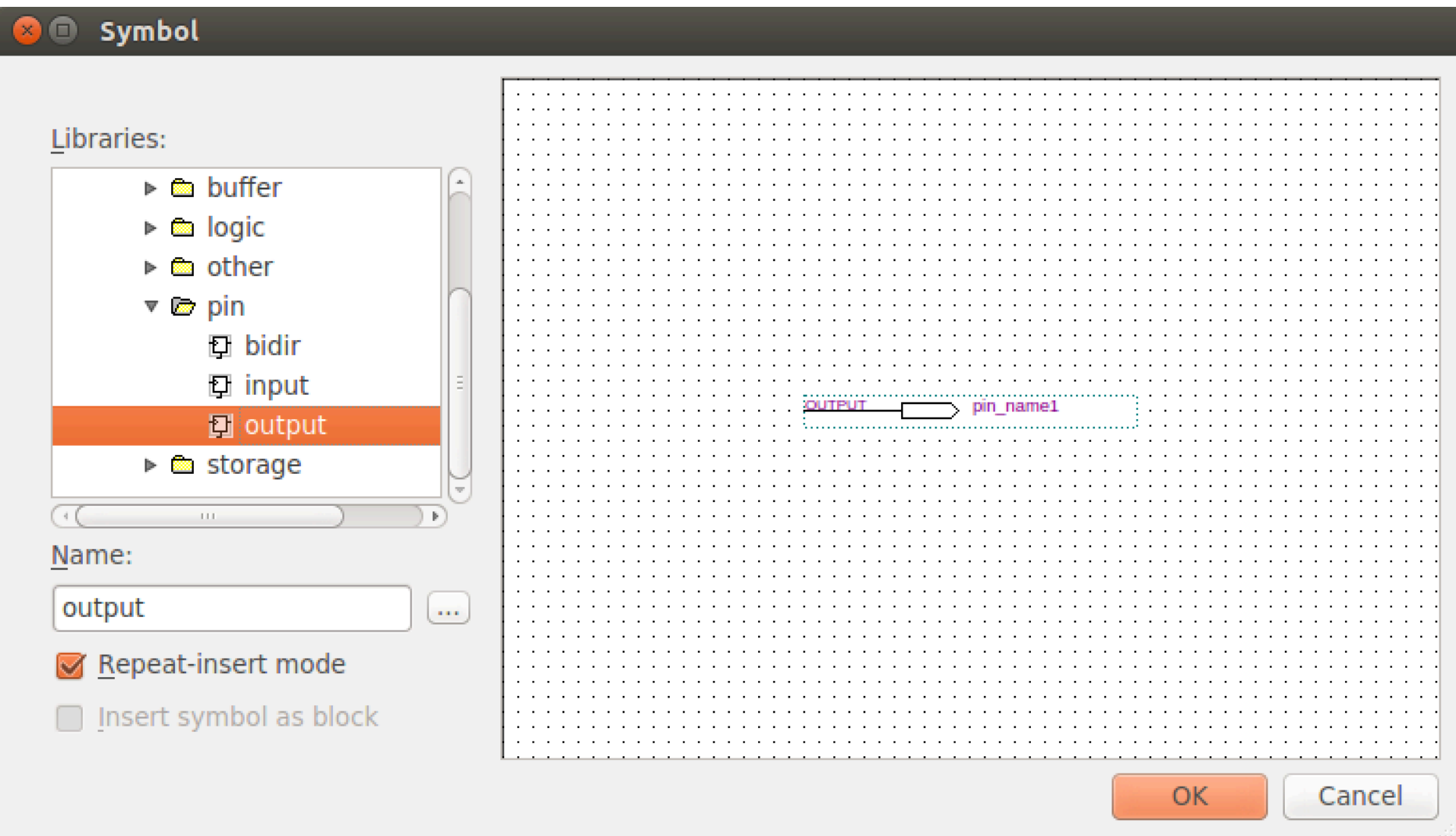
The image shows the Altera Quartus II software interface for designing a half adder. The main workspace displays a logic diagram with the following components:

- Two input ports labeled **A0** and **B0**.
- An XOR gate labeled **XOR** with instance **inst2**.
- An AND2 gate labeled **AND2** with instance **inst1**.

The diagram shows the inputs A0 and B0 connected to the inputs of both the XOR and AND2 gates. A large red arrow points to the connection point between the two inputs and the XOR gate.

The interface includes a Project Navigator on the left showing the project name **Cyclone V: 5CSEMA6F31C6** and the design file **halfadder**. The top menu bar includes **File**, **Edit**, **View**, **Project**, **Assignments**, **Processing**, **Tools**, **Window**, and **Help**. The top status bar shows the time **4:31 PM** and the language **En**.

Entrar com os pinos de entrada e saída



Conectar os pinos de entrada e saída e as portas lógicas

Quartus II 64-Bit - /home/parallels/Documents/halfadder/halfadder - halfadder

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

- Cyclone V: 5CSEMA6F31C6
 - halfadder

Hierarchy Files

Tasks

Flow: Compilati Customize...

Task

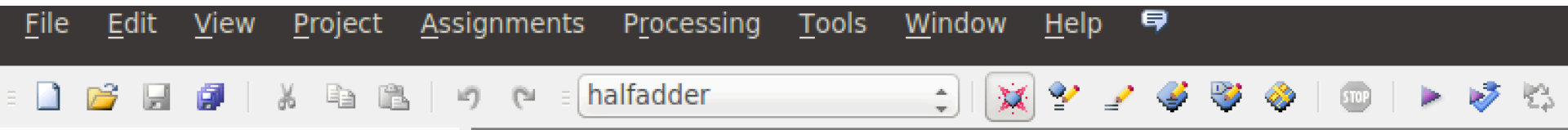
- Compile Design
 - Analysis & Synthe
 - Fitter (Place & Ro
 - Edit Settings
 - View Report
 - Chip Planner

Block1.bdf*

The diagram shows a logic circuit for a half adder. It features two input pins labeled 'A0' and 'B0'. These inputs are connected to two logic gates: an XOR gate (labeled 'inst2') and an AND2 gate (labeled 'inst1'). The output of the XOR gate is connected to an output pin labeled 'S0', and the output of the AND2 gate is connected to an output pin labeled 'C0'. The circuit is implemented on a Cyclone V: 5CSEMA6F31C6 device.

2. Síntese – criação do “hardware”

Realizar a síntese do circuito (*compile*)



3. Simulação

Configurar a ferramenta de simulação

Quartus II 64-Bit - /home/parallels/Documents/halfadder/halfadder - halfadder

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Entity

- Cyclone V: 5CSEMA6F31C6
 - halfadder

Hierarchy Files

Tasks

Flow: Compilati Customize...

- Compile Design
 - Analysis & Synthe
 - Fitter (Place & Ro
 - Edit Settings
 - View Report
 - Chip Planner

Messages

All [Icons] <<Filter>>

Type	ID	Message
------	----	---------

Run Simulation Tool

Launch Simulation Library Compiler

Launch Design Space Explorer II

TimeQuest Timing Analyzer

Advisors

Chip Planner

Design Partition Planner

Netlist Viewers

SignalTap II Logic Analyzer

In-System Memory Content Editor

Logic Analyzer Interface Editor

In-System Sources and Probes Editor

SignalProbe Pins...

Programmer

JTAG Chain Debugger

Fault Injection Debugger

System Debugging Tools

IP Catalog

Nios II Software Build Tools for Eclipse

Qsys

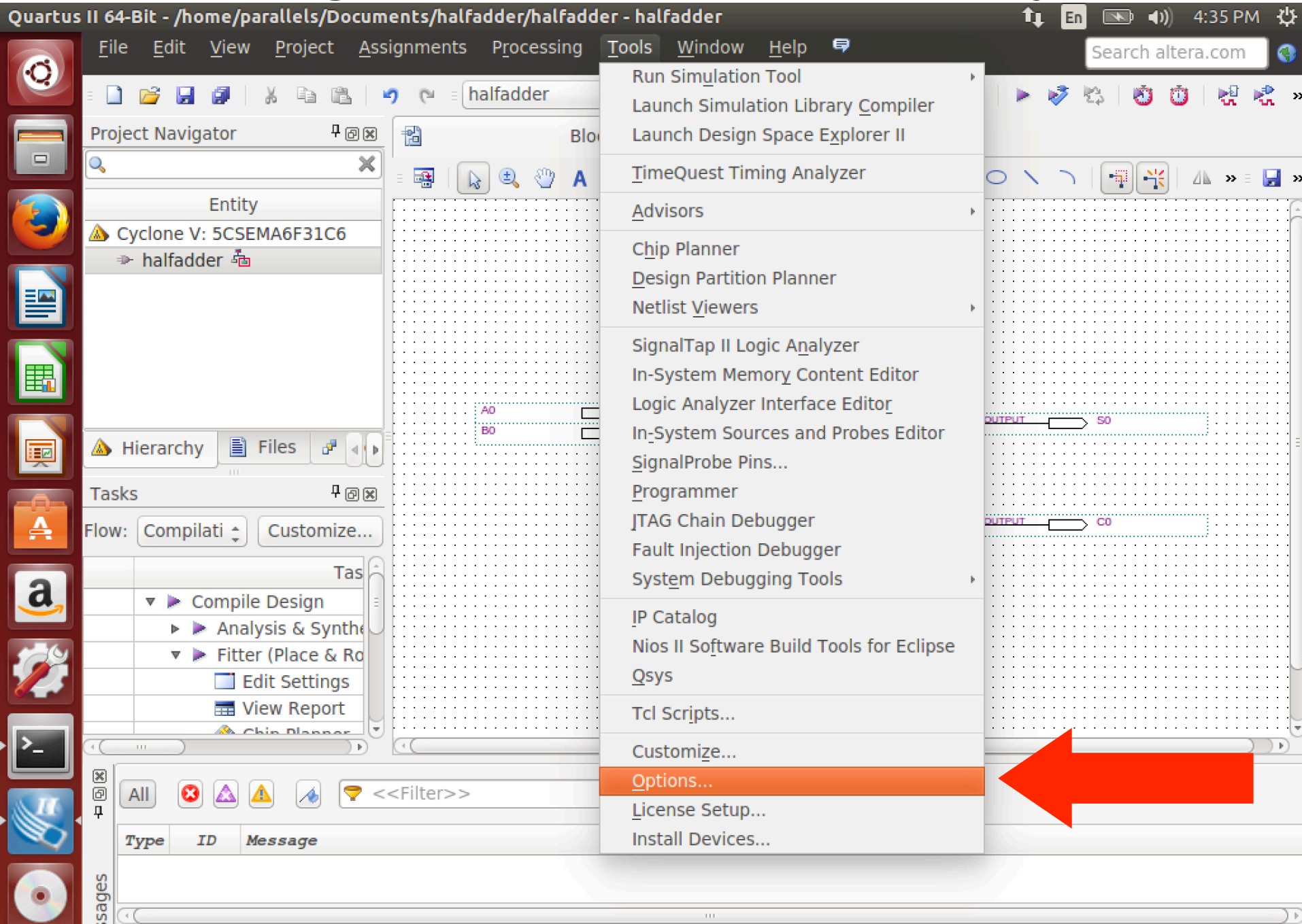
Tcl Scripts...

Customize...

Options...

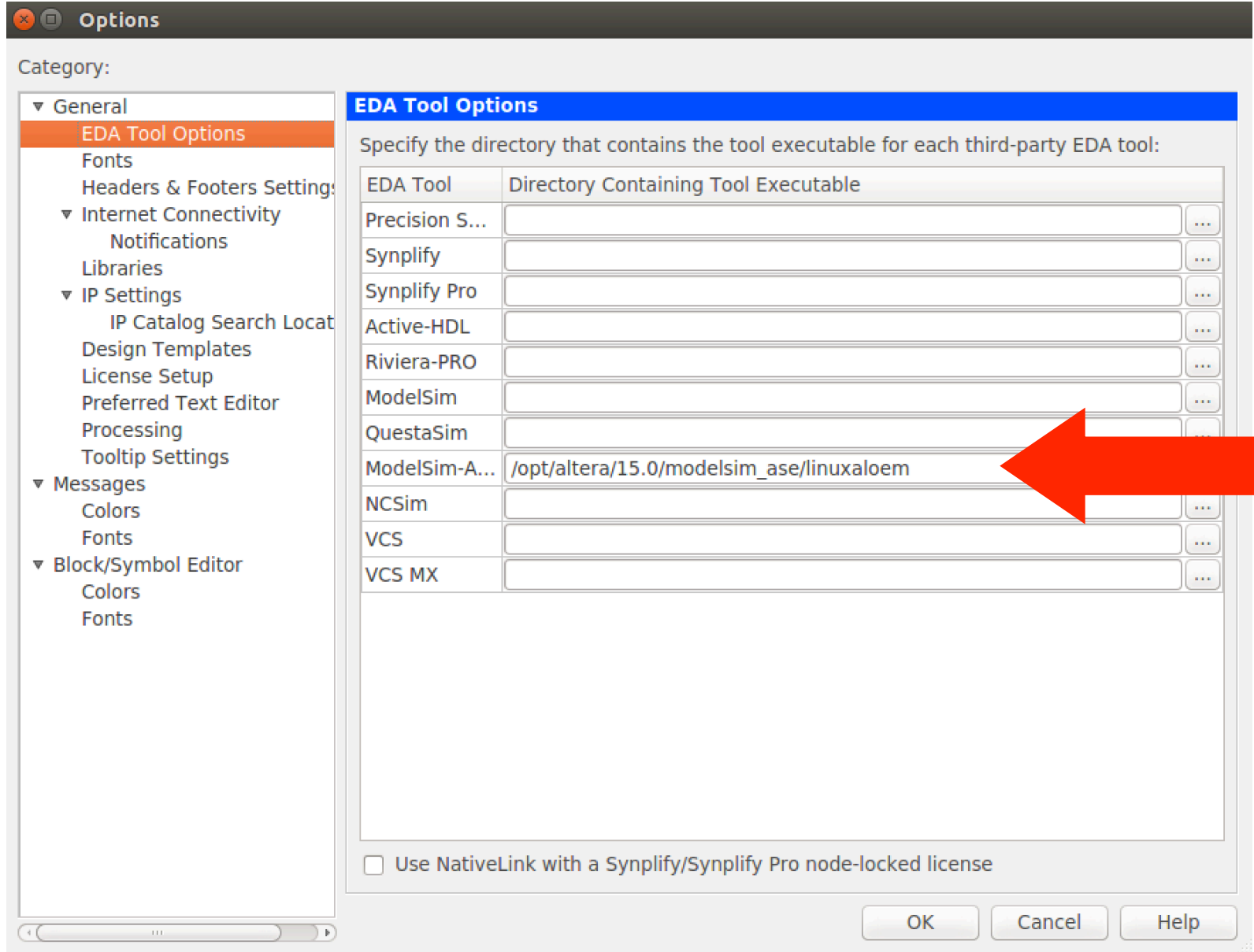
License Setup...

Install Devices...

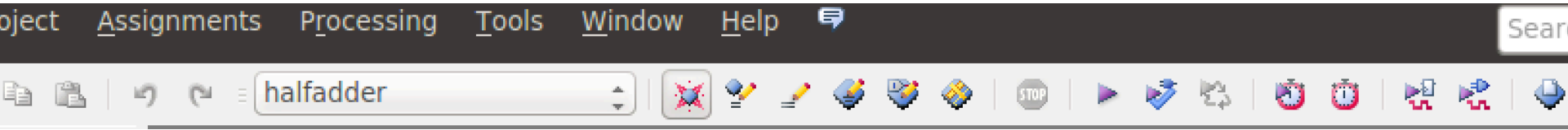


The screenshot shows the Quartus II software interface. The 'Tools' menu is open, and the 'Options...' item is highlighted in orange. A large red arrow points from the right side of the screen towards the 'Options...' menu item. The background shows the Project Navigator with the 'halfadder' entity selected, and the main workspace displaying a logic diagram with signals 'AD', 'BO', 'S0', and 'CO'.

Configurar a ferramenta de simulação



Executar o ModelSim (ferramenta de simulação)




Executar o ModelSim (ferramenta de simulação)

Obs. Caso o ModelSim não venha a ser executado ao pressionar o botão indicado, digitar *vsim* no terminal do Linux, para executar o ModelSim via linha de comando.

```
[1]+ Done          quartus
parallels@ubuntu:~$
parallels@ubuntu:~$ quartus &
[1] 7390
parallels@ubuntu:~$ Inconsistency detected by ld.so: dl-close.c: 762: _dl_close:
Assertion `map->l_init_called' failed!

parallels@ubuntu:~$
parallels@ubuntu:~$ vsim &
[2] 15290
parallels@ubuntu:~$ Reading pref.tcl
```



Obs. Se a biblioteca work não for apresentada:

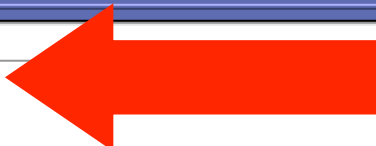
ModelSim ALTERA STARTER EDITION 10.3d - Custom Altera Version

File Edit View Compile Simulate Add **Library** Tools Layout Bookmarks Window Help

ColumnLayout AllColumns

Layout NoDesign

Name	Type	Path
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_insim	Library	\$MODEL_TECH/./altera/vhdl/altera_In...
altera_insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera_...
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera_...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii_...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_pc...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii_...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz_...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiig...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz_...
arriaiigz_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiig...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriav_...
arriav_pcie_hip_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav_...



**Obs. Se a biblioteca work não for apresentada:
*Pressionar o Compile, e procurar o arquivo criado.***

ModelSim ALTERA STARTER EDITION 10.3d - Custom Altera Version

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

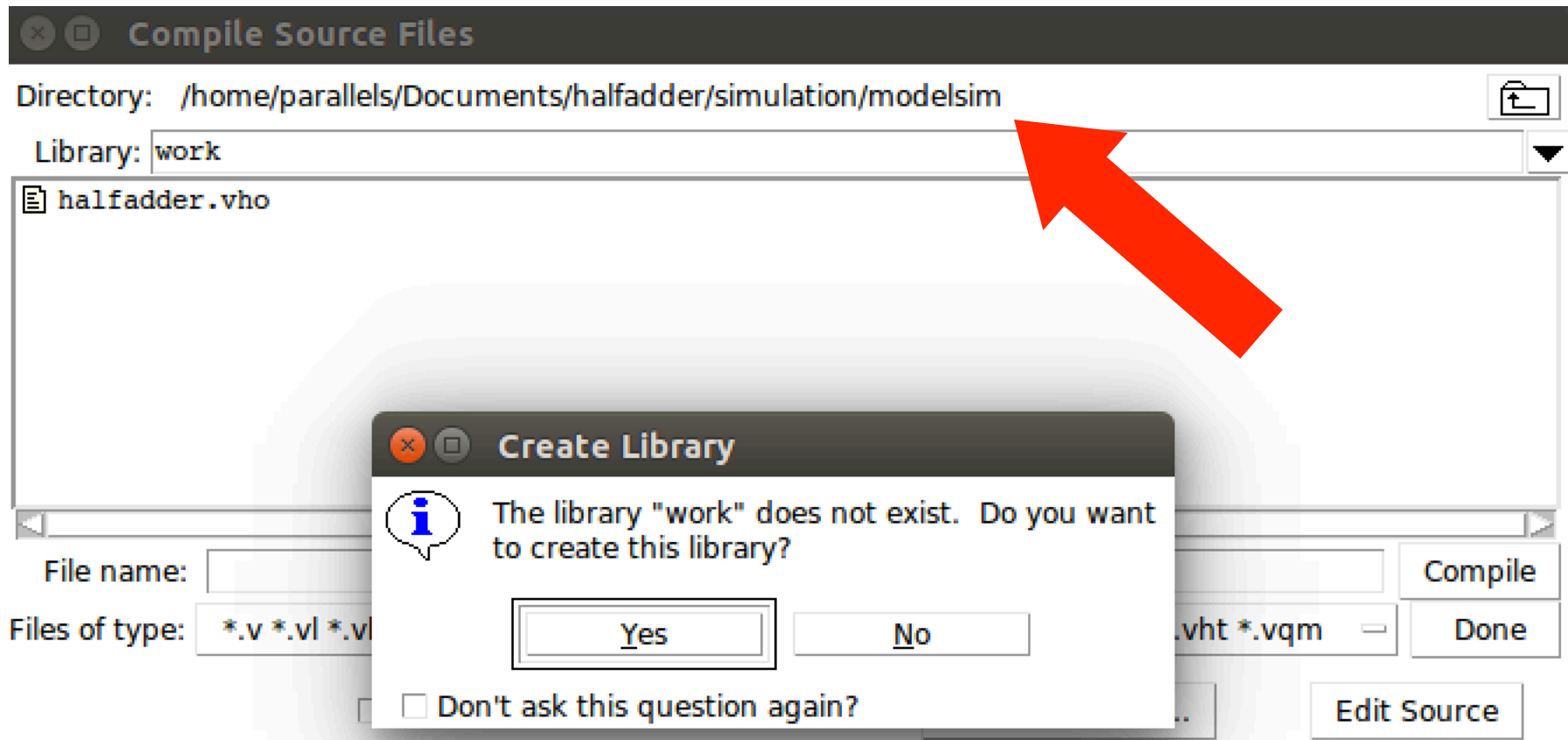
ColumnLayout AllColumns

Layout NoDesign

Library

Name	Type	Path
220model	Library	\$MODEL_TECH/./altera/220model
220model_ver	Library	\$MODEL_TECH/./altera/220m...
altera	Library	\$MODEL_TECH/./altera
altera_insim	Library	\$MODEL_TECH/./altera/altera_In...
altera_insim_ver	Library	\$MODEL_TECH/./altera/altera_...
altera_mf	Library	\$MODEL_TECH/./altera/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera_...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii_...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_pc...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii_...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz_...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiig_...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz_...
arriaiigz_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiig_...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriav_...
arriav_pcie_hip_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav_...

**Obs. Se a biblioteca work não for apresentada:
*Pressionar o Compile, e procurar o arquivo criado no
Quartus. Compilar (Compile) esse arquivo.***



Selecionar o módulo a ser simulado


ModelSim ALTERA STARTER EDITION 10.3d - Custom Altera Version

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

ColumnLayout AllColumns

Library

Name	Type	Path
work	Library	/home/parallels/work
halfadder	Entity	/home/parallels/Documents/halfadder...
structure	Architecture	
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_Insim	Library	\$MODEL_TECH/./altera/vhdl/altera_In...
altera_Insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera_...
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera_...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii_...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_pc...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii_...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz_...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiig...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz_...
arriaiigz_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiig...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (emnt)	Library	\$MODEL_TECH/./altera/verilog/arriav



Adicionar os sinais de interesse ao diagrama de formas de onda

The screenshot displays the ModelSim ALTERA STARTER EDITION 10.3d interface. The main window shows a waveform viewer with a dark background and a time axis at the bottom. A context menu is open over the waveform, with the 'Add to' option selected. This option has opened a sub-menu with the following items:

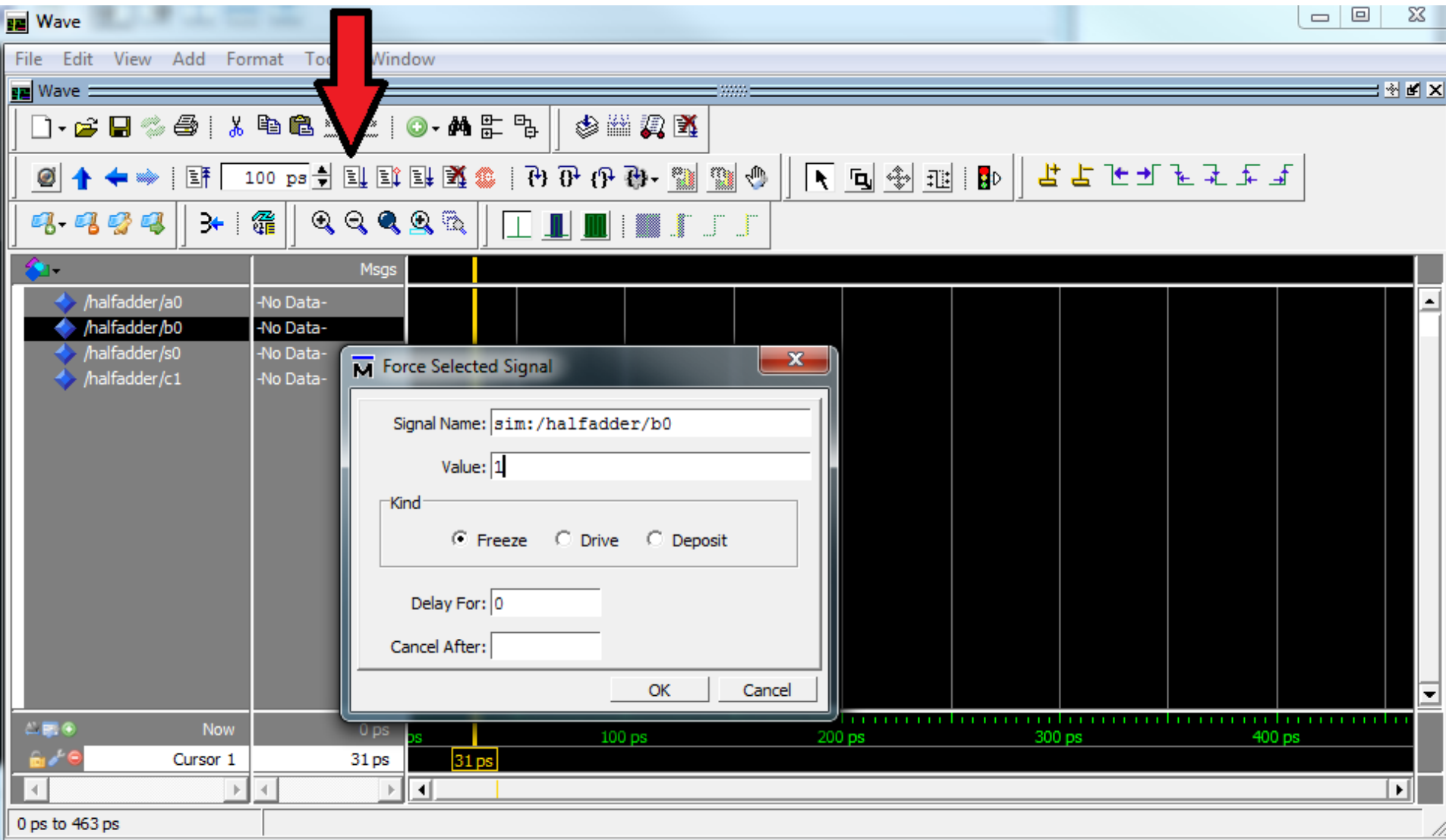
- Wave
- List
- Log
- Dataflow
- Watch

The 'Wave' option is further expanded, showing a sub-menu with the following items:

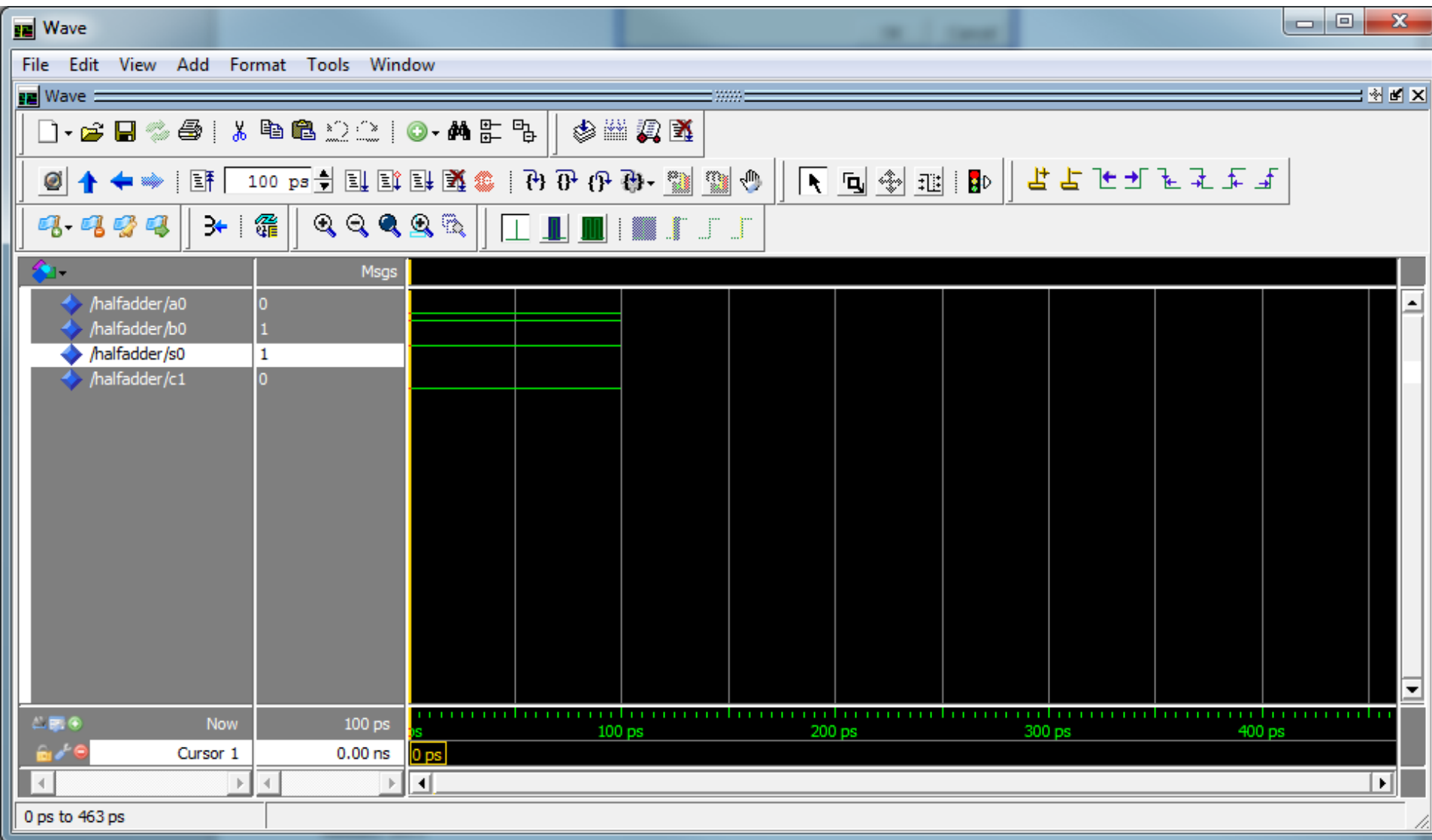
- Selected Signals
- Signals in Region
- Signals in Design

A large red arrow points from the right side of the image towards the 'Selected Signals' option in the sub-menu. The interface also shows a menu bar with options like File, Edit, View, Compile, Simulate, Add, Objects, Tools, Layout, Bookmarks, Window, and Help. The toolbar includes various icons for file operations, simulation control, and waveform manipulation. The 'Layout' dropdown is set to 'Simulate'. The 'ColumnLayout' is set to 'Default'. The 'Instance' pane on the left shows a tree view of the design hierarchy, including components like 'halfa', 'VS', 'VC', 'VA', 'VE', 'in', 'V', 'lir', and 'sim'. The 'Transcript' pane at the bottom left shows the output of the simulation, including the text '# Loading cyclonev.cy' and 'VSIM 4>'. The 'Msgs' pane is also visible, showing a list of messages.

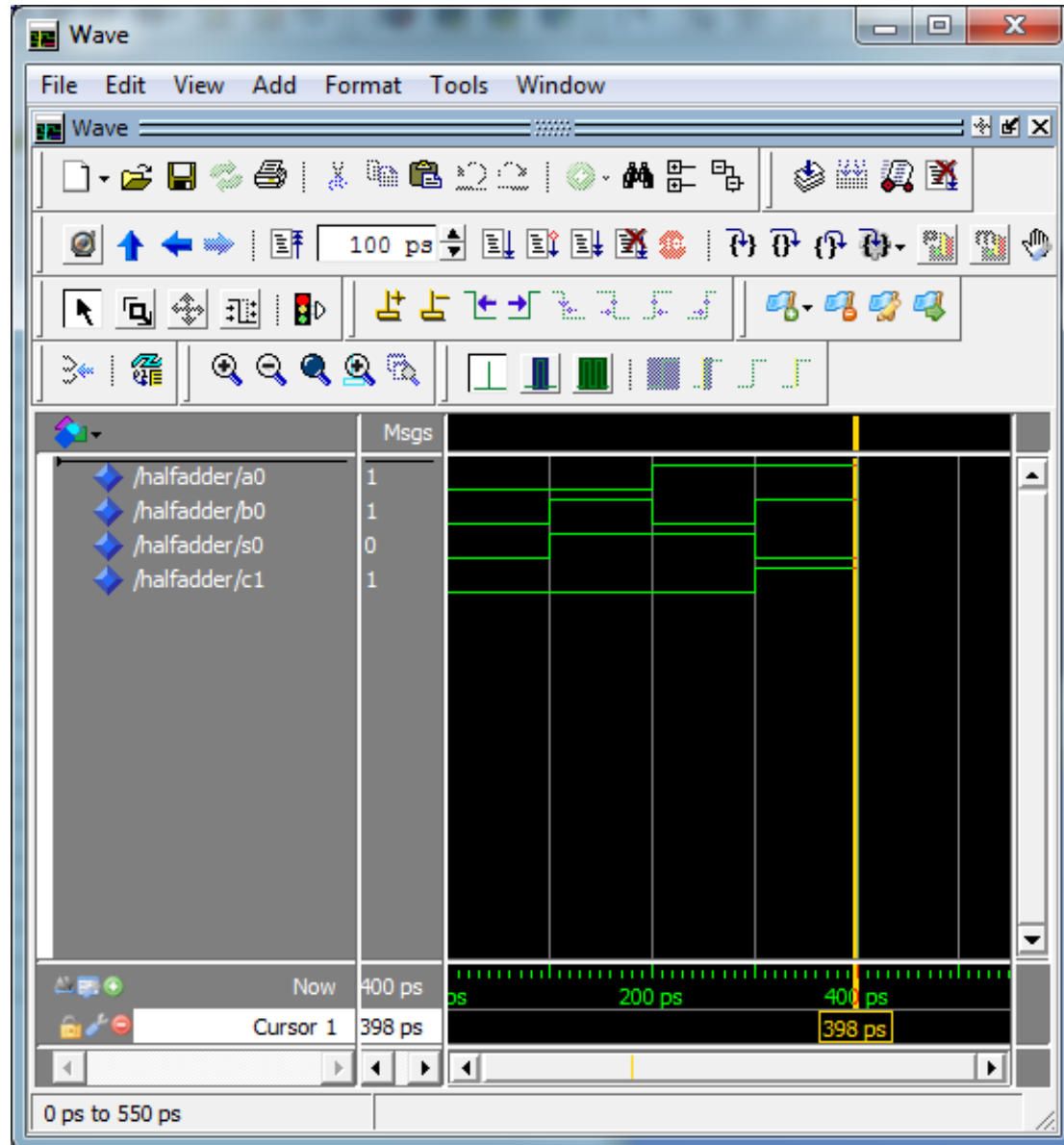
- Fixar os sinais em '0' ou '1' utilizando o botão direito do mouse sobre o sinal desejado.
- Pressionar o botão *Run* indicado na figura.



Para $A0 = '0'$ e $B0 = '1'$, o resultado da simulação será $0 + 1 = 1$ (S0), com vai-um = $'0'$ (C0).



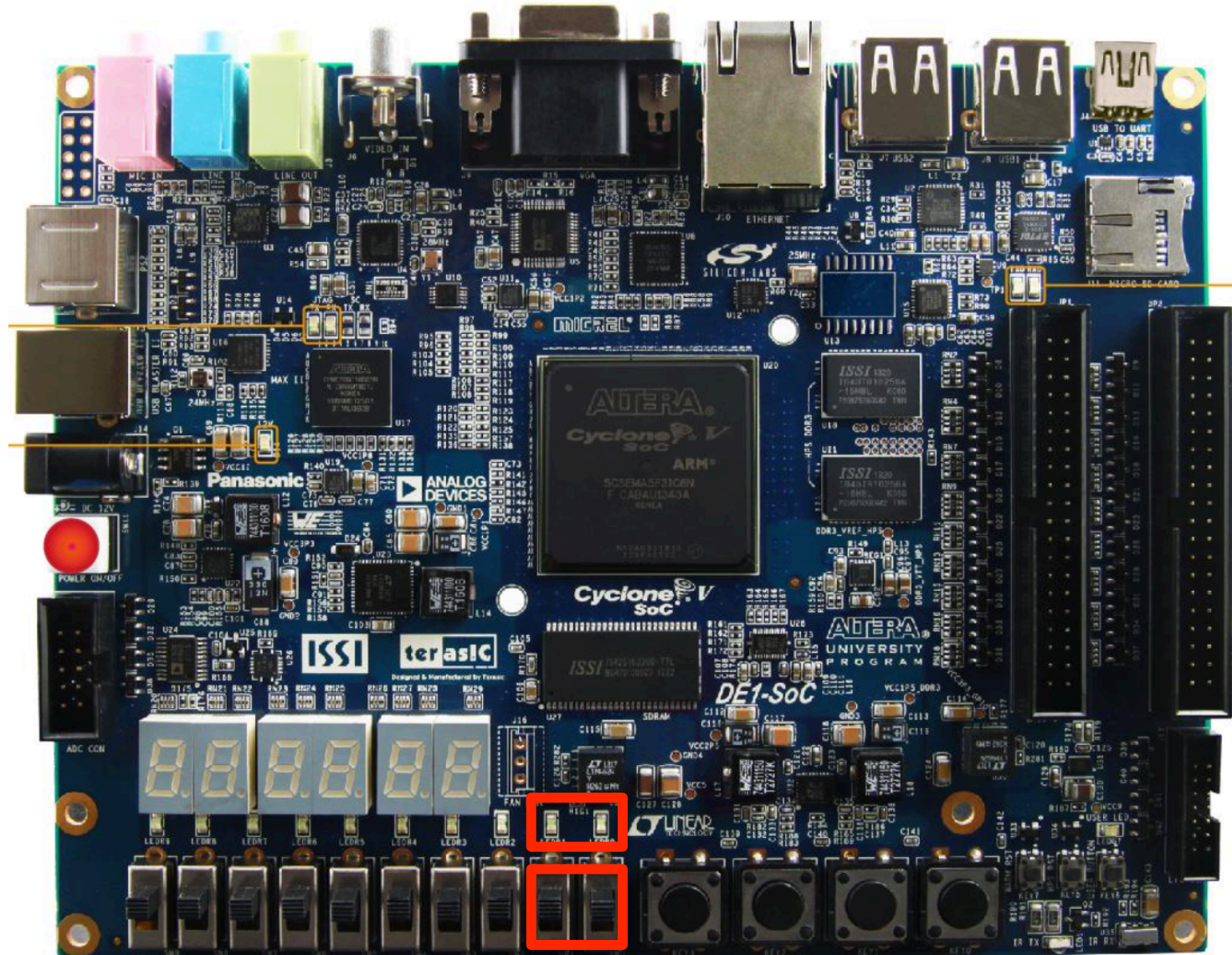
Resultado da simulação para todas as combinações de A0 e B0



4. Prototipação – Teste do circuito no kit de desenvolvimento

Testar o circuito na placa com o FPGA

Primeiro passo, associar os pinos do FPGA aos sinais de entrada e saída definidos no projeto (esquemático).



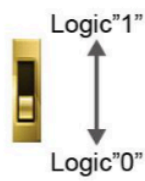
Testar o circuito na placa com o FPGA

Primeiro passo, associar os pinos do FPGA aos sinais de entrada e saída definidos no projeto (esquemático).



a0 = SW0 = PIN_AB12
b0 = SW1 = PIN_AC12

s0 = LED0 = PIN_V16
c1 = LED1 = PIN_W16

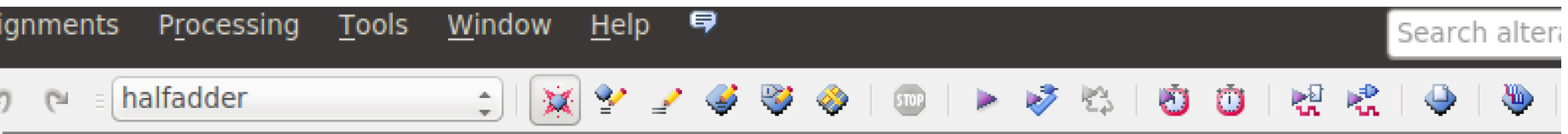


Testar o circuito na placa com o FPGA

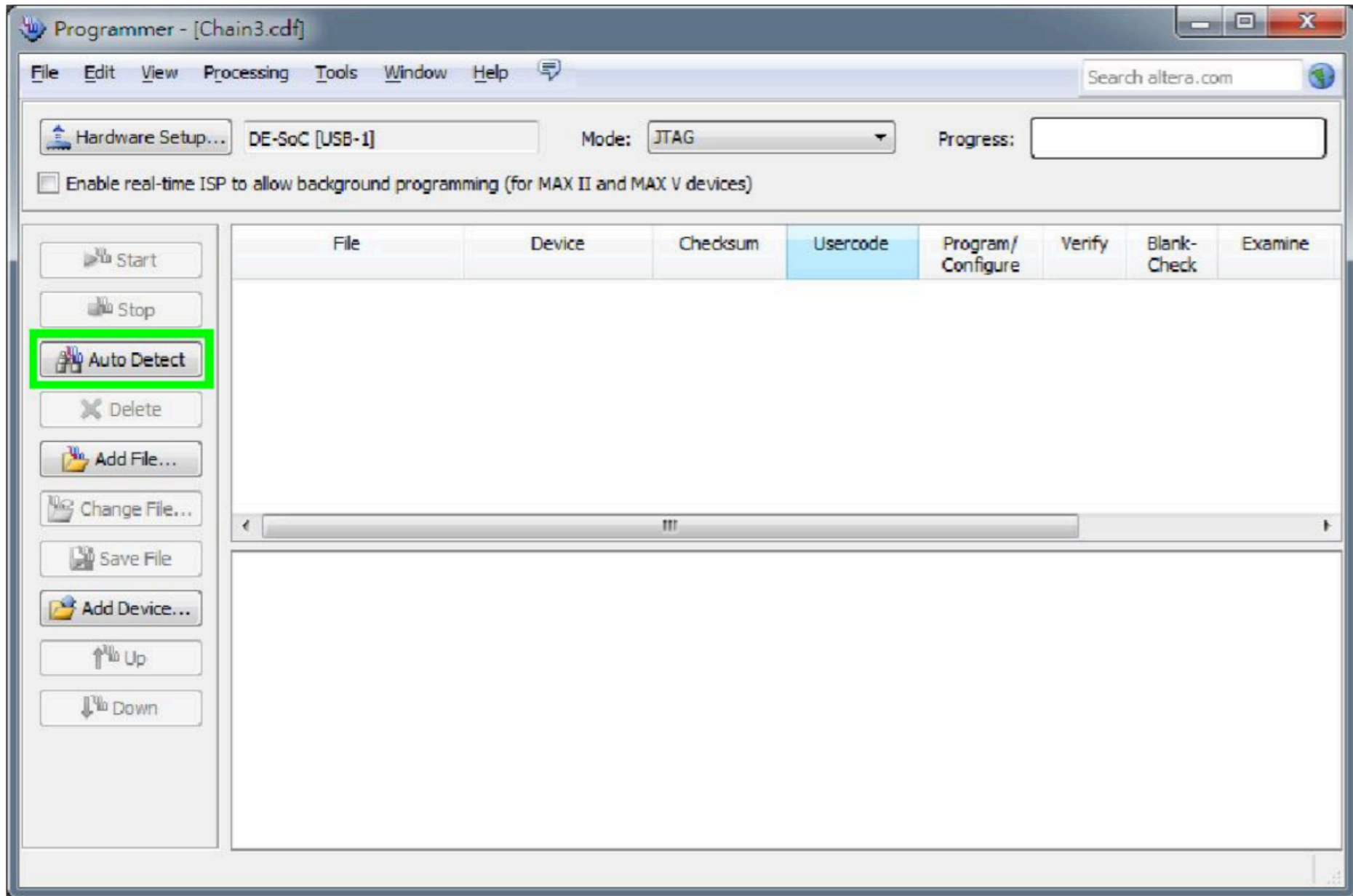
Primeiro passo, associar os pinos do FPGA aos sinais de entrada e saída definidos no projeto (esquemático).

The image shows the Quartus II software interface. The top menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The 'Assignments' menu is open, showing options like Device..., Settings..., Assignment Editor, Pin Planner (highlighted), Remove Assignments..., Back-Annotate Assignments..., Import Assignments..., Export Assignments..., Assignment Groups..., LogicLock Regions Window, and Design Partitions Window. The main workspace displays a logic circuit schematic with inputs A0 and B0, an XOR gate (inst2), an AND gate (inst1), and outputs S0 and C0. The interface also shows a Project Navigator, Hierarchy, Files, Tasks, and a task list on the left side.

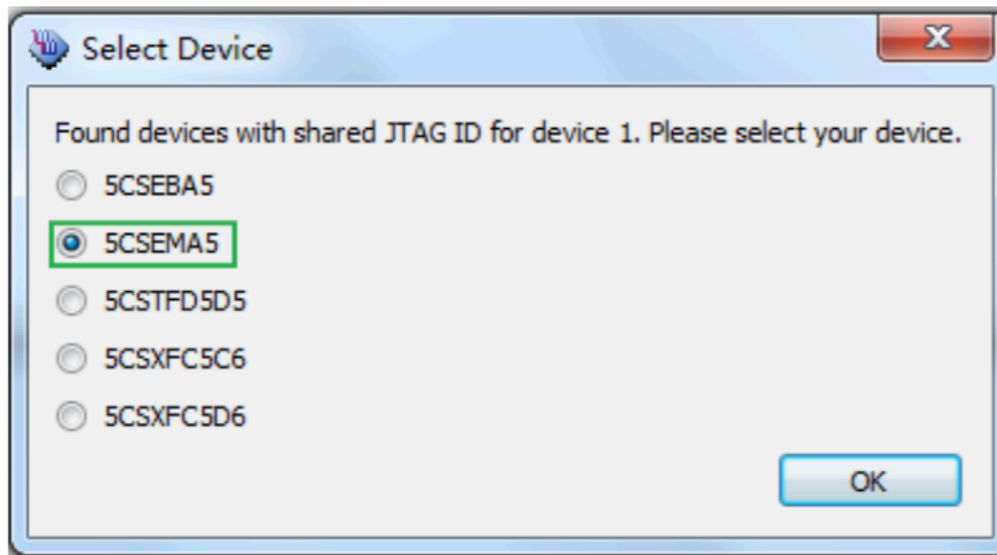
Download do arquivo de configuração para o FPGA



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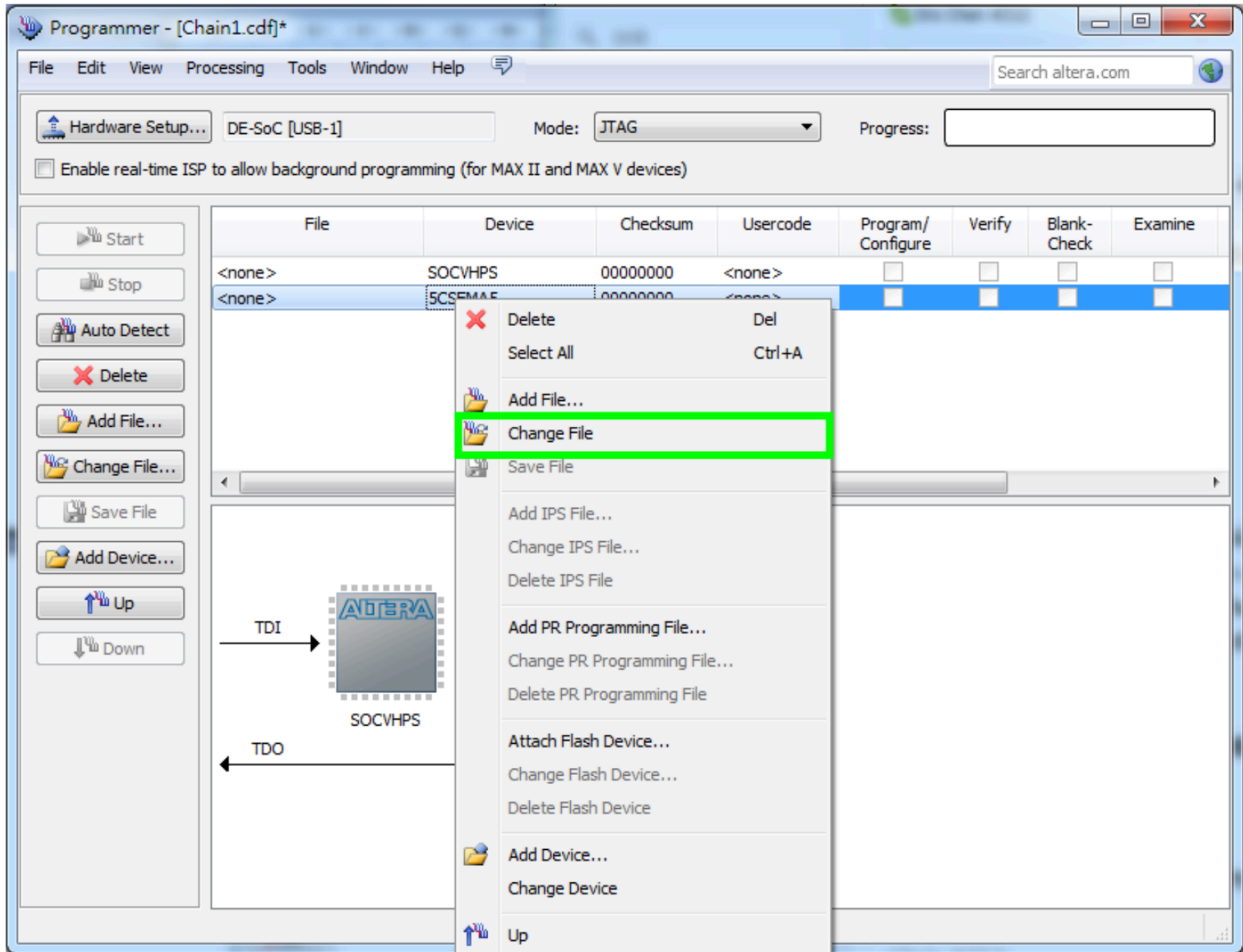
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The screenshot shows the Altera Programmer software interface. The window title is "Programmer - [Chain1.cdf]*". The menu bar includes File, Edit, View, Processing, Tools, Window, and Help. A search bar for "altera.com" is visible. The hardware setup is configured for "DE-SoC [USB-1]" in "JTAG" mode. A progress bar is empty. A checkbox for "Enable real-time ISP to allow background programming (for MAX II and MAX V devices)" is unchecked. On the left, there is a vertical toolbar with buttons for Start, Stop, Auto Detect, Delete, Add File..., Change File..., Save File, Add Device..., Up, and Down. The main area contains a table of the JTAG chain configuration:

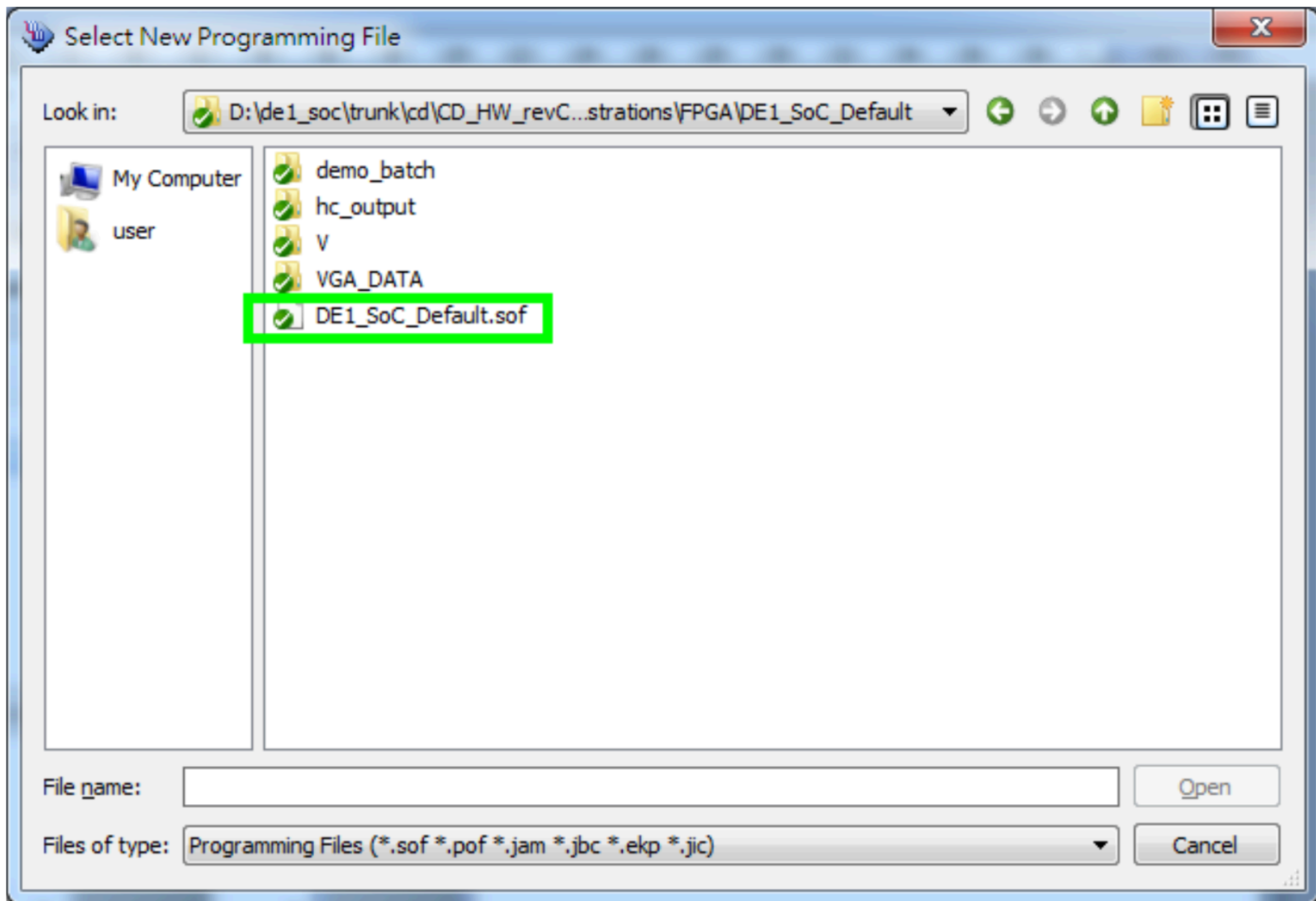
File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine
<none>	SOCVHPS	00000000	<none>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<none>	SCSEMAS	00000000	<none>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Below the table is a diagram of the JTAG chain. It shows two Altera devices connected in series. The first device is labeled "SOCVHPS" and the second is "SCSEMAS". An arrow labeled "TDI" points to the first device. An arrow labeled "TDO" points away from the second device. The devices are connected by a horizontal line, and a vertical line connects the second device to the TDO output.

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The screenshot shows the Altera Programmer software interface. The window title is "Programmer - [Chain1.cdf]*". The hardware setup is "DE-SoC [USB-1]" and the mode is "JTAG". The "Start" button is highlighted with a green box. Below the hardware setup, there is a table with the following data:

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine
<none>	SOCVHPS	00000000	<none>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
D:/de1_soc/trunk/cd/CD_...	5CSEMA5F31	03888274	03888274	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Below the table, there is a diagram illustrating the JTAG connection. It shows two Altera devices: "SOCVHPS" and "5CSEMA5F31". The "SOCVHPS" device is connected to the "5CSEMA5F31" device via a JTAG chain. The "TDI" (Test Data In) signal is connected to the "SOCVHPS" device, and the "TDO" (Test Data Out) signal is connected to the "5CSEMA5F31" device.